A Time-to-Digital Converter with Small Circuitry

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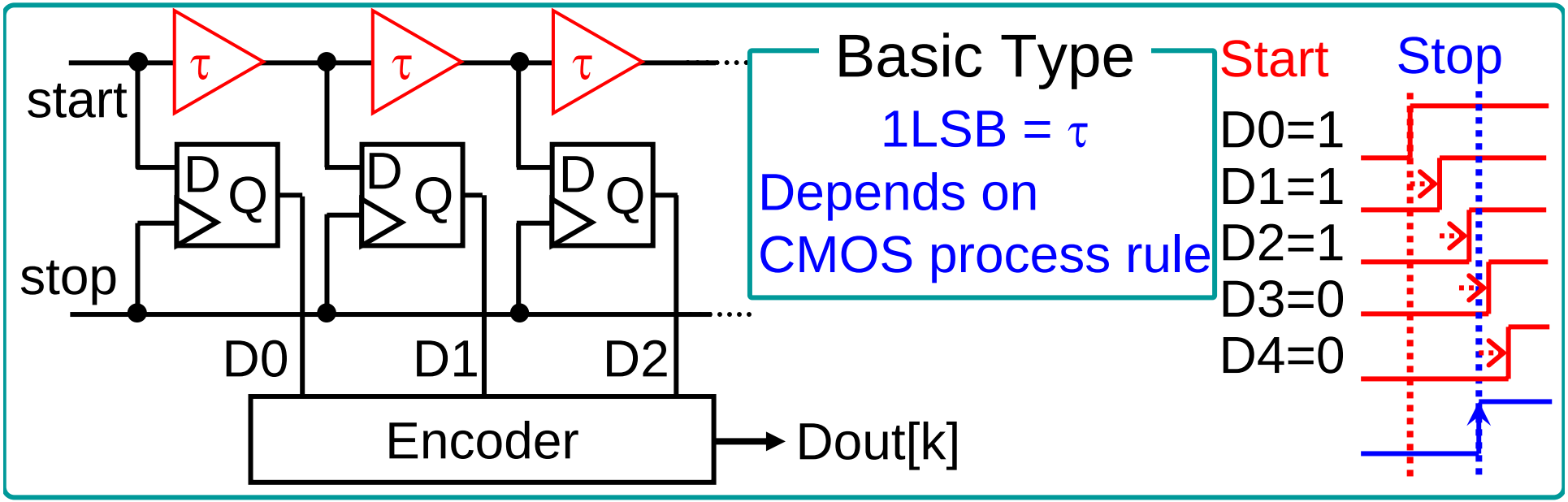
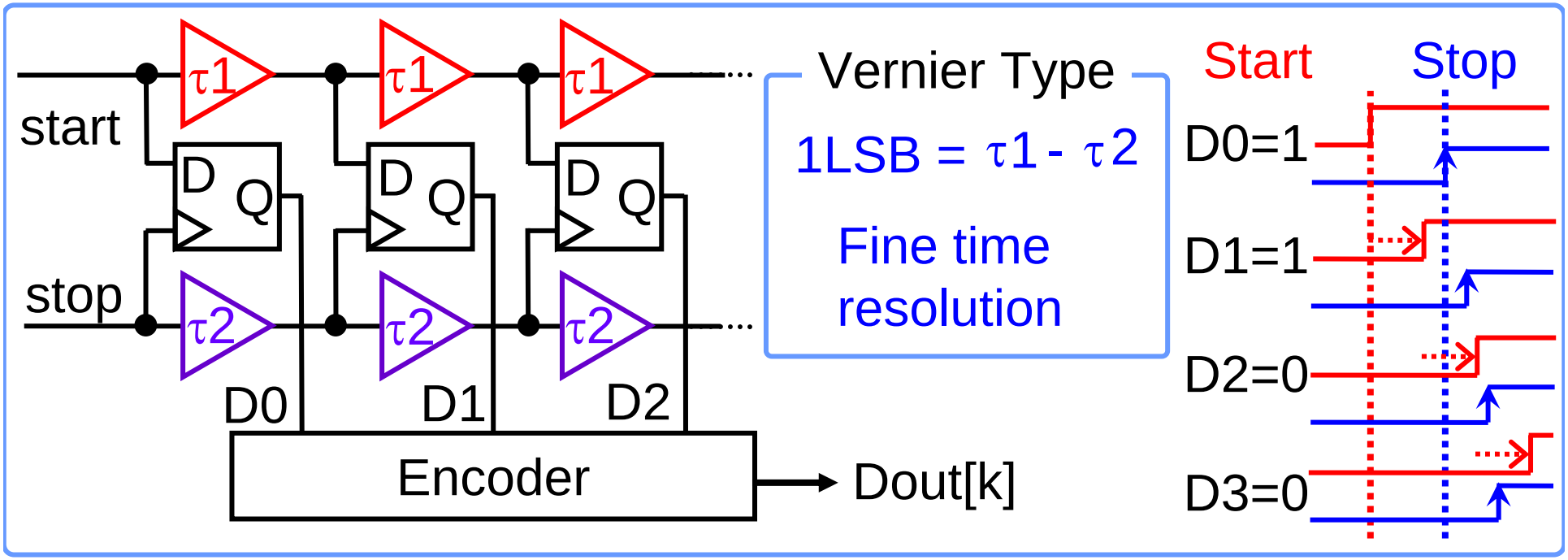
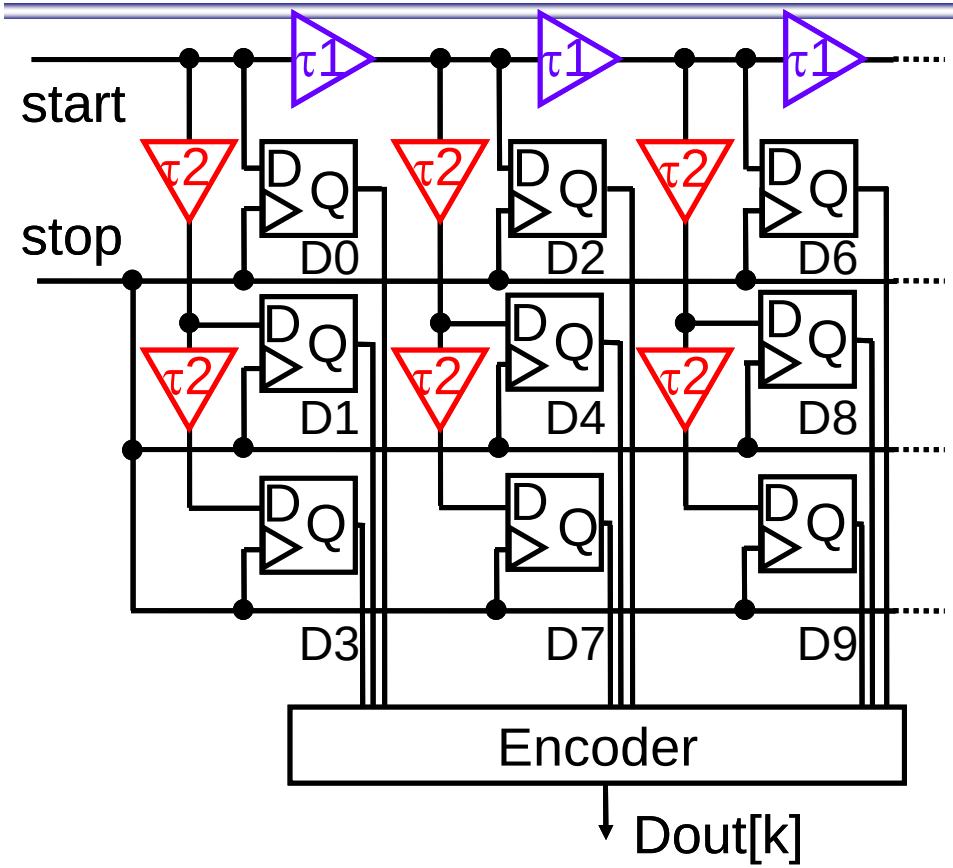
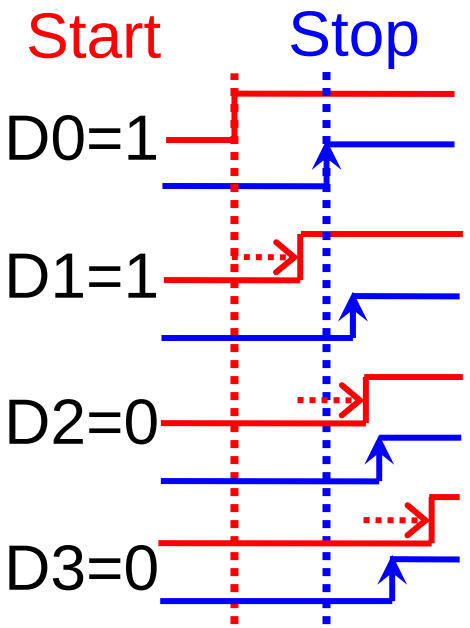
Conventional TDC Architectures





New TDC Architecture

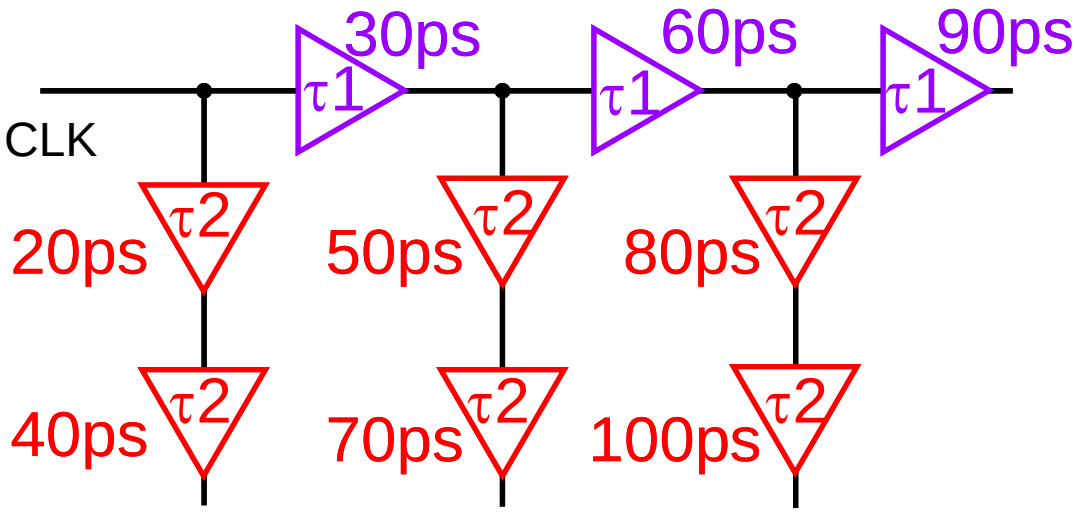




1LSB = τ1 - τ2

Fine time resolution

Small circuitry



Comparison among TDC Architectures

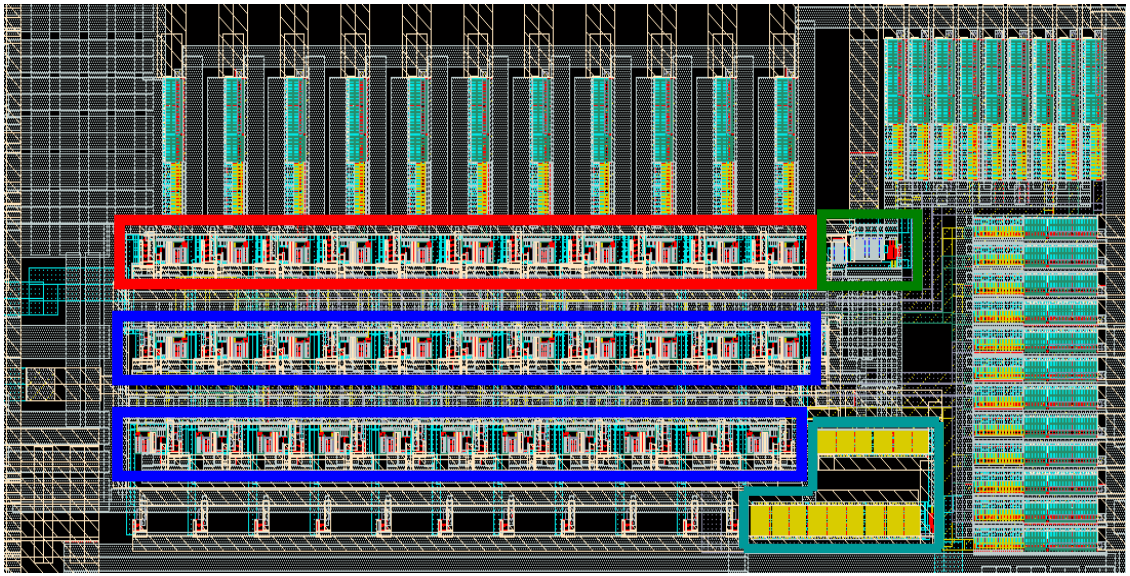
	Basic TDC	Vernier Delay Line TDC	Proposed TDC
Time resolution	$\tau 2$ 20ps	$\tau 1$-$\tau 2$ 10ps	$\tau 1$-$\tau 2$ 10ps
# of delay buffers	19	38	19

$\tau 1$: 30ps $\tau 2$: 20ps
Input range : 0 - 200ps

Proposed TDC Layout and photo

Delay line1

Delay line2

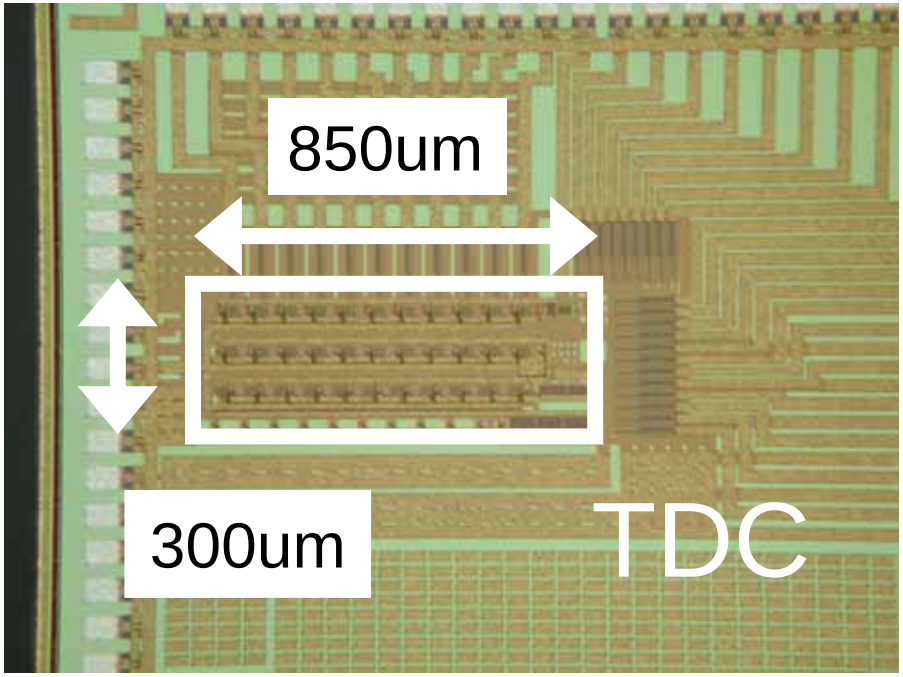


Process:
TSMC 0.18um CMOS (1P6M)

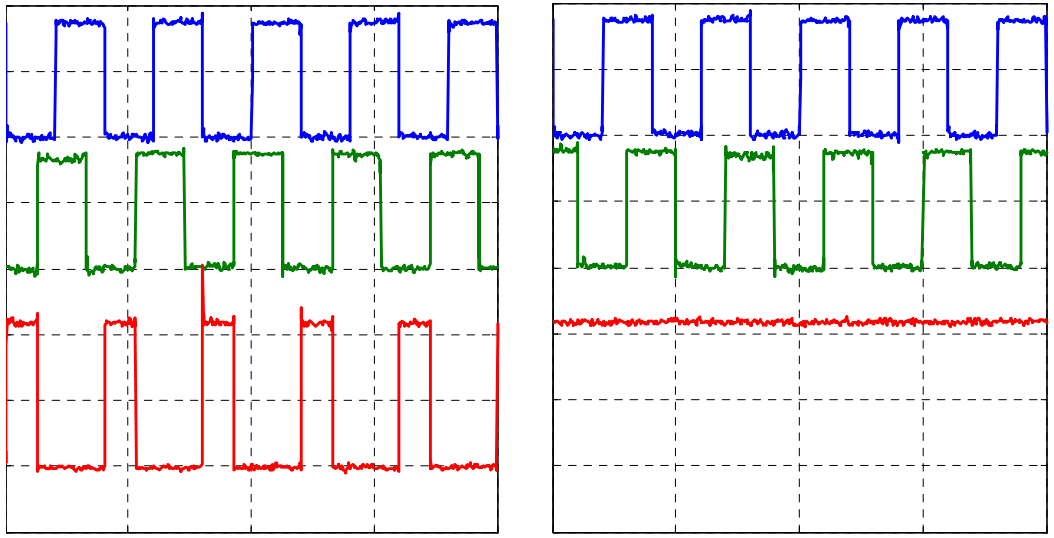
Vdd:1.8V

5bit output

time interval:100ps



Measurement Results



Start

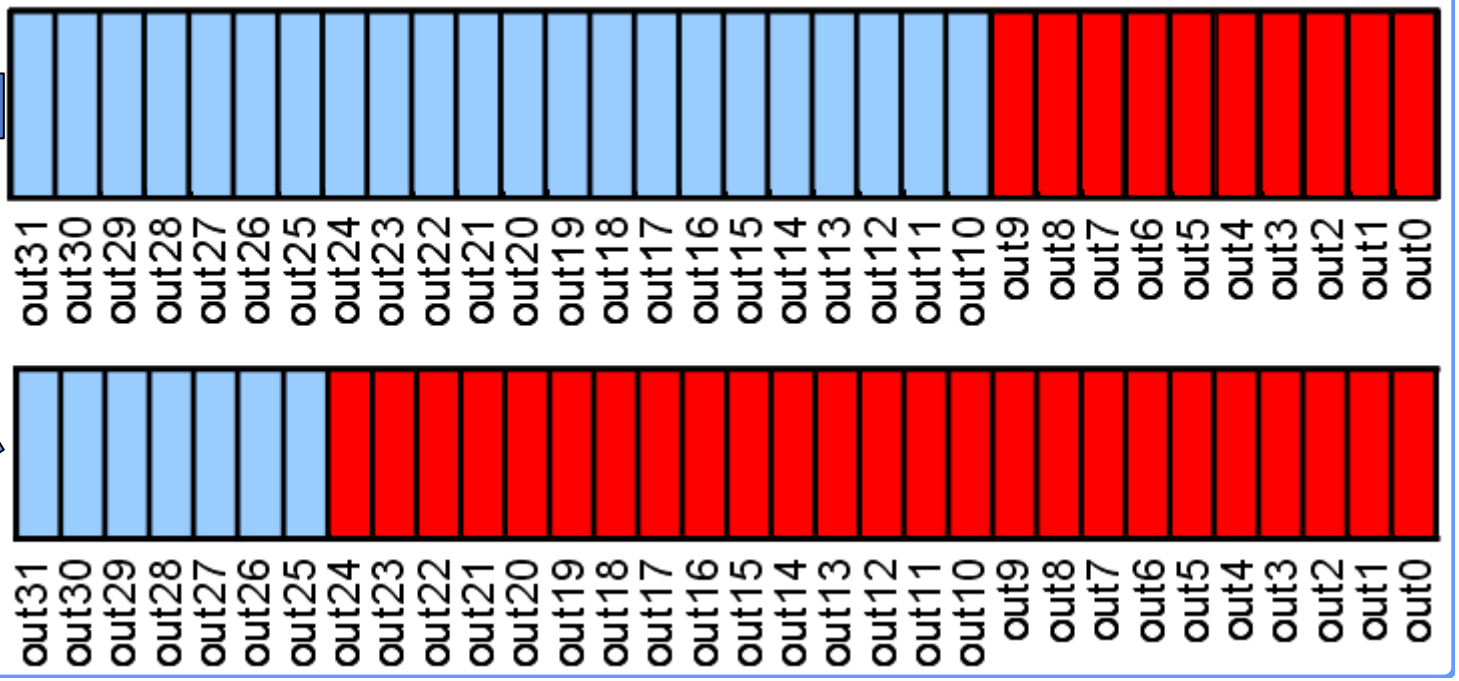
Stop

DFF out

DFF Teg measurement

Whole TDC measurement

+2n sec



output Low

output High

Conclusion

- We have proposed a TDC architecture with small circuitry.
- We have designed and laid out a prototype TDC.
- We have measured the prototype TDC

⇒ Its principle is confirmed.