A Low-Power FPGA Based on Autonomous Fine-Grain Power-Gating

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Background

Reconfigurable VLSIs: FPGA, etc.

Users can program the function on FPGAs without fabrication but FPGAs have a complex structure to achieve programmability.

Advantages
- Low cost for small volume products
- Short time-to-market

Disadvantage
- Larger power consumption than ASICs about 10 times
Proposed asynchronous FPGA

1. Reduction of the dynamic power
   - Lowest power asynchronous encoding (LEDR encoding) to eliminate the power in the clock network

2. Reduction of the static power
   - Autonomous fine-grain power gating with small overheads at the control circuit
     (Area overhead 13%)

   Power reduction:
   - dynamic: 48%, static: 41%
   - (Utilization: 15%)

Process: 90nm CMOS
Cell size: 34um x 31um
Power-gating in synchronous architecture

Activity detecting is necessary

Large hardware of the sleep controller
Difficult to use fine-grain power-gating
Activity detection in an asynchronous circuit

Phase_in = Phase_out \rightarrow LB is un-used
Phase_in =! Phase_out \rightarrow LB is used

Simple hardware for activity detection
Autonomous fine-grain power-gating

Problem of power-gating

Large time for waking up the sleeping circuit

Data arrive at the previous cells

Sleep

Power: OFF

Data don’t come during the waiting time

Stand-by

Power: ON

Operation completion

Active

Power: ON

Data arrival

Data

Logic block1

Active

Logic block2

Stand-by

Data-arrival

Data

Logic block1

Stand-by

Logic block2

Active
Evaluation in a 45nm process

- LEDR with power-gating
- LEDR without power-gating
- Sync. without power-gating

- Utilization [%]
- Power/cell [uW]

41% reduced
60% reduced
56% reduced