1D-16: A 52-mW 8.29mm² 19-mode LDPC Decoder Chip for Mobile WiMAX Applications


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Motivation

- First introduced by Gallager in 1962. [1]
- Rediscovered by MacKay in 1995. [2]:
  - Excellent error-correcting performance near the Shannon limit.
  - Highly parallel decoding scheme.
- Become more popular in advanced communication systems (Mobile WiMAX) with advanced VLSI technology.
Low-Density Parity-Check Codes (LDPC)

- Parity check matrix: very sparse matrix

\[
H = \begin{bmatrix}
1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 \\
0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 \\
0 & 1 & 0 & 0 & 0 & 1 & 1 & 0 & 0 \\
0 & 0 & 1 & 1 & 0 & 0 & 0 & 1 & 0
\end{bmatrix}
\]

- Bipartite graph

Bit nodes (columns):

Check nodes (rows):

C1, C2, C3, C4, C5, C6
Proposed Design Techniques

- Overlapped Operations of BNUs & CNUs
- New Early Termination Scheme
- Distributed Memory Banks
- Reconfigurable Architecture

CU: Counter Unit
AGU: Address Generator Unit
Efficient Checkerboard Layout Scheme (ECLS)

- Divided memory bank (architecture)
  - Activation of memory bank in need
  - Small address decoder inside memory
  - Reduced power

- Distributed memory bank (physical)
  - Evenly data transmission
  - Lower routing complexity
  - Reduced area
## Comparison Table

<table>
<thead>
<tr>
<th></th>
<th>JSSC’02</th>
<th>ISCAS’05</th>
<th>TCAS-I’06</th>
<th>JSSC’06</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multi-mode</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>7 modes</td>
<td>19 modes</td>
</tr>
<tr>
<td>Spec</td>
<td>(1024,512)</td>
<td>(2048,1732)</td>
<td>(1024,512)</td>
<td>(2048,128*k)</td>
<td>(96<em>k, 48</em>k)</td>
</tr>
<tr>
<td></td>
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</tr>
<tr>
<td>Code Construction</td>
<td>Random</td>
<td>RS-based</td>
<td>QC-based</td>
<td>Turbo-Interleaved</td>
<td>QC-based</td>
</tr>
<tr>
<td>Technology</td>
<td>0.16um</td>
<td>0.18um</td>
<td>0.18um</td>
<td>0.18um</td>
<td>0.13um</td>
</tr>
<tr>
<td>Parallelism</td>
<td>Fully</td>
<td>Fully</td>
<td>Partial</td>
<td>Partial</td>
<td>Partial</td>
</tr>
<tr>
<td>Iterations</td>
<td>64</td>
<td>32</td>
<td>8</td>
<td>16</td>
<td>2 ~ 8</td>
</tr>
<tr>
<td>Chip Area</td>
<td>52.5 mm²</td>
<td>17.64 mm²</td>
<td>10.08 mm²</td>
<td>14.3 mm²</td>
<td>8.29 mm²</td>
</tr>
<tr>
<td>Frequency</td>
<td>64 MHz</td>
<td>100 MHz</td>
<td>200 MHz</td>
<td>125 MHz</td>
<td>83.3 MHz</td>
</tr>
<tr>
<td>Throughput</td>
<td>1 Gbps</td>
<td>3.2 Gbps</td>
<td>985 Mbps</td>
<td>640 Mbps</td>
<td>30~111 Mbps</td>
</tr>
<tr>
<td>Power</td>
<td>690 mW</td>
<td>N/A</td>
<td>N/A</td>
<td>787 mW</td>
<td>52 mW</td>
</tr>
</tbody>
</table>

*This work* spec: 
- (1024,512) \(k = 6\sim24\)
- (96*k, 48*k) \(k = 6\sim24\)
- (2048,128*k) \(k = 8\sim14\)
- \((2048,1732)\)
- \((1024,512)\)
- \((1024,512)\)
- \((1024,512)\)
- \((1024,512)\)
- \((1024,512)\)
Conclusion

- An efficient IC strategy with four design techniques and efficient checkerboard layout scheme (ECLS).

- Features of our LDPC decoder design:
  - Multi-mode design (19-mode)
  - Smaller chip area (8.29mm\(^2\))
  - Higher hardware utilization (50% → 75%)
  - Lower decoding latency (68.75%)
  - Flexible decoding throughput (30Mbps~111Mbps)
  - Lower power consumption (52mW @ 83.3 MHz)