1D-16 : A 52-mW 8.29mm^2 19-mode LDPC Decoder Chip for Mobile WiMAX Applications

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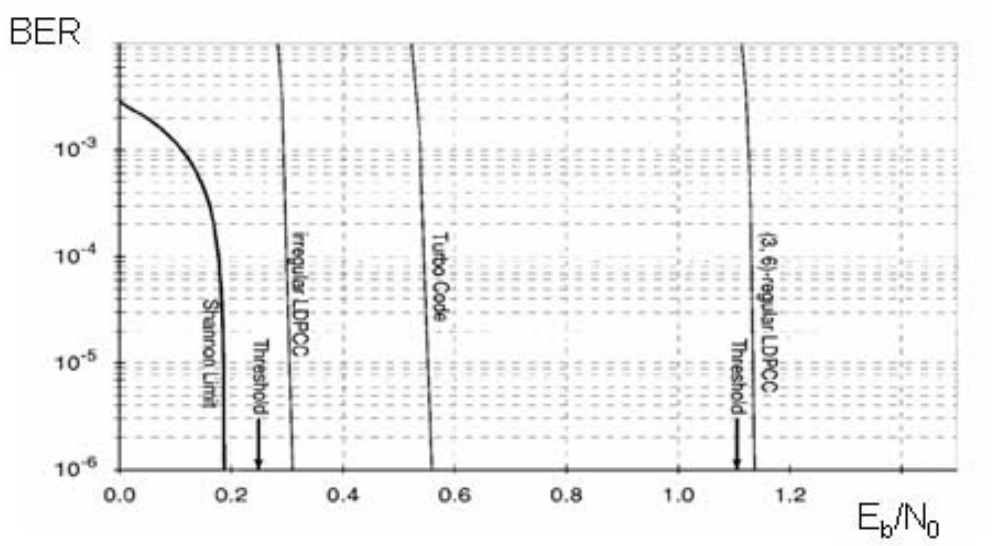
Jan. 20th, 2009

Motivation

- First introduced by Gallager in 1962. [1]
- Rediscovered by MacKay In 1995. [2] :
  - Excellent error-correcting performance near the Shannon limit.
  - Highly parallel decoding scheme.
- Become more popular in advanced communication systems (Mobile WiMAX) with advanced VLSI technology.

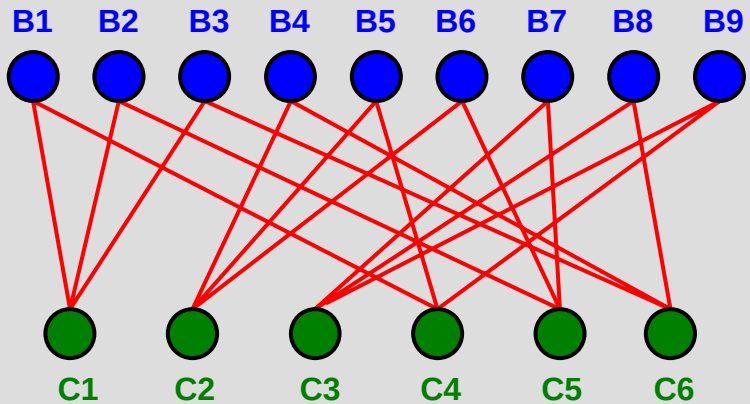


Low-Density Parity-Check Codes (LDPC)

- Parity check matrix : very sparse matrix

$$H = \begin{array}{c} \begin{matrix} B1 & B2 & B3 & B4 & B5 & B6 & B7 & B8 & B9 \end{matrix} \\ \begin{bmatrix} 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 \\ 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 \\ 0 & 1 & 0 & 0 & 0 & 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 & 0 & 0 & 0 & 1 & 0 \end{bmatrix} \end{array} \begin{matrix} C1 \\ C2 \\ C3 \\ C4 \\ C5 \\ C6 \end{matrix}$$

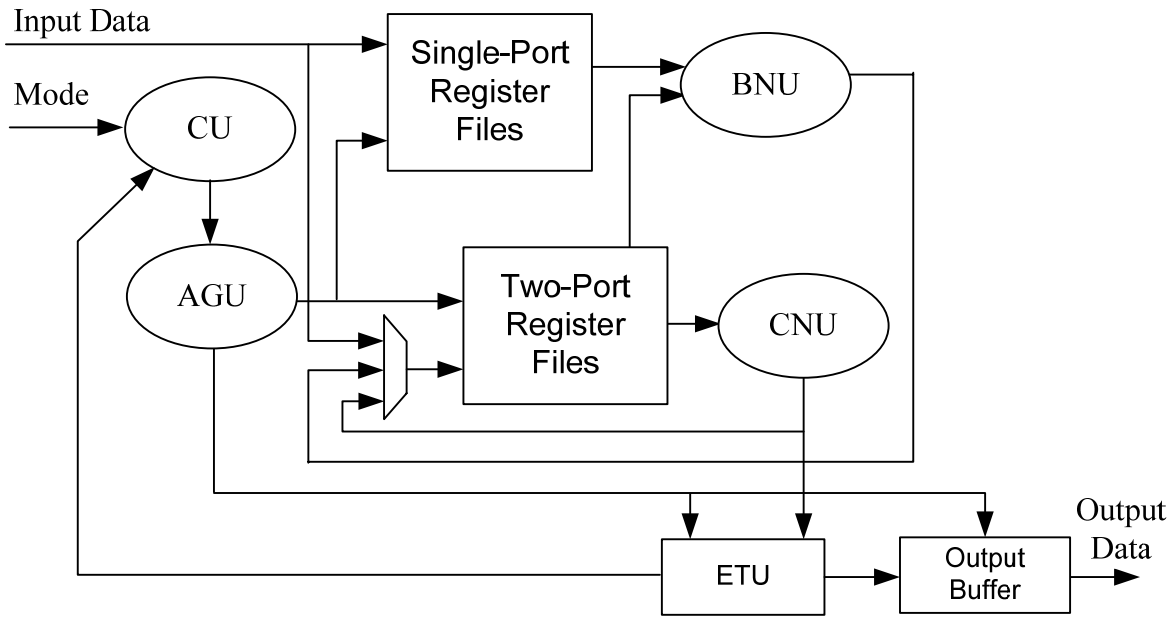
- Bipartite graph



Proposed Design Techniques

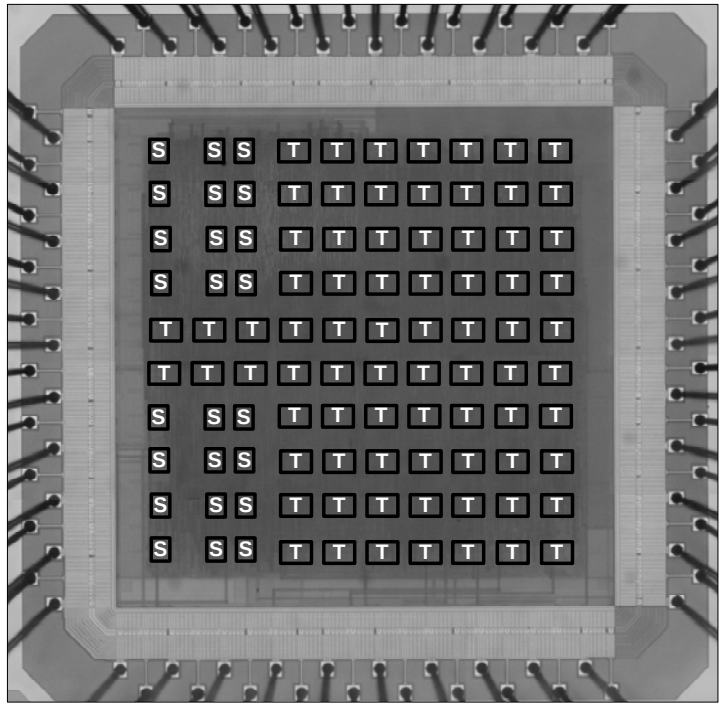
- Overlapped Operations of BNUs & CNUs
- New Early Termination Scheme
- Distributed Memory Banks
- Reconfigurable Architecture

CU : Counter Unit
AGU : Address Generator Unit



Efficient Checkerboard Layout Scheme (ECLS)

- Divided memory bank (architecture)
  - Activation of memory bank in need
  - Small address decoder inside memory
  - Reduced power
- Distributed memory bank (physical)
  - Evenly data transmission
  - Lower routing complexity
  - Reduced area



Comparison Table

	JSSC'02	ISCAS'05	TCAS-I'06	JSSC'06	**This work**
Multi-mode	No	No	No	7 modes	**19 modes**
Spec	(1024,512)	(2048,1732)	(1024,512)	(2048,128*k) k = 8~14	**(96*k, 48*k) k = 6~24**
Code Construction	Random	RS-based	QC-based	Turbo-Interleaved	**QC-based**
Technology	0.16um	0.18um	0.18um	0.18um	**0.13um**
Parallelism	Fully	Fully	Partial	Partial	**Partial**
Iterations	64	32	8	16	**2 ~ 8**
Chip Area	52.5 mm^2	17.64 mm^2	10.08 mm^2	14.3 mm^2	**8.29 mm^2**
Frequency	64 MHz	100 MHz	200 MHz	125 MHz	**83.3 MHz**
Throughput	1 Gbps	3.2 Gbps	985 Mbps	640 Mbps	**30~111 Mbps**
Power	690 mW	N/A	N/A	787 mW	**52 mW**

Conclusion

- An efficient IC strategy with four design techniques and efficient checkerboard layout scheme (ECLS).
- Features of our LDPC decoder design :
  - Multi-mode design (19-mode)
  - Smaller chip area (8.29mm^2)
  - Higher hardware utilization (50%→75%)
  - Lower decoding latency (68.75%)
  - Flexible decoding throughput (30Mbps~111Mbps)
  - Lower power consumption (52mW @ 83.3 MHz)