A Full-Synthesizable High-Precision Built-In Delay Time Measurement Circuit

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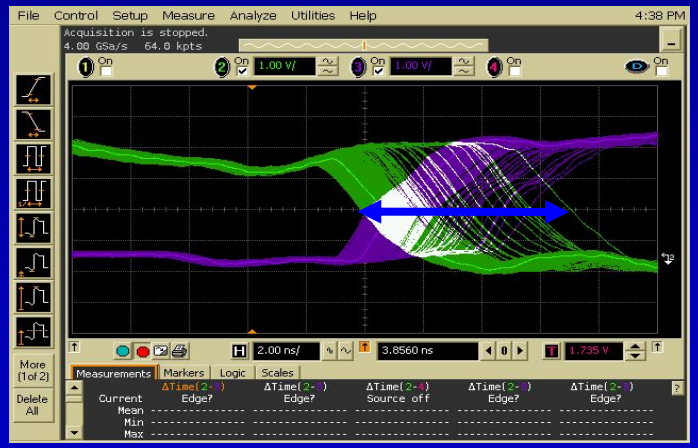
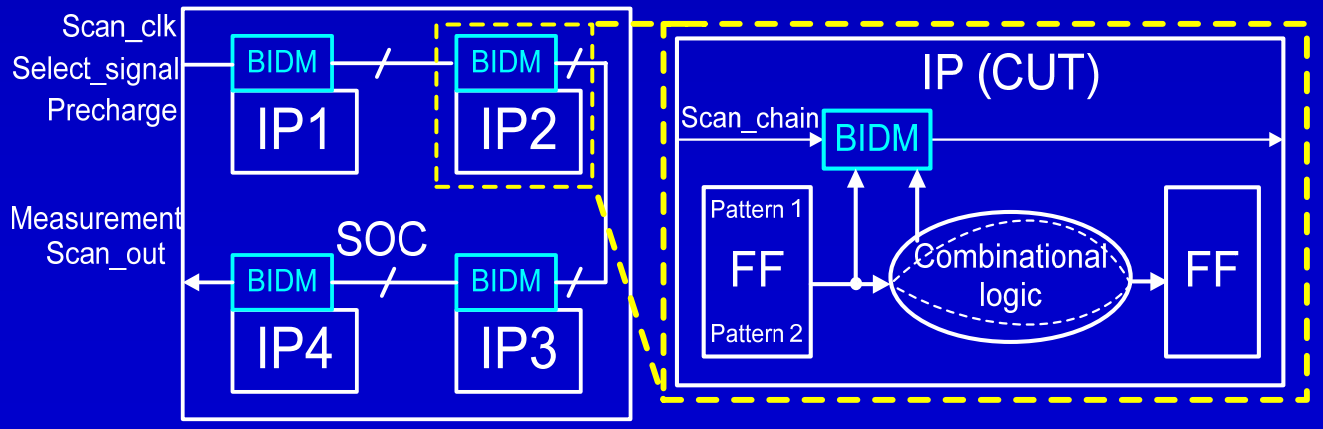
Introduction

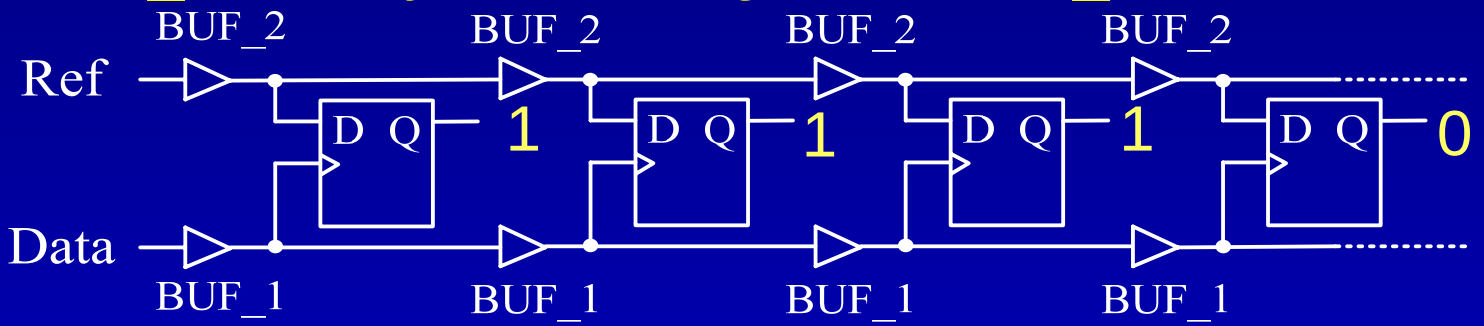
- The accuracy delay testing and internal chip small delay defects debugging have become major issues for manufacturing advanced System on a Chip.

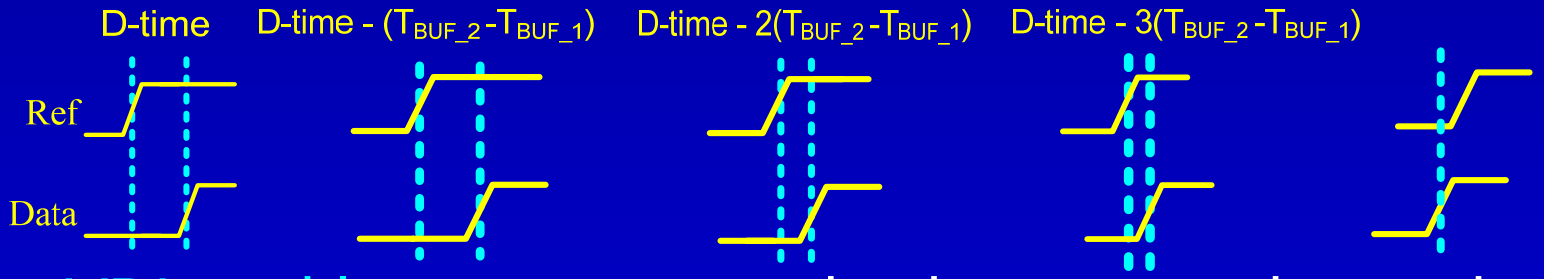




The Vernier Delay Line Circuit

- The VDL circuit transforms the two signals' timing difference into digital format, which can be recorded into DFF.
  - BUF_2's delay time is larger the BUF_1's



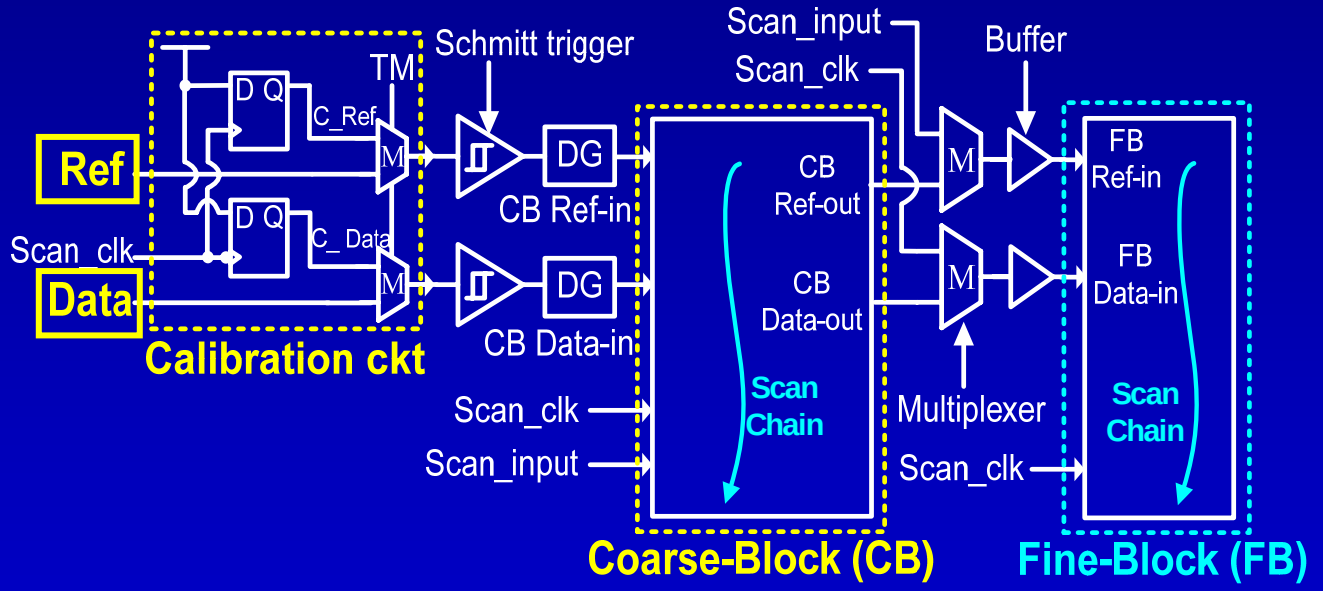


Long VDL problem: not easy maintain accuracy by synthesized design, large area overhead

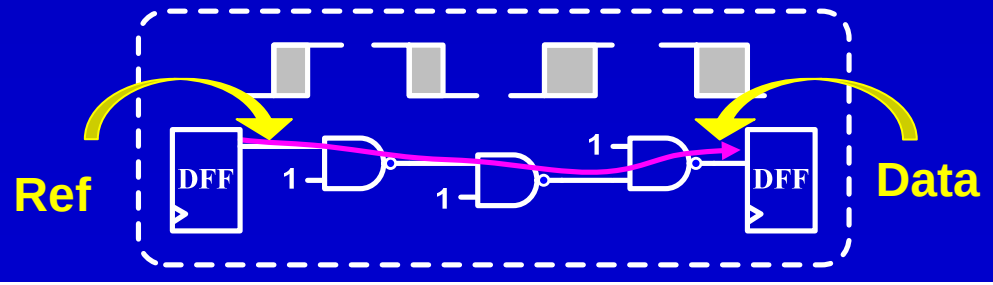
Nxx	n01	n02	n03	n04	n05	n06	n07	n08	n09	n10	n11	n12
Range	**21ps**	19ps	19ps	19ps	**26ps**	19ps	18ps	**14ps**	18ps	20ps	24ps	19ps
Nxx	n13	n14	n15	n16	n17	n18	n19	n20	n21	n22	n23	Avg
Range	17ps	**15ps**	18ps	**24ps**	23ps	18ps	15ps	16ps	18ps	29ps	22ps	19.6ps

The BIDM Circuit Design

- The BIDM's architecture is divided into Coarse-Block (CB) and Fine-Block (FB).
- 2 tens digits for FB, 3 tens digits for CB.

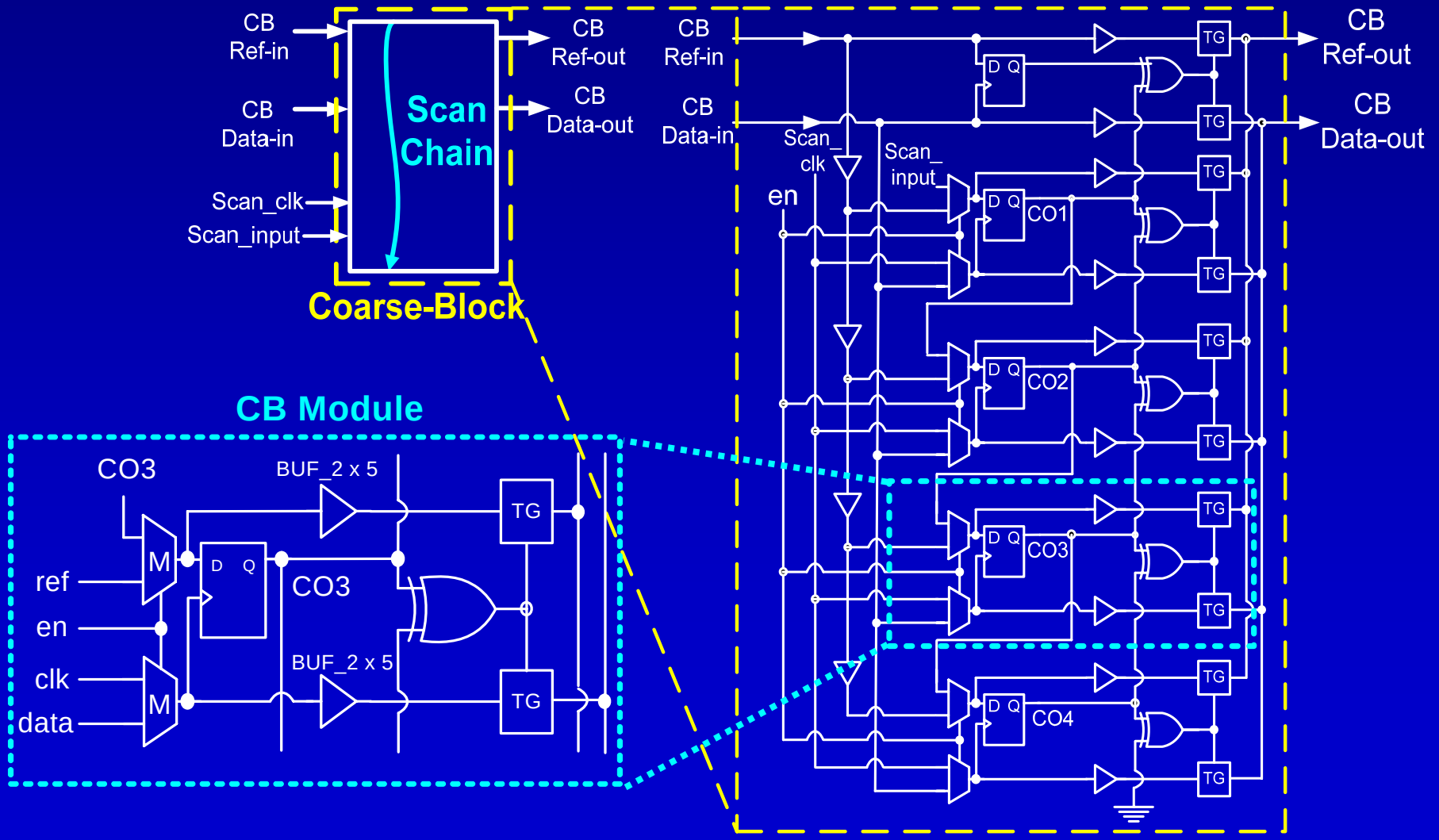


- D-time:Data-Ref, D-range: MaxD-time - MinD-time



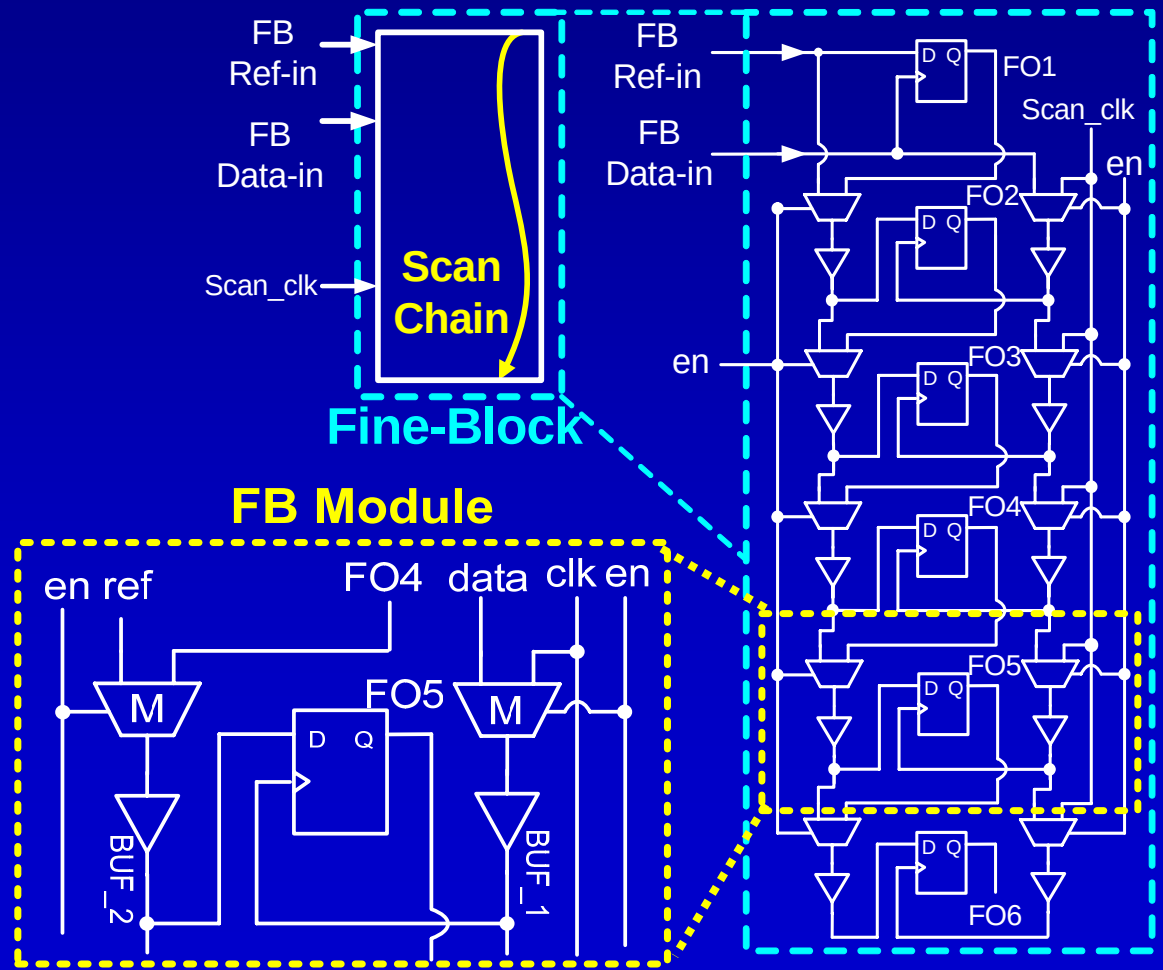
The BIDM Coarse Block Circuit Design

- The average D-range is 130ps for CB outputs.



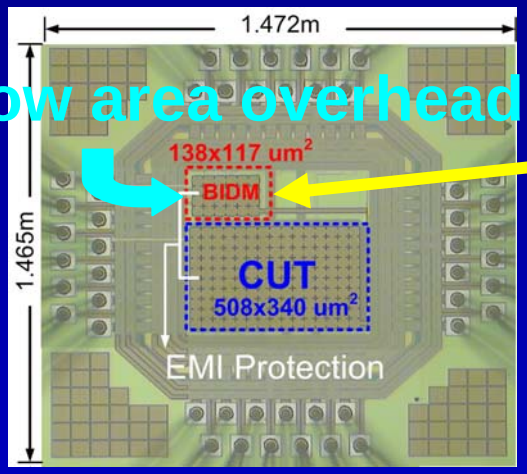
The BIDM Fine Block Circuit Design

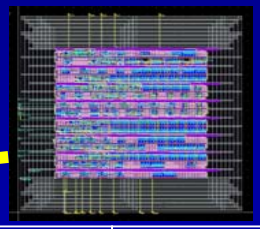
- The average D-range is 21.35ps for FB outputs.



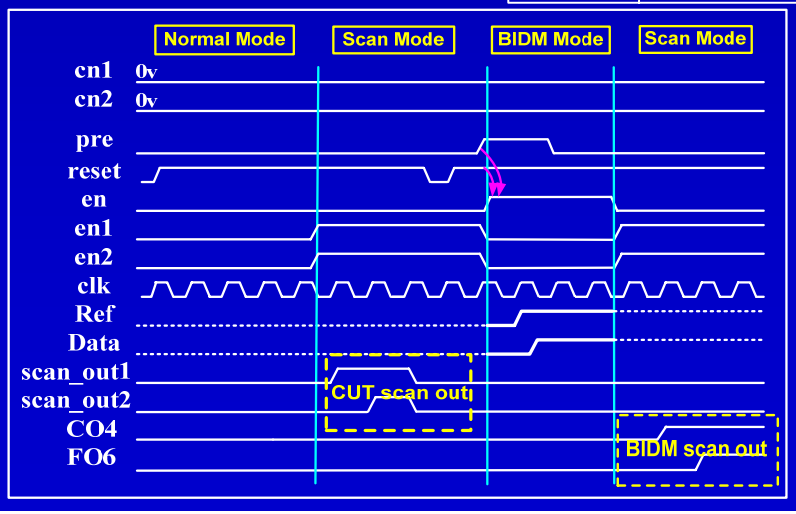
Test Chip Implementation

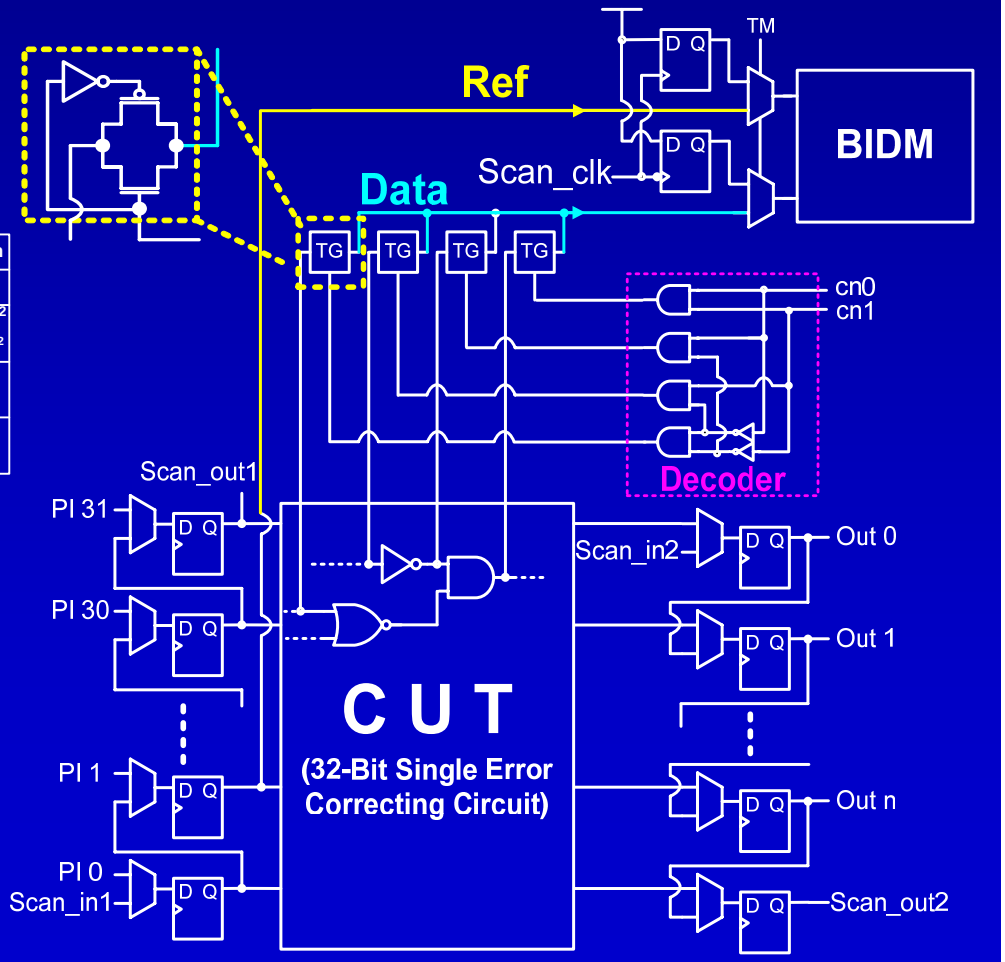
- The integrated circuit of CUT with BIDM
  - The integrated chip was implemented by a cell-based design flow using TSMC 0.18um technology.





Process	TSMC 1P6M 0.18um
Package	48 S/B
Chip area	1.472x1.465 mm² BIDM: 1.38x117 um²
Transistor count	7938 BIDM: 1118
Max. Power	5.216mW BIDM: 1.807mW



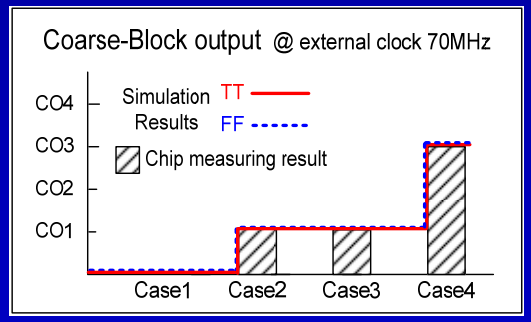


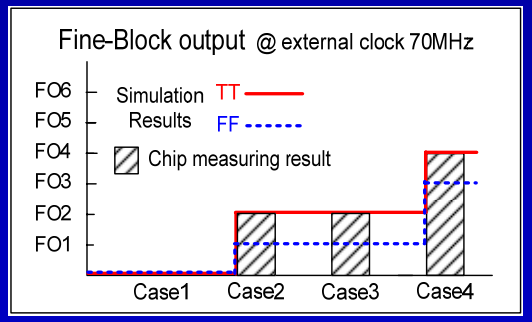
Chip Validation Results

- The integrated circuit postlayout simulation results

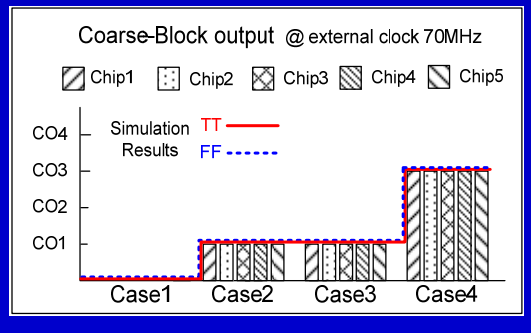
Case/Model	Case1			Case2			Case3			Case4		
	FF	TT	SS	FF	TT	SS	FF	TT	SS	FF	TT	SS
Ref (ps)	11711	**11891**	Fail	11712	**11885**	Fail	11712	**11885**	0	11711	**11885**	Fail
Data (ps)	11662	**11849**	12279	11837	**12063**	12551	11843	**12066**	12583	12068	**12346**	Fail
D-time (ps)	-49	**- 42**	w/o	125	**178**	w/o	131	**181**	w/o	357	**461**	w/o

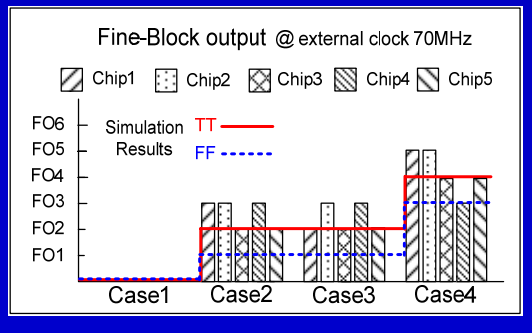
- Chip measuring result of four TestCases





- The measuring results from five chips

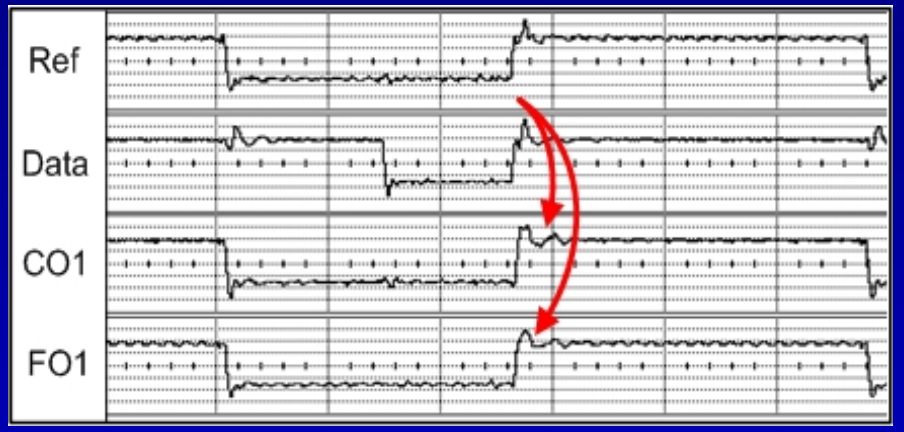




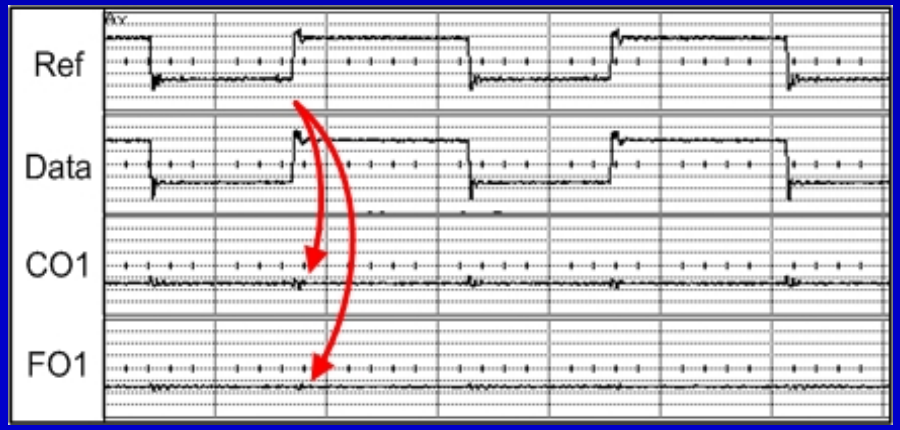
Oscillator Scope's Measurements

- The scope measurement waveforms of chips

(a) The correct scan output from FO1 to FO6 stage.



(b) The CO1 and FO1 correct response.



(c) Ref signal slower than Data signal

(d) The control signals timing diagram.