A Dynamic Quality-Scalable H.264 Video Encoder Chip

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Introduction: Design Specification

- Dynamic quality scalability
  - Tradeoff: Quality & Working Frequency (Power)
  - Flexibility for different applications
  - Dynamically mode configuration
    4 encoding modes (QS0, QS1, QS2, QS3)

- Support versatile video resolutions
  - From QCIF to HD720

For network transmission
- Constant and stable bit-rate
- HW BU-based Rate Control

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.13µm 1P8M CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip Size</td>
<td>4.9 x 4.9 mm²</td>
</tr>
<tr>
<td>Gate-Count</td>
<td>470K</td>
</tr>
<tr>
<td>On-Chip Memory</td>
<td>13.3K Bytes (SRAM)</td>
</tr>
<tr>
<td>Package</td>
<td>160CQFP</td>
</tr>
</tbody>
</table>
Proposed Design: System Architecture

- RISC
- Video In
- Memory Controller
- Video Frame Buffer

AHB Bus Interface

PDSB Controller
- Intra Upper Pels SRAM
- Upper MB Encoding Info. SRAM
- ILF Upper Pels SRAM
- Bitstream Buffer

Quality Scalable H.264 Video Encoder

- System Controller (Quality Scalable Control)
- Rate Control Unit (Basic Unit Pipeline)
- Encoding Info. Reg.
- Motion Estimation
  - Luma SRAM
  - Integer ME
  - Fractional ME
  - Best MV SRAM
- AHB Bus Interface
- System Memory Arbiter

Intra Coding
- Luma/Chroma SRAM
- Best Mode Reg.
- Residual SRAM

In-Loop Filter
- MB Pel. SRAM
- Reconstruct SRAM
- Residual SRAM

Entropy Coding
- Bitstream Buffer

MB Pipeline Stage 1
MB Pipeline Stage 2
MB Pipeline Stage 3
MB Pipeline Stage 4

Modules providing scalable video quality
Proposed Techniques:
Quality Scalable Algorithms

1. **Down Sample (X,Y)**
   - Scalable down sample rate: 1~5
   - Calculate Cost

2. **Find Best Candidate**
   - Scalable candidate number: 1~4
   - Calculate Cost

3. **Local Full Search Around Candidate(s)**
   - Scalable local full search range: 1~7
   - Calculate Cost

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**Fractionsal ME Algorithm**

<table>
<thead>
<tr>
<th>Quality Mode</th>
<th>HDLFS-IME (DSR, CN, LFSR)</th>
<th>CS-FME</th>
<th>Intra Coding</th>
</tr>
</thead>
<tbody>
<tr>
<td>QS0</td>
<td>(5,4,3)</td>
<td>Cluster 1 + Cluster 2</td>
<td>Full-SA</td>
</tr>
<tr>
<td>QS1</td>
<td>(4,3,2)</td>
<td>Cluster 1 + Cluster 2</td>
<td>Full-SA</td>
</tr>
<tr>
<td>QS2</td>
<td>(5,2,2)</td>
<td>Cluster 1</td>
<td>CC-SA + QMB-SA</td>
</tr>
<tr>
<td>QS3</td>
<td>(5,1,2)</td>
<td>Cluster 1</td>
<td>PCC-SA + QMB-SA</td>
</tr>
</tbody>
</table>

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**Intra Algorithm**

<table>
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<tr>
<th>Mode</th>
<th>CS-FME</th>
<th>Intra Coding</th>
</tr>
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<tr>
<td></td>
<td></td>
<td>Full-SA</td>
</tr>
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<td></td>
<td></td>
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</tr>
<tr>
<td></td>
<td></td>
<td>CC-SA + QMB-SA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PCC-SA + QMB-SA</td>
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</table>
Proposed Techniques: Rate Control Algorithm

4 MB BU-Based Pipelined Rate Control
- 2-stage algorithm
- Lagrange Model Prediction
- Less prediction data are required
- Better Performance

Frame-based Rate Control

BU-based Rate Control (BU=1 MB)
Analysis on Quality-Scalable Modes

Low-power techniques
-- Lower operating frequency at the same resolution
-- Lower voltage

Tradeoff
-- Encoding quality
-- Power consumption

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<tr>
<th>Quality Mode</th>
<th>Average PSNR drop (dB) (compared to JM)</th>
</tr>
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<tbody>
<tr>
<td>QS0</td>
<td>- 0.15 db</td>
</tr>
<tr>
<td>QS1</td>
<td>- 0.16 db</td>
</tr>
<tr>
<td>QS2</td>
<td>- 0.4 db</td>
</tr>
<tr>
<td>QS3</td>
<td>- 0.6 db</td>
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</tbody>
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FPGA & Chip Implementation