

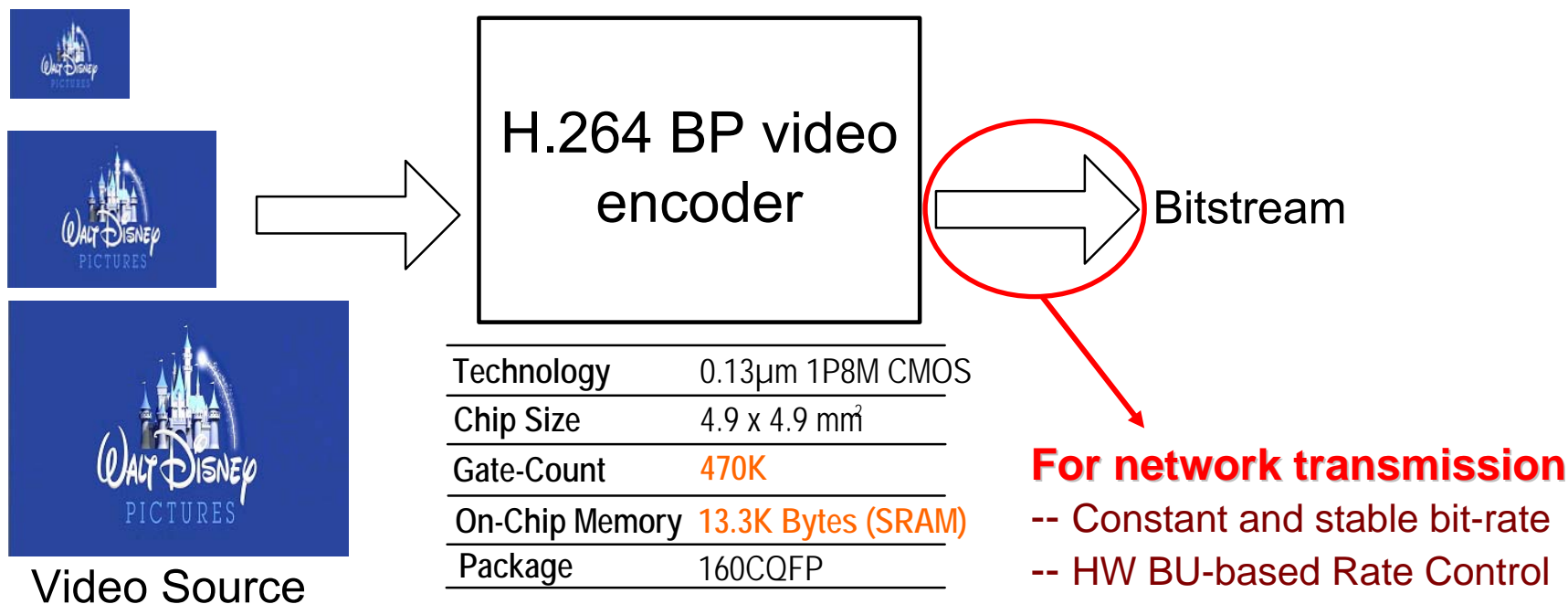
A Dynamic Quality-Scalable H.264 Video Encoder Chip

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Introduction: Design Specification



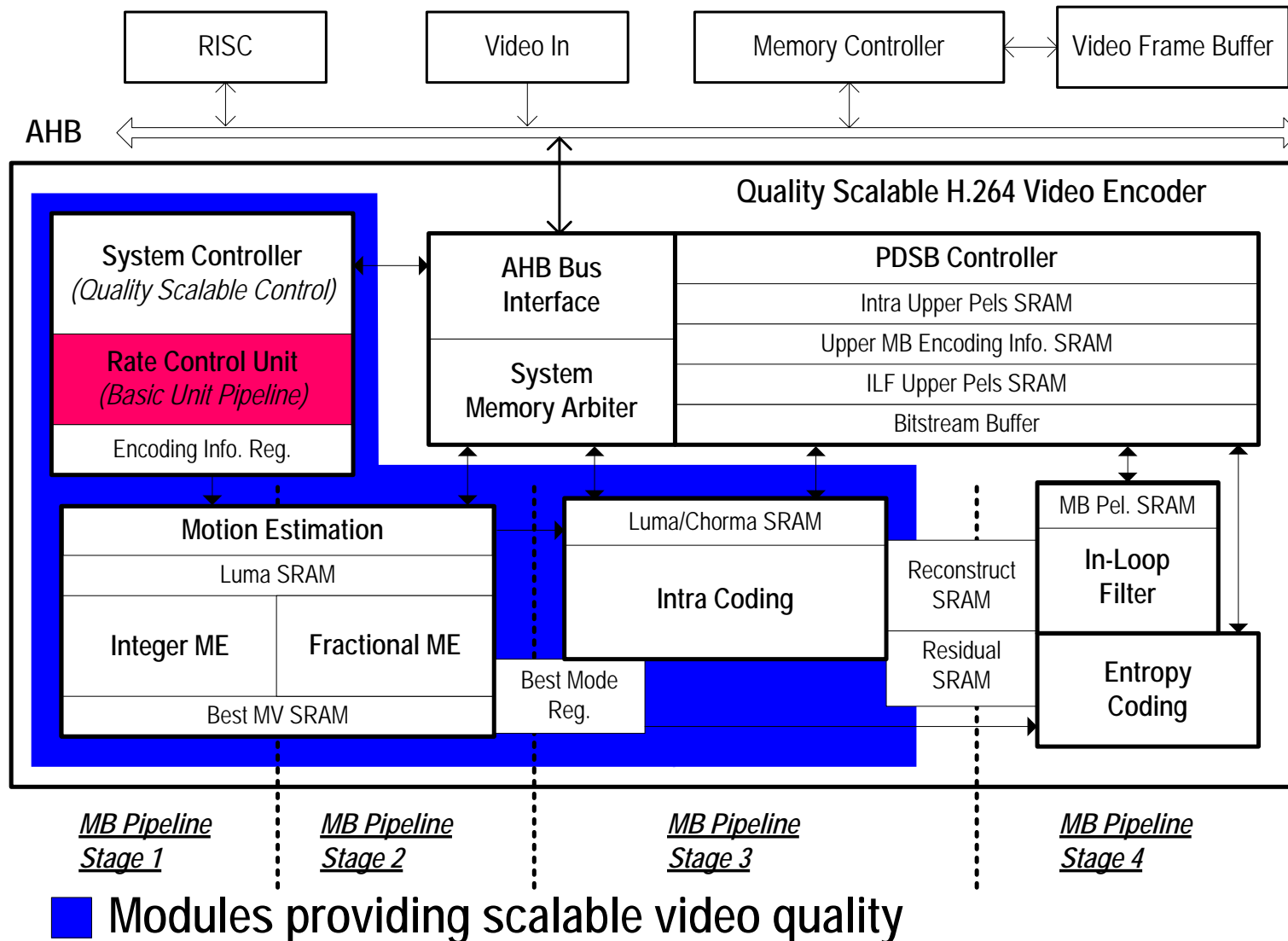
Support versatile video resolutions

-- From QCIF to HD720

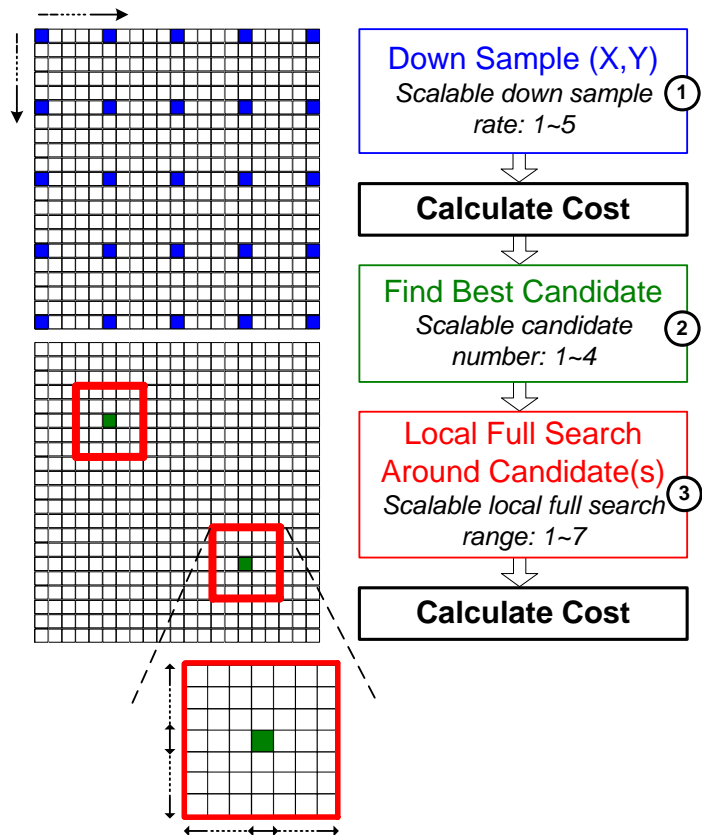
Dynamic quality scalability

- Tradeoff : Quality & Working Frequency (Power)
- Flexibility for different applications
- Dynamically mode configuration
- 4 encoding modes (QS0, QS1, QS2, QS3)

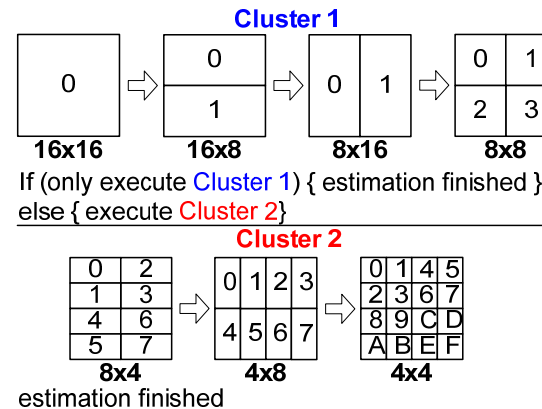
Proposed Design: System Architecture



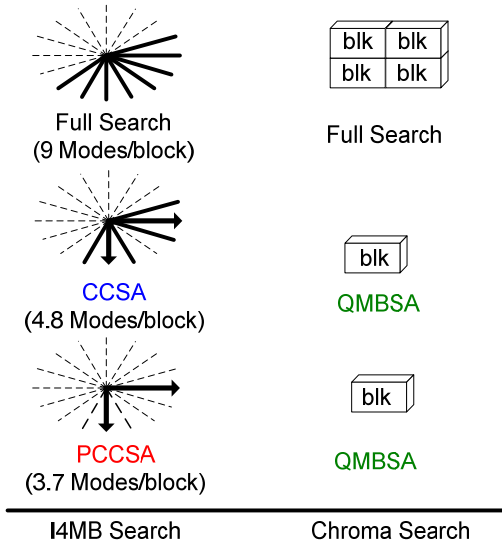
Proposed Techniques: Quality Scalable Algorithms



Integer ME Algorithm



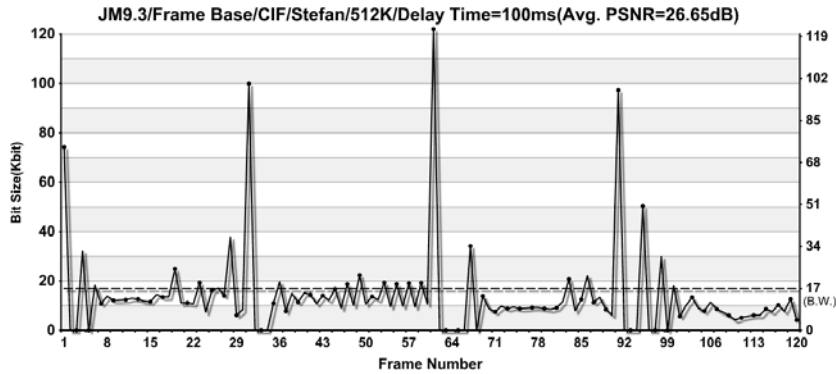
Fractional ME Algorithm



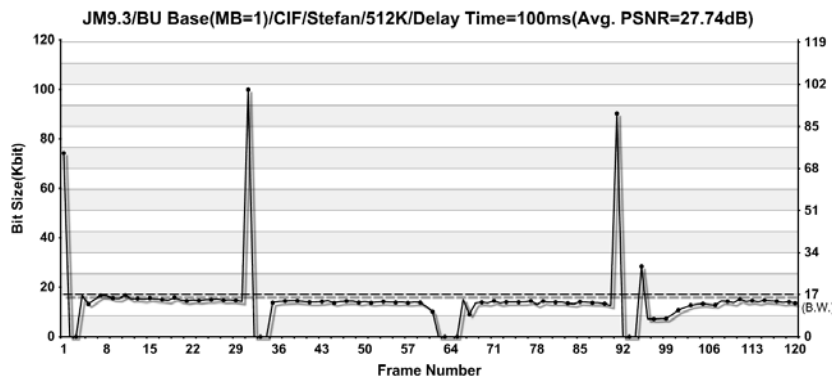
Intra Algorithm

Quality Mode	HDLFS-IME (DSR, CN, LFSR)	CS-FME	Intra Coding
QS0	(5,4,3)	Cluster 1 + Cluster 2	Full-SA
QS1	(4,3,2)	Cluster 1 + Cluster 2	Full-SA
QS2	(5,2,2)	Cluster 1	CC-SA + QMB-SA
QS3	(5,1,2)	Cluster 1	PCC-SA + QMB-SA

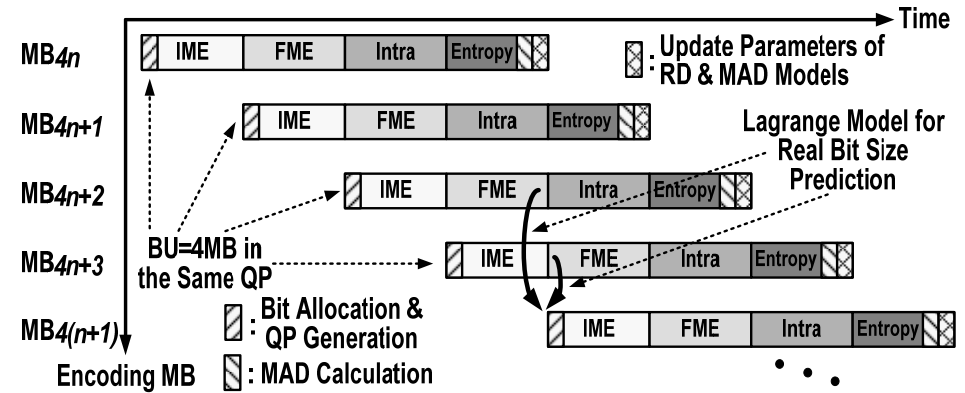
Proposed Techniques: Rate Control Algorithm



Frame-based Rate Control

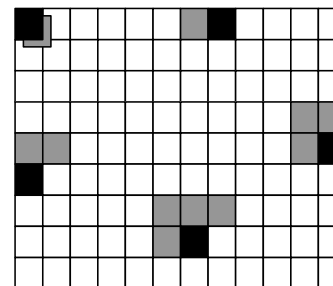


BU-based Rate Control (BU=1MB)



- 4MB BU-Based Pipelined Rate Control
 - 2-stage algorithm
- Lagrange Model Prediction
 - Less prediction data are required
- Better Performance

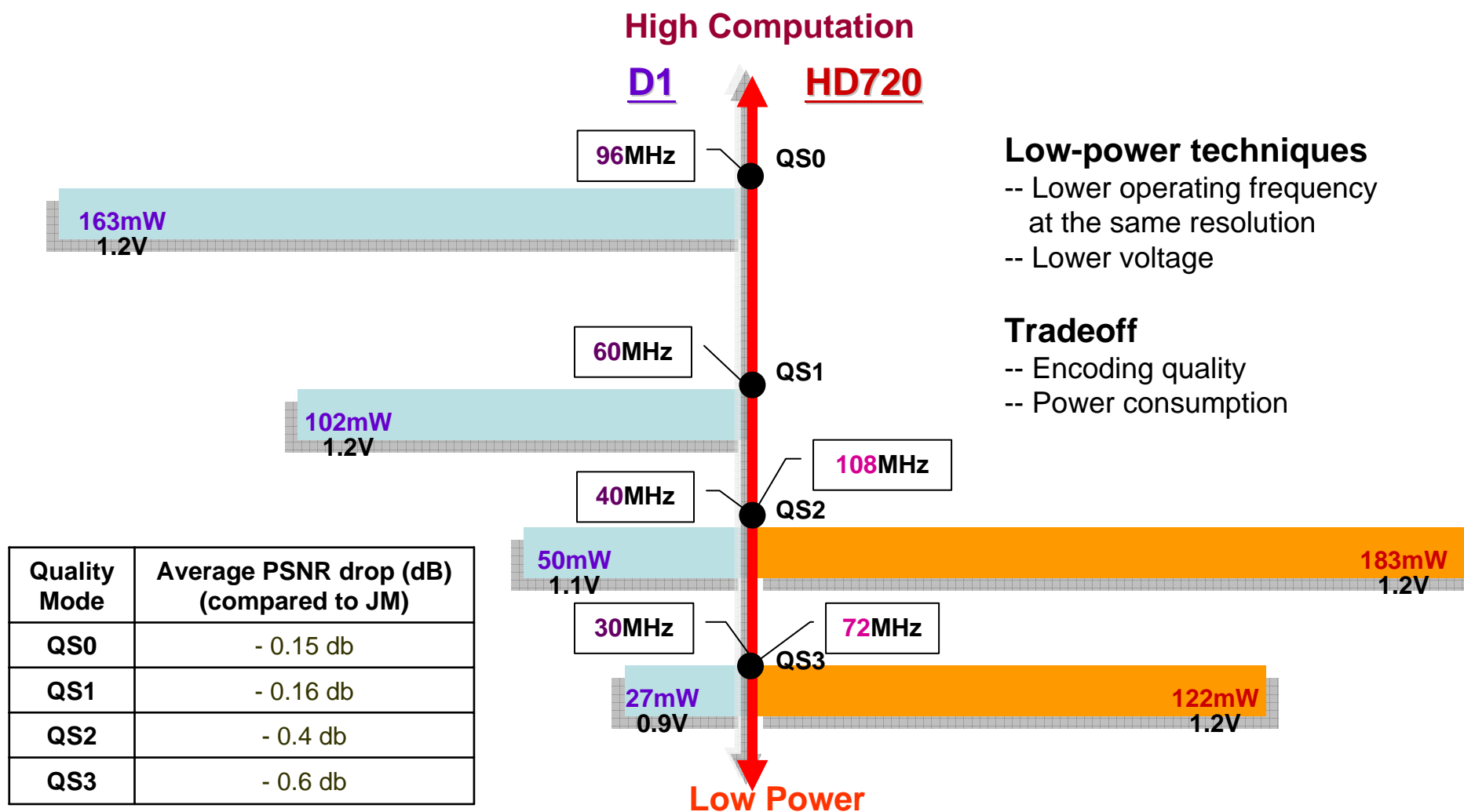
MAD Prediction Pattern



■ : Current BU ■ : Predict-Data BU

Pipelined BU-based vs. Frame-based Improvement	
QCIF	PSNR: +0.826dB
	Skipped Frame: -4.8
CIF	PSNR: +0.31dB
	Skipped Frame: -7.5
D1	PSNR: +1.90dB
	Skipped Frame: -19

Analysis on Quality-Scalable Modes



FPGA & Chip Implementation

