A High Performance LDPC Decoder for IEEE802.11n Standard

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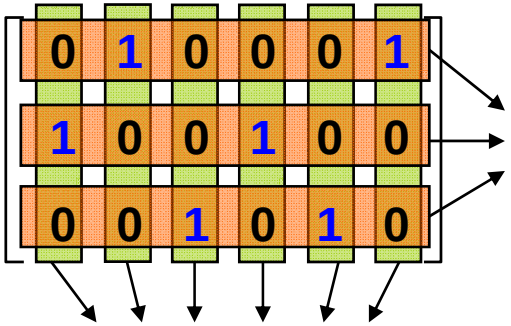
Jan. 20th 2009

LDPC Decoders

Parity Check Matrix

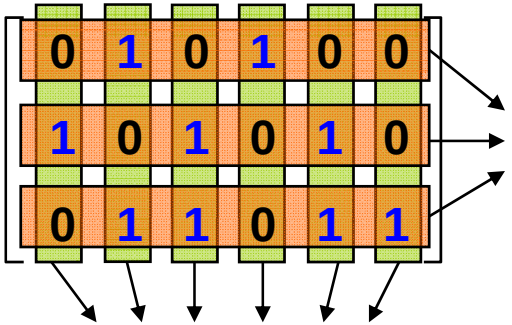
Regular Codes



Same row weight

Same column weight

Irregular Codes

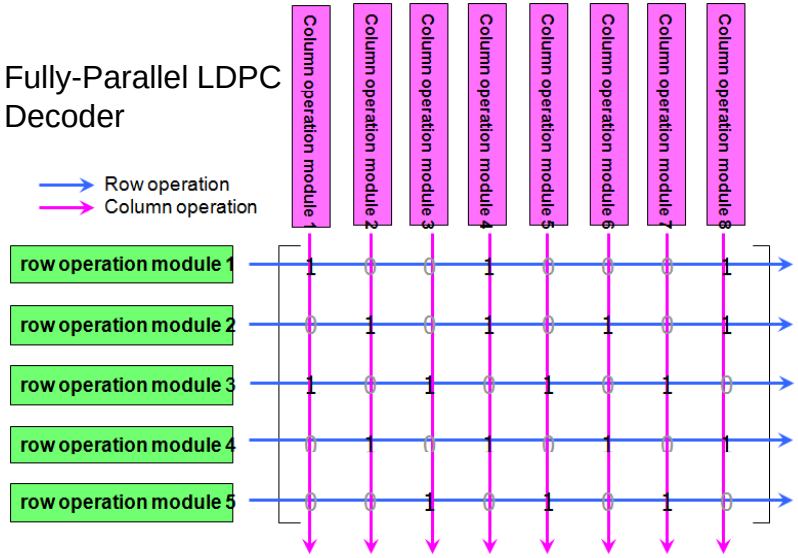


Different row weight

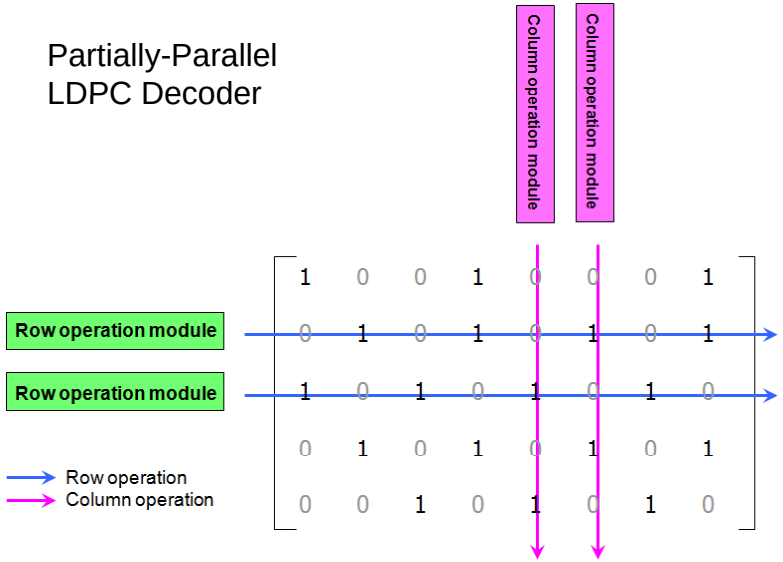
Different column weight

LDPC Decoders

Fully-Parallel LDPC Decoder



Partially-Parallel LDPC Decoder



Message Passing Algorithm

Start: Give all the places labeled '1' message alpha and beta.

Initial: $\beta_{mn} = \lambda_n = \frac{2y_n}{\sigma^2}$

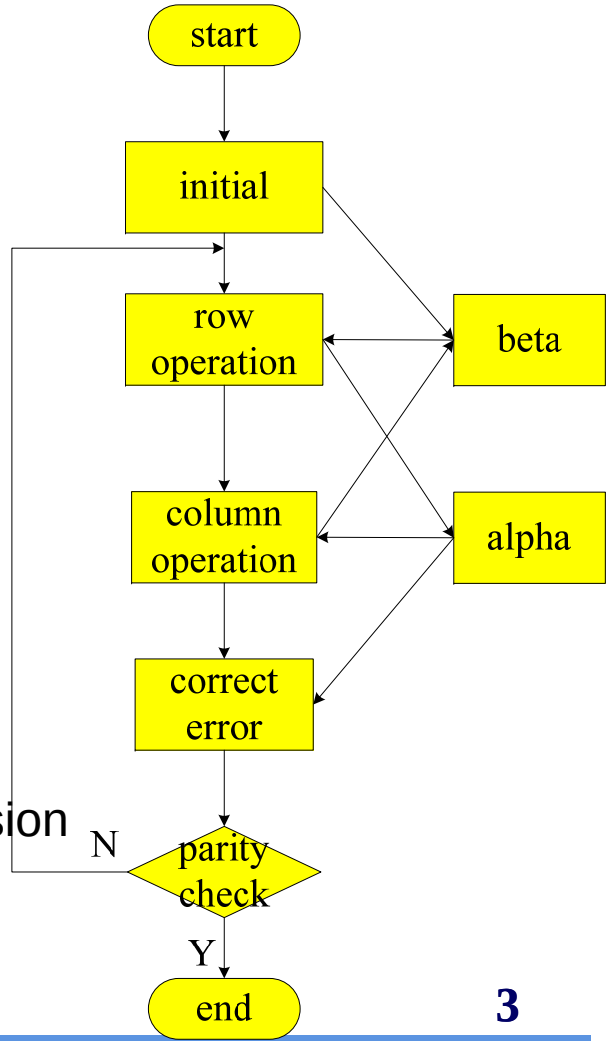
Row Operation: $\alpha_{mn} = \left(\prod_{n' \in A(m)\backslash n} \operatorname{sign}(\beta_{mn'})\right) \times \min_{n' \in A(m)\backslash n} |\beta_{mn'}|$

Column Operation: $\beta_{mn} = \lambda_n + \sum_{m' \in B(n)\backslash m} \alpha_{m'n}$

Error Correction: $\hat{y}_n = \begin{cases} 0, sign(\lambda_n + \sum_{m' \in B(n)} \alpha_{m'n}) = 1 \\ 1, sign(\lambda_n + \sum_{m' \in B(n)} \alpha_{m'n}) = -1 \end{cases}$

Parity Check: Parity check matrix × Tentative Decision

$\begin{cases} = 0 & \text{No error} \\ \neq 0 & \text{Error} \end{cases}$



Example of SDMP Algorithm

Traditional MP algorithm

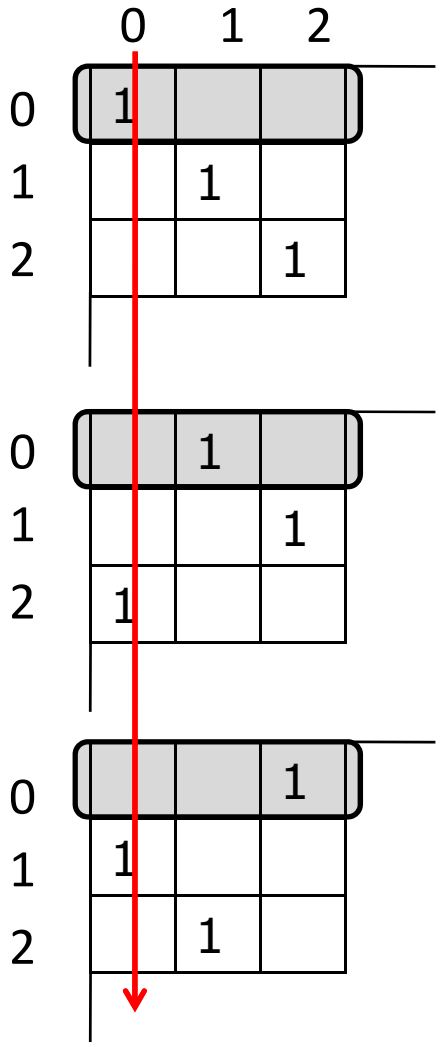
$$\beta_1(0,0) = \lambda(0) + \alpha_2(2,0) + \alpha_3(1,0)$$
$$\beta_2(2,0) = \lambda(0) + \alpha_1(0,0) + \alpha_3(1,0)$$
$$\beta_3(1,0) = \lambda(0) + \alpha_1(0,0) + \alpha_2(2,0)$$

DVMP algorithm in [5]

$$\beta_1'(0,0) = \beta_1(0,0)$$
$$\beta_2'(2,0) = \beta_2(2,0) + \Delta\alpha_1(0,0);$$
$$\beta_3'(1,0) = \beta_3(1,0) + \Delta\alpha_1(0,0);$$

SDMP algorithm

$$sum(0) = \lambda(0) + \alpha_1(0,0) + \alpha_2(2,0) + \alpha_3(1,0)$$
$$sum'(0) = sum(0) + \Delta\alpha_1(0,0)$$
$$\beta_1'(0,0) = sum'(0) - \alpha_1(0,0)$$
$$\beta_2'(2,0) = sum'(0) - \alpha_2(2,0)$$
$$\beta_3'(1,0) = sum'(0) - \alpha_3(1,0)$$



[5] W. Ji, X. Li, T. Ikenaga, and S. Goto, "High Throughput Partially-Parallel Irregular LDPC Decoder Based on Delta-Value Message Passing Schedule ", *VLSI Design, Automation and Test*, April, 2008

Flowchart for SDMP Algorithm

Row Operation

$$\beta(m,n) = sum(n) - \alpha(m,n)$$

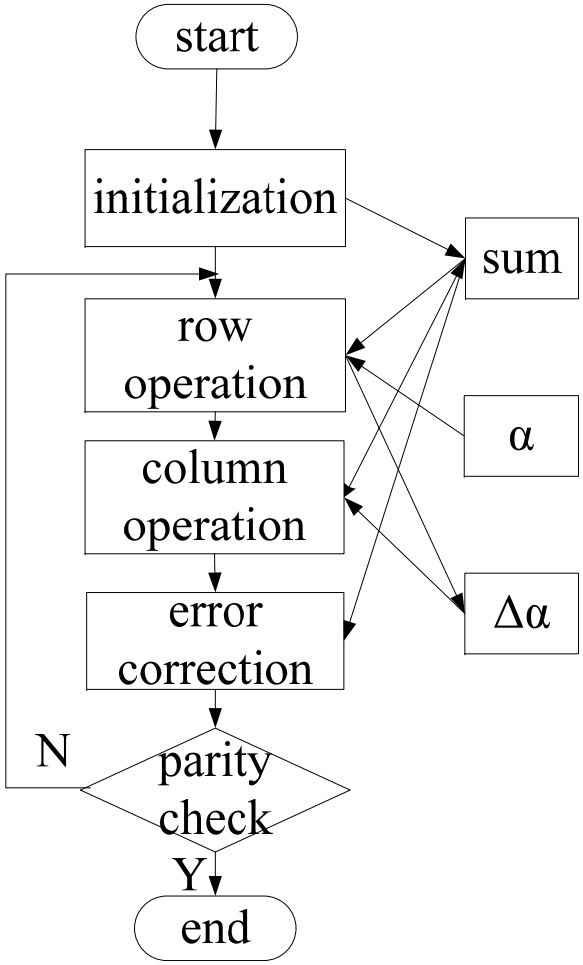
$$\alpha(m,n) = \left(\prod_{n' \in A(m)\backslash n} \mathrm{sign}(\beta(m,n'))\right) \times \min_{n' \in A(m)\backslash n} |\beta(m,n')|$$

$$\Delta\alpha(m,n) = \alpha'(m,n) - \alpha(m,n)$$

Column Operation

$$sum'(n) = sum(n) + \sum_{m' \in D(n)} \Delta\alpha(m',n)$$

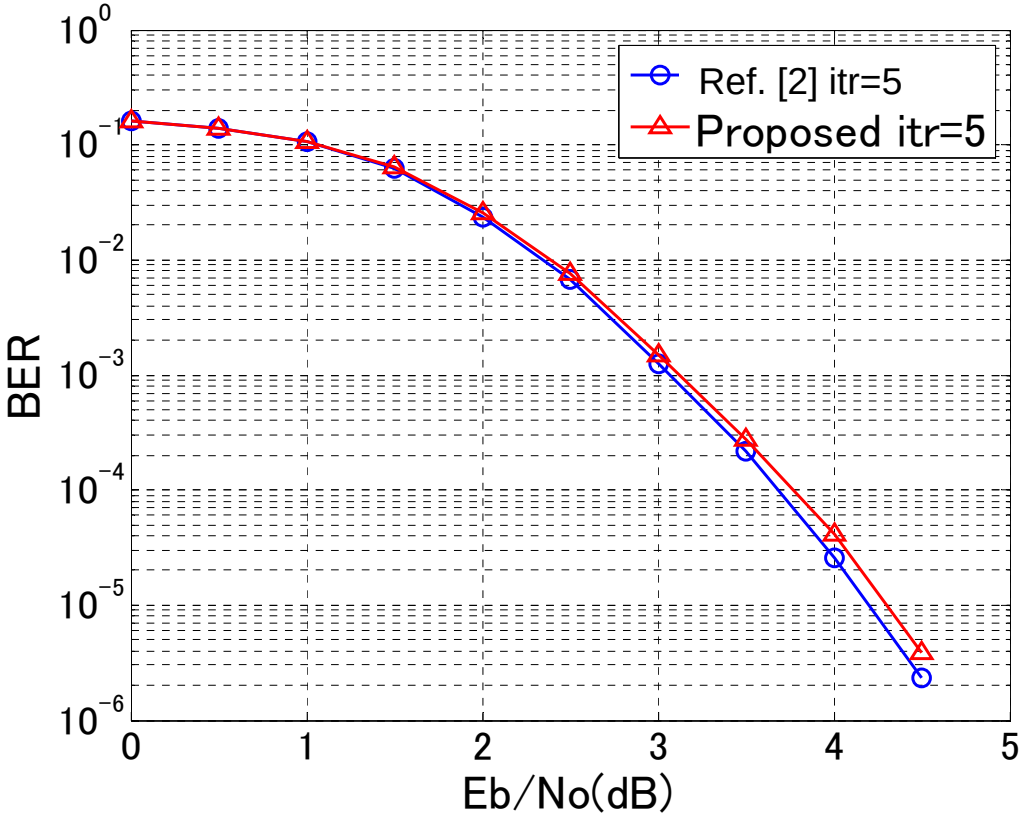
	Ref. [2]	proposed	Comparison
β	1,949,487	0	+1,949,487
sum	0	347,036	-347,036
α	1,949,487	1,695,501	+253,986
λ	1,301,845	0	+1,301,845
Δα	0	40,395	-40,395
Total saving			+3,117,887



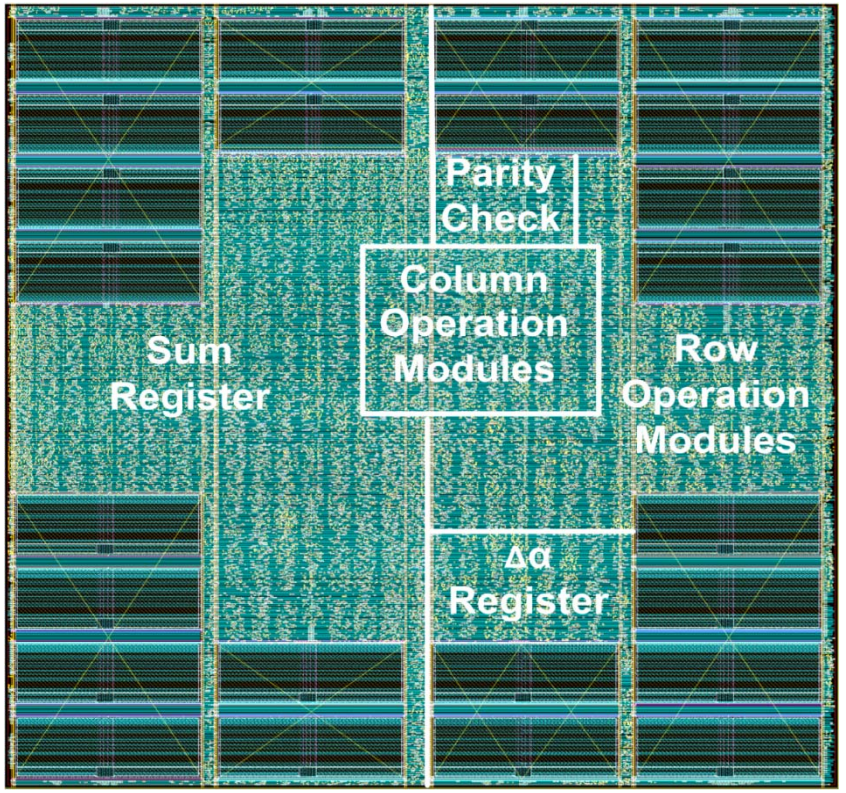
[2] X. Li, Y. Abe, K. Shimizu, Z. Qiu, T. Ikenaga, S. Goto, "Cost-efficient partially-parallel irregular LDPC decoder with message passing schedule", International Symposium on Integrated Circuits (ISIC-2007), Sep. 2007.

Implementation Result

BER Performance



Chip Layout



[2] X. Li, Y. Abe, K. Shimizu, Z. Qiu, T. Ikenaga, S. Goto, "Cost-efficient partially-parallel irregular LDPC decoder with message passing schedule", International Symposium on Integrated Circuits (ISIC-2007), Sep. 2007.

Simulation Result

	Ref[4]	Ref[3]*	Ref.[2]	***proposed***
Design rule	0.11μm	TSMC 0.18μm CMOS		
LDPC Code	8088bit rate 1/2 irregular	802.11n 648bit rate 1/2 irregular LDPC		
Throughput (itr =5,SNR=3.0dB)	188Mbps	54Mbps	54Mbps	***404Mbps***
Frequency	212MHz	200MHz	200MHz	***200MHz***
Memory area(gates)	407K	708K	502K	***170K***
Area w/o wiring (gates)	742K	832K	611K	***313K***
Area w/. wiring (μm^2)	NA	13,090,549	9,004,366	***8,012,999***
Power[mW] @200MHz, SNR=3.0, 1.62V	NA	765.85	486.44	***712.38***
Chip area(mm^2)	NA	NA	NA	***13.69***

[3] K. Shimizu, T. Ishikawa, N. Togawa, T. Ikenaga, and S. Goto, "Power-efficient LDPC decoder architecutre based on accelerated message-passing shcedule", IEICE Trans. Fundamentals, vol. E89-A, no. 12, pp. 3602-3612
[4] Y. Chen and D. Hocevar, "A FPGA and ASIC implementation of rate 1/2 8088-b irregular low density parity check decoder", in IEEE Global Telecommunications Conf., Dec. 2003, pp. 113-117