CKVdd: A Self-Stabilization Ramp-Vdd Technique for Dynamic Power Reduction

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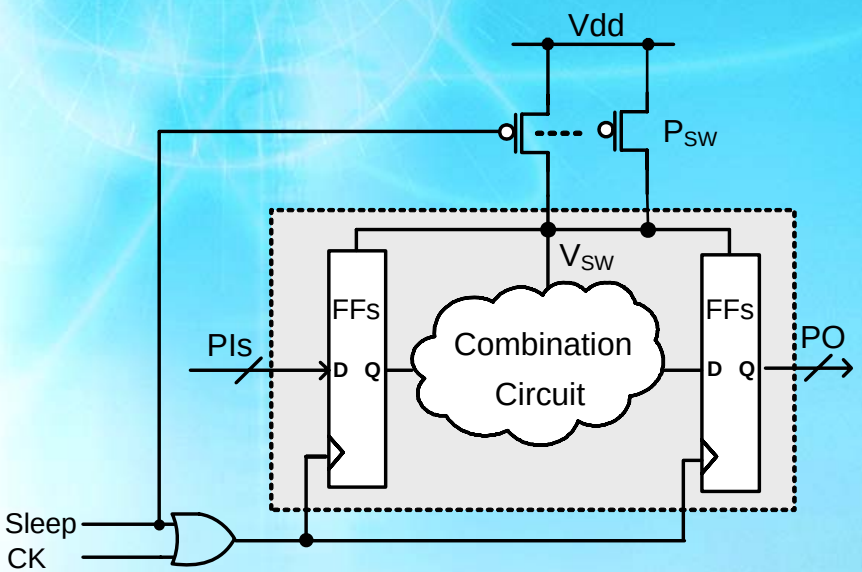
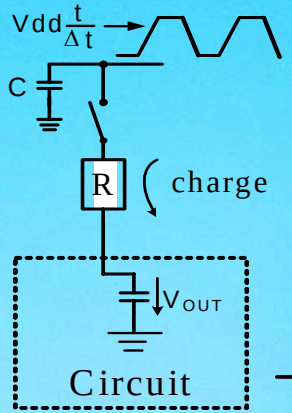
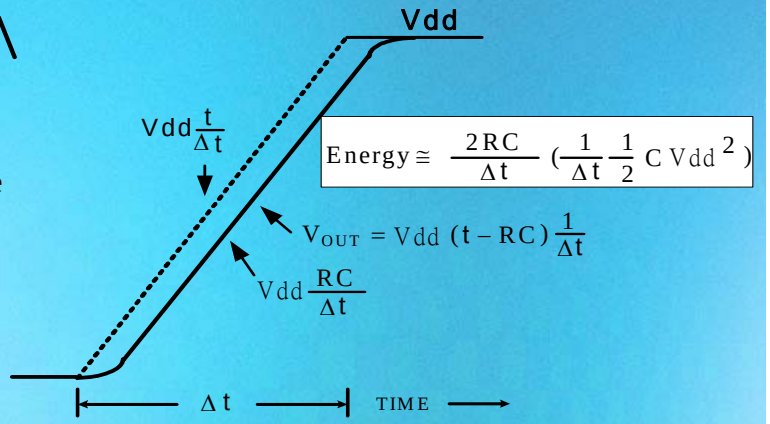
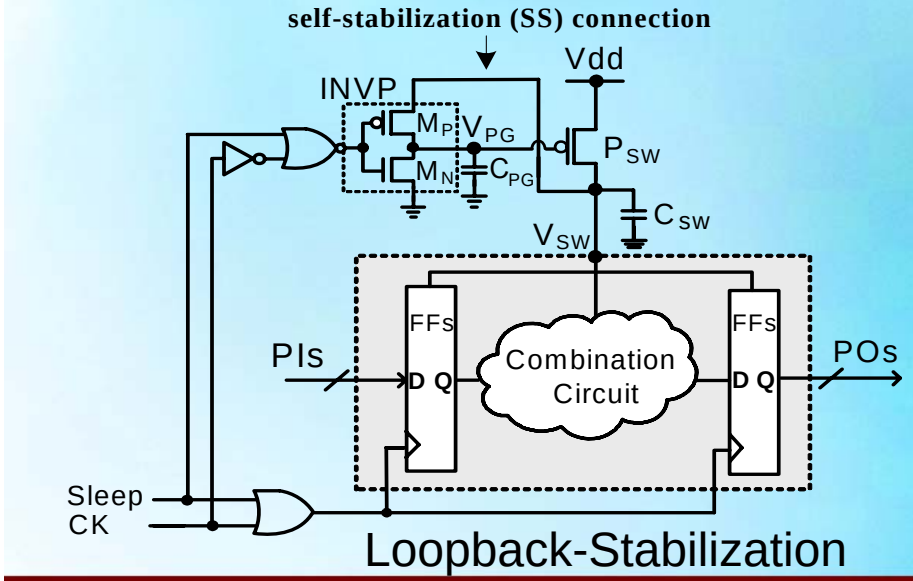
Propose CKVdd Circuit Structure

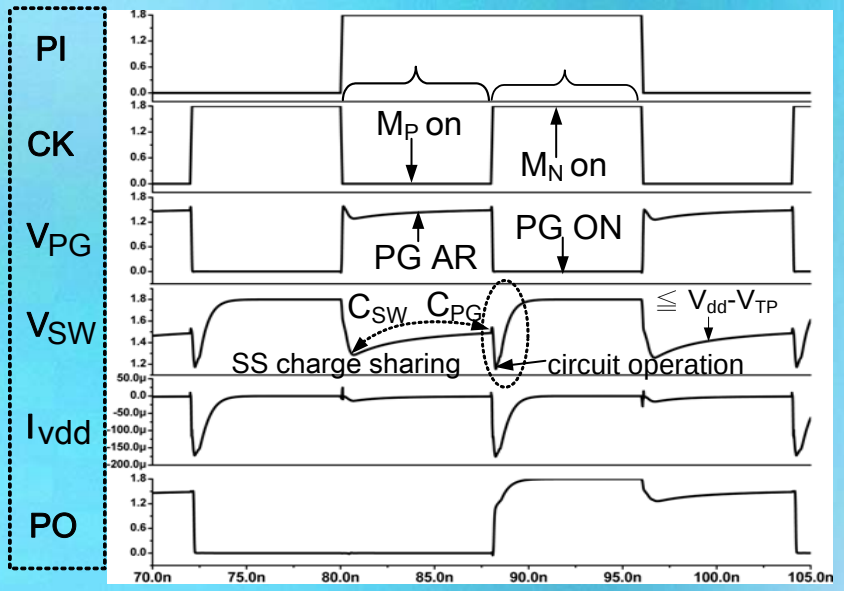




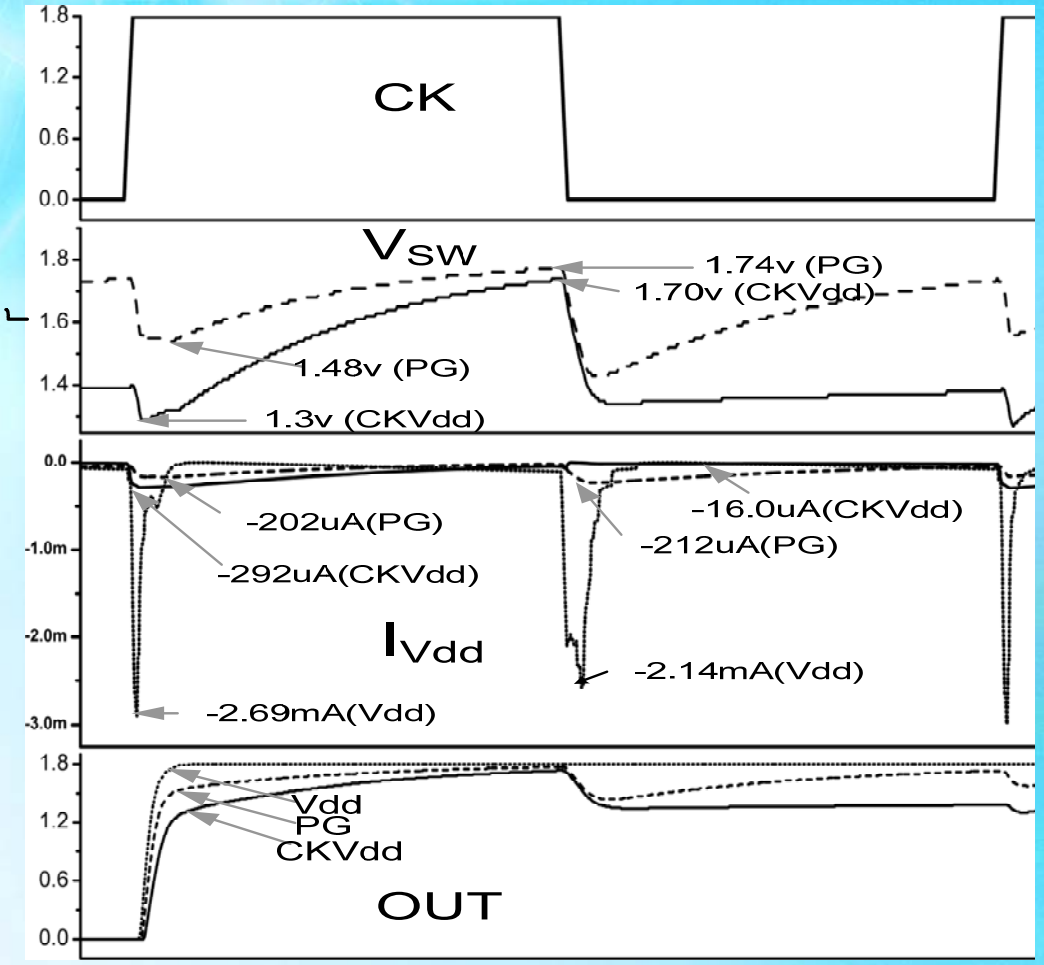


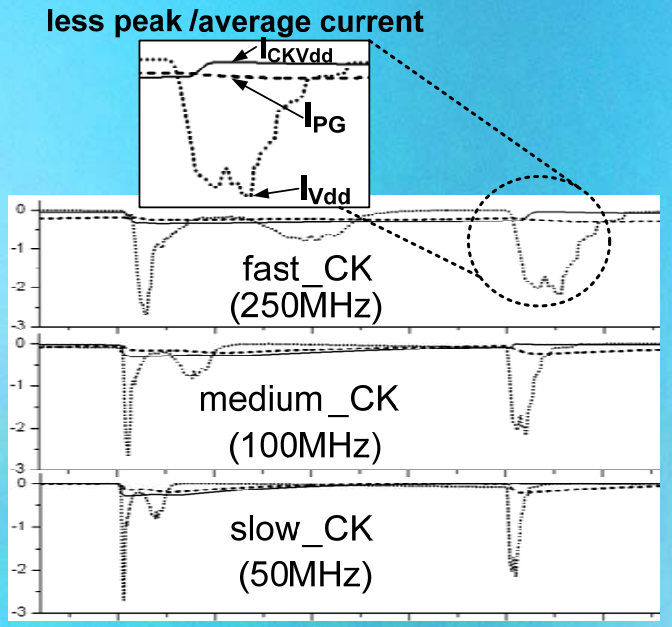


Loopback-Stabilization

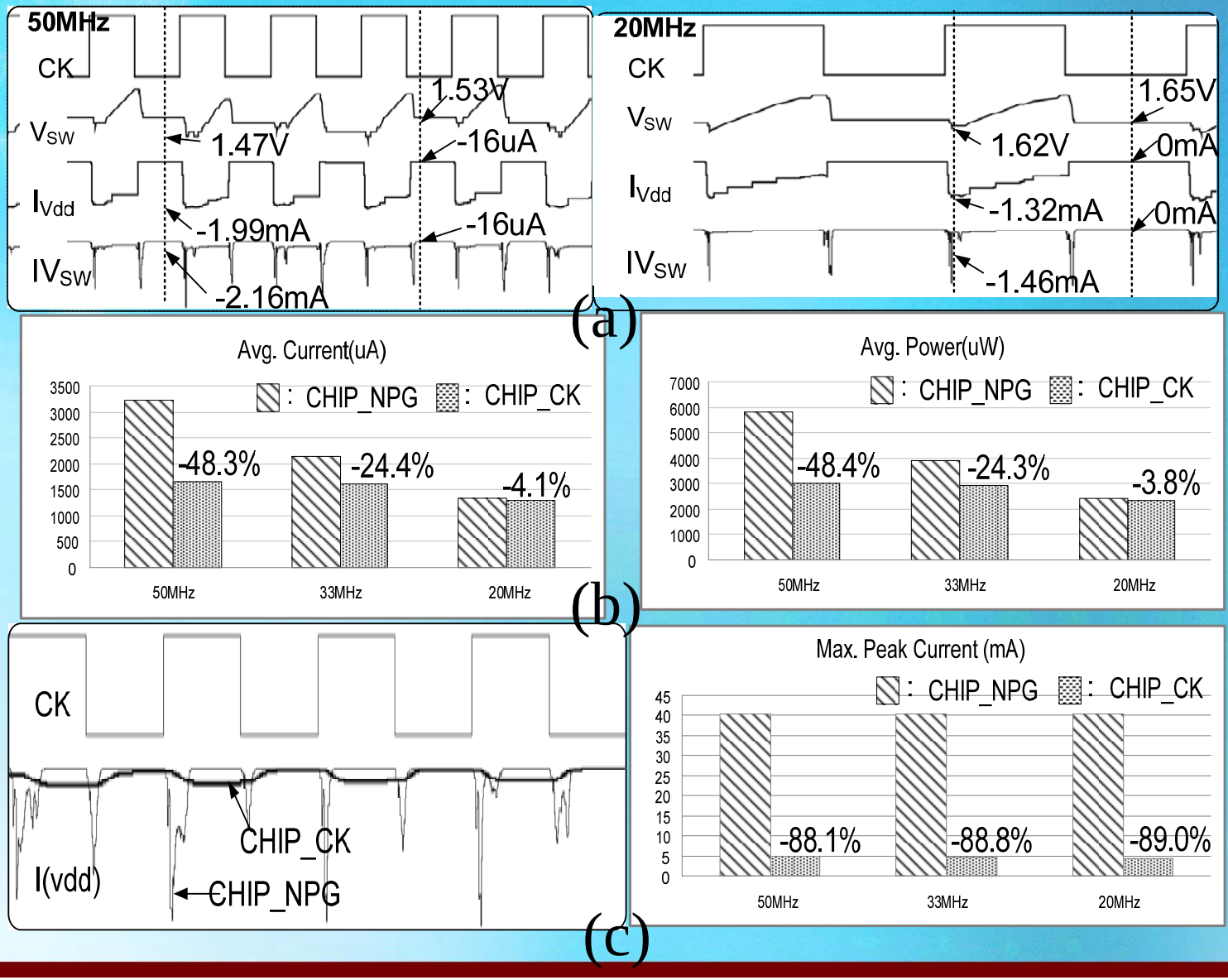


CKVdd Low Power Technique

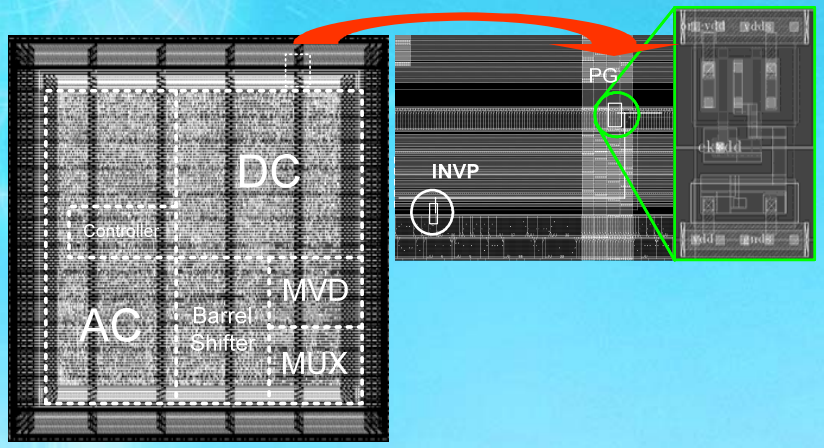


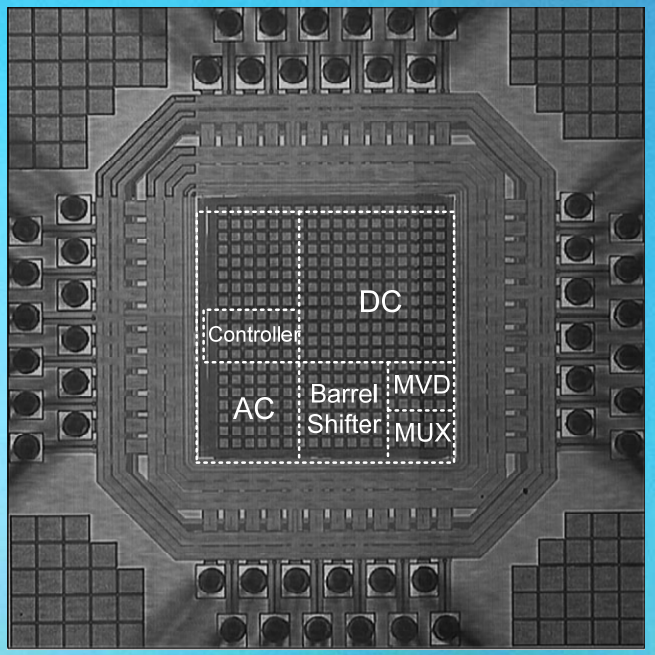


MPEG VLD Postlayout Simulation Analysis



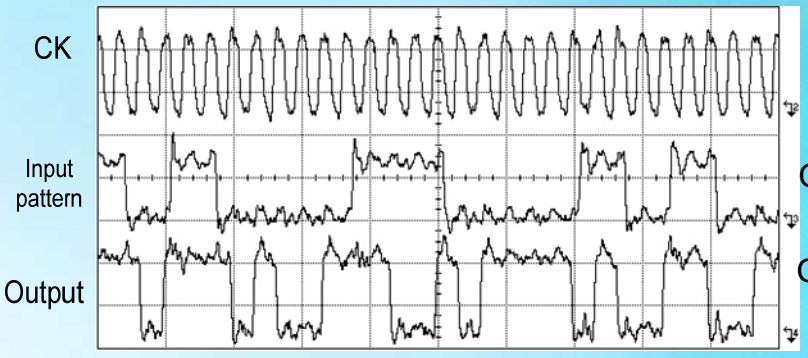
VLD Test Chip Implementation and Testing

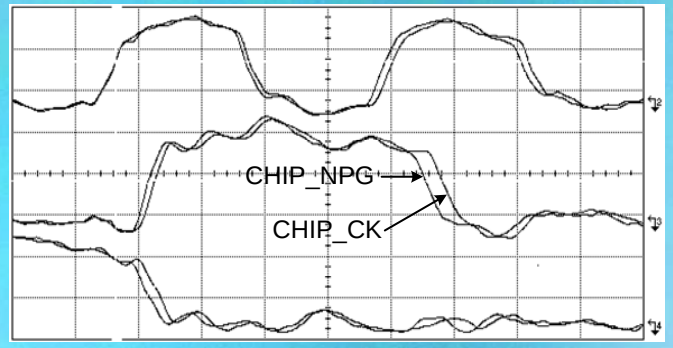




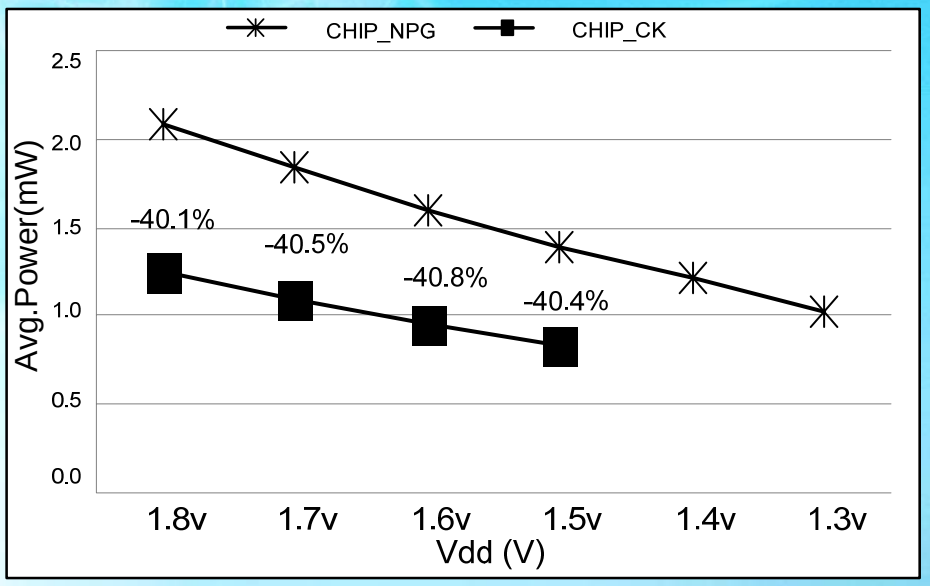
Technology	TSMC 0.18μm 1P6M CMOS
Supply Voltage	1.8V
Chip Size / Core Size	1.49x1.49 mm^2 /0.645x0.645 mm^2
Transistors	74382
Operation frequency/ Power Consumption	36.5MHz/3.19mW(CHIP_NPG) 36.5MHz/1.75mW(CHIP_CK)

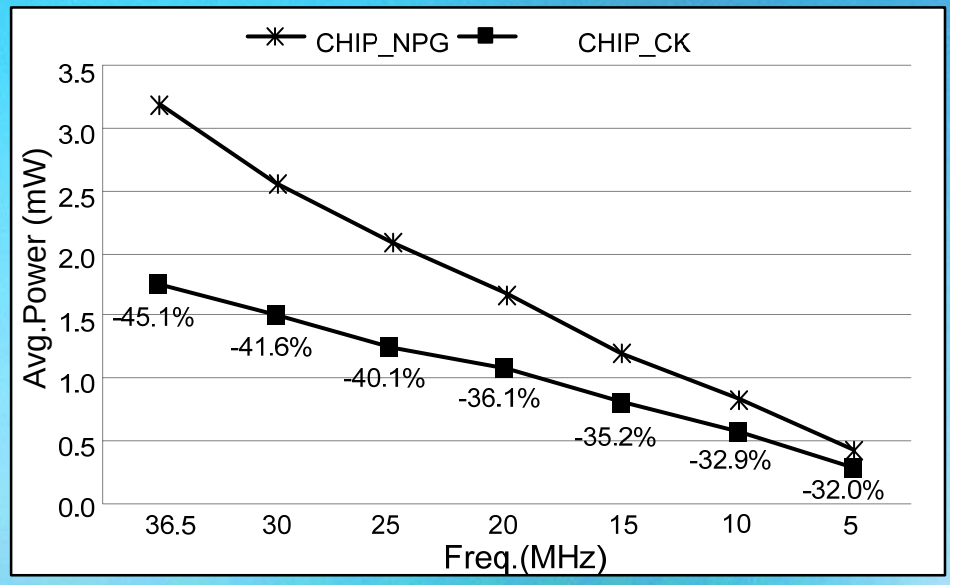
- The chip features





MPEG VLD Chip Measurement Results

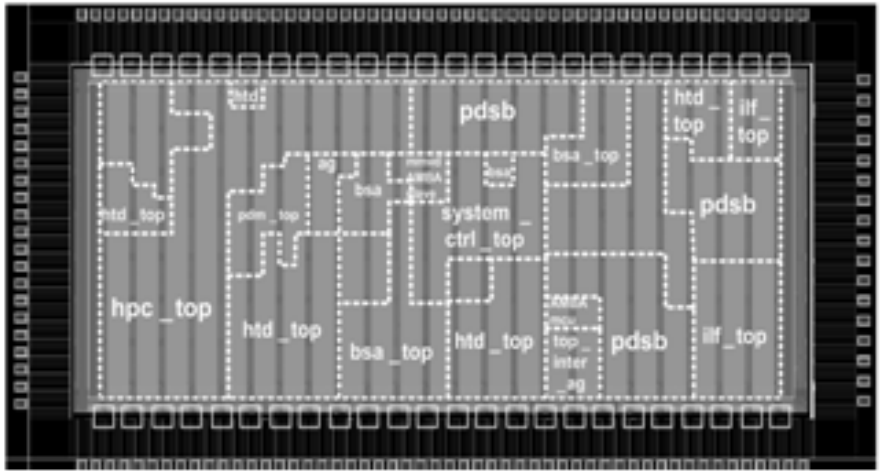


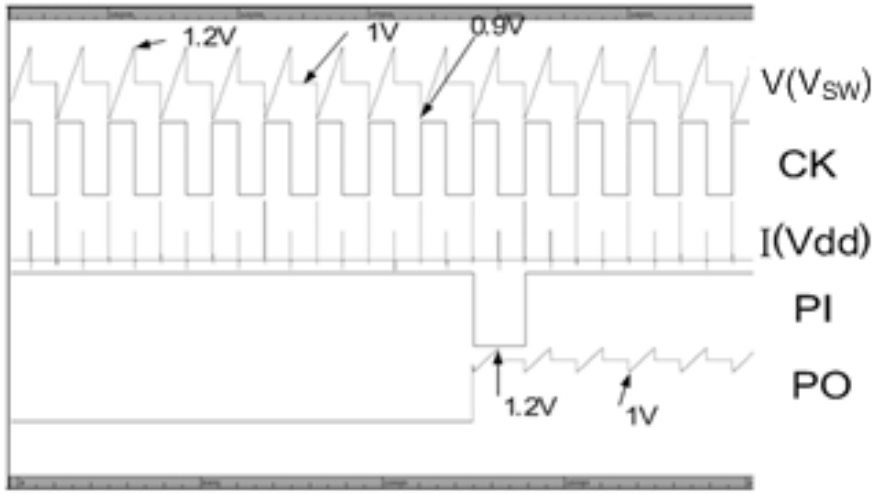


1. At a 36.5MHz clock frequency, CHIP_CK savings ratio becomes 45.1%.
2. Both CHIP_CK and CHIP_NPG increase power use as frequency increases, it is interesting to note that the increase is lower for CHIP_CK

CKVdd Multi-mode Multi-channel Video Decoder

● Multi-mode Multi-channel Video Decoder (MMVD)





● Comparison result

Items		MMVD(RaVdd)	MMVD (Vdd)
Specification		MPEG - 1/2 Simple Profile	
		MPEG - 4 Simple Profile	
		H.264 Baseline Profile	
		Resolution : Up to HD1080	
Transistor count		3,023,379	2,994,166
Internal Memory		55kB	55kB
Technology (um)		0.13	0.13
Power Supply		1.2	1.2
Core size		4.16mm x 1.96 mm	4.17mm x 1.21mm
Current(mA)	125MHz	18.77 (-76.53%)	79.96
Power (mW)		56.38 (-41.24%)	95.95
Delay (ns)		0.3 (0%)	0.3

Thanks for Your Attention *!!*