CKVdd: A Self-Stabilization Ramp-Vdd Technique for Dynamic Power Reduction

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Propose CKVdd Circuit Structure

Energy \cong \frac{2RC}{\Delta t} (\frac{1}{\Delta t} - \frac{1}{2} C Vdd^2)

V_{OUT} = V_{dd} (t - RC) \frac{1}{\Delta t}

\Delta t

TIME

INVP

M_P

M_P

M_N

M_N

V_{dd}

V_{dd}

P_{SW}

C_{sw}

C_{sw}

V_{SW}

V_{SW}

V_{dd}

V_{dd}

FFs

FFs

DQ

DQ

PIS

POs

PIS

PO

Sleep CK

Sleep CK

self-stabilization (SS) connection

SS charge sharing

circuit operation
CKVdd Low Power Technique

- **CK**: Clock signal
- **V_{SW}**: Switching voltage
- **I_{Vdd}**: Current at Vdd
- **V_{dd}**: Supply voltage
- **PG**: Power Good
- **CKVdd**: A reference voltage level

- **Less peak/average current**
- **Fast_CK (250MHz)**
- **Medium_CK (100MHz)**
- **Slow_CK (50MHz)**
MPEG VLD Postlayout Simulation Analysis

(a) Voltage and Current Waveforms at 50MHz and 20MHz

(b) Average Current and Power Comparison

(c) Maximum Peak Current Comparison
VLD Test Chip Implementation and Testing

<table>
<thead>
<tr>
<th>Technology</th>
<th>TSMC 0.18μm 1P6M CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>1.8V</td>
</tr>
<tr>
<td>Chip Size / Core Size</td>
<td>1.49x1.49 mm² / 0.645x0.645 mm²</td>
</tr>
<tr>
<td>Transistors</td>
<td>74382</td>
</tr>
<tr>
<td>Operation frequency/ Power Consumption</td>
<td>36.5MHz/3.19mW(CHIP_NPG) 36.5MHz/1.75mW(CHIP_CK)</td>
</tr>
</tbody>
</table>

The chip features

- CK
- Input pattern
- Output
- CK
- Out1
- Out2
- CHIP_NPG
- CHIP_CK
MPEG VLD Chip Measurement Results

1. At a 36.5MHz clock frequency, CHIP_CK savings ratio becomes 45.1%.
2. Both CHIP_CK and CHIP_NPG increase power use as frequency increases, it is interesting to note that the increase is lower for CHIP_CK.
CKVdd Multi-mode Multi-channel Video Decoder

Comparison result

<table>
<thead>
<tr>
<th>Items</th>
<th>MMVD (RaVdd)</th>
<th>MMVD (Vdd)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Specification</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MPEG - 1/2 Simple Profile</td>
<td></td>
<td></td>
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<tr>
<td>MPEG - 4 Simple Profile</td>
<td></td>
<td></td>
</tr>
<tr>
<td>H.264 Baseline Profile</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Resolution: Up to HD1080</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Transistor count</td>
<td>3,023,379</td>
<td>2,994,166</td>
</tr>
<tr>
<td>Internal Memory</td>
<td>55kB</td>
<td>55kB</td>
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<tr>
<td>Technology (um)</td>
<td>0.13</td>
<td>0.13</td>
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<tr>
<td>Power Supply</td>
<td>1.2</td>
<td>1.2</td>
</tr>
<tr>
<td>Core size</td>
<td>4.16mm x 1.96 mm</td>
<td>4.17mm x 1.21mm</td>
</tr>
<tr>
<td>Current (mA)</td>
<td>18.77 (-76.53%)</td>
<td>79.96</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>56.38 (-41.24%)</td>
<td>95.95</td>
</tr>
<tr>
<td>Delay (ns)</td>
<td>0.3 (0%)</td>
<td>0.3</td>
</tr>
</tbody>
</table>
Thanks for Your Attention !!