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HIROSAKI UNIV
VLSI PROJECT

Design and Chip Implementation of the Ubiquitous Processor HCgorilla

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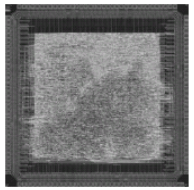
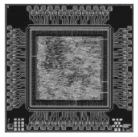
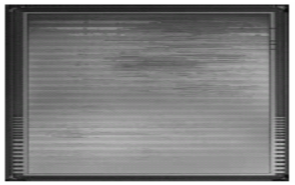
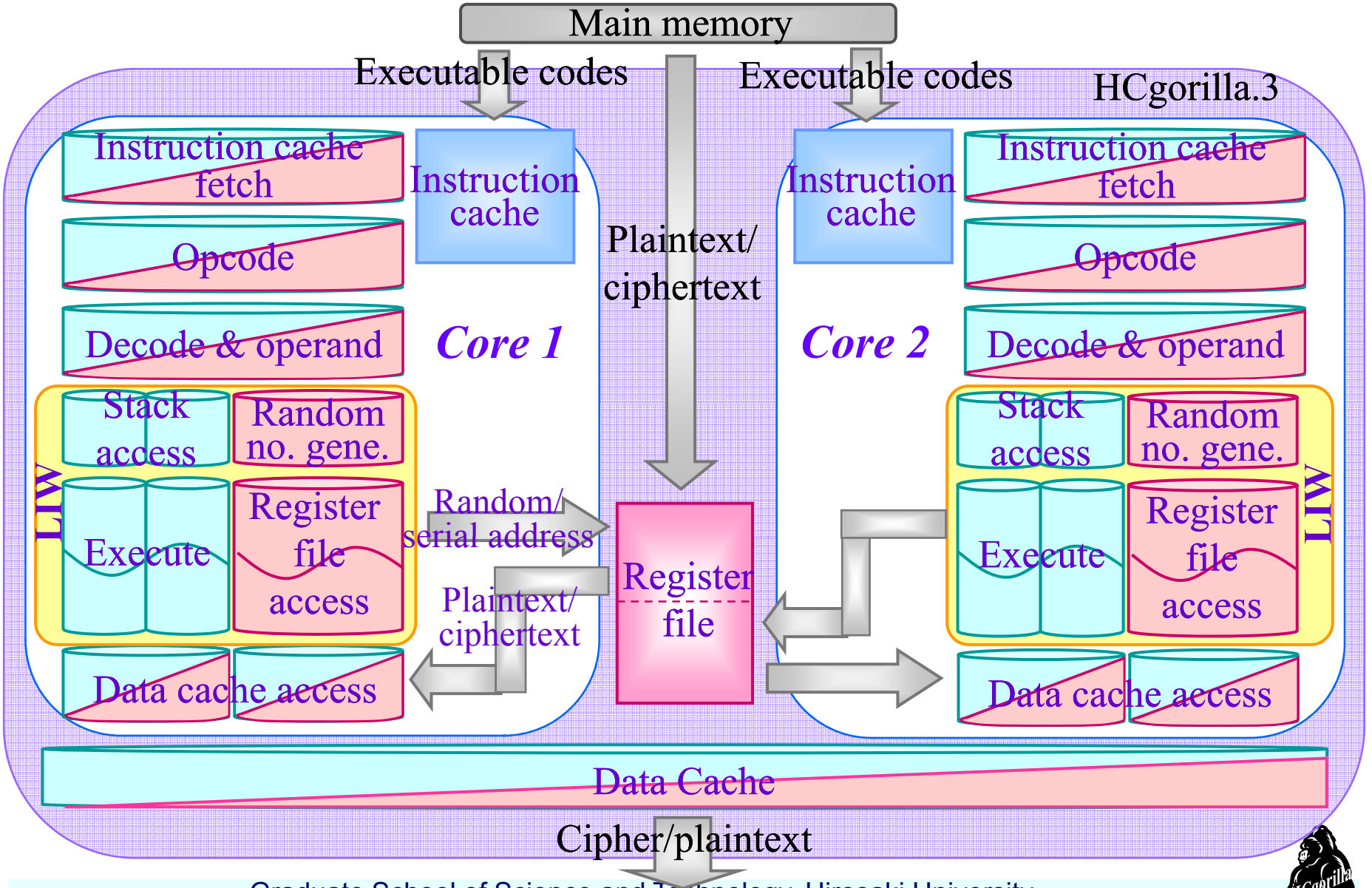
Overview

- HCgorilla
  - ✓ Ubiquitous computing
  - ✓ Special architecture
- Architectural points
  - ✓ H/S co-design
  - ✓ Parallelism: multicore & multiple pipeline
  - ✓ Popularity: Java compatible media pipes
  - ✓ Security: cipher pipes for streaming
- Chip design & implementation
  - ✓ Power conscious wave-pipelining
  - ✓ Test simplification design scheme
  - ✓ 0.18μm CMOS standard cell

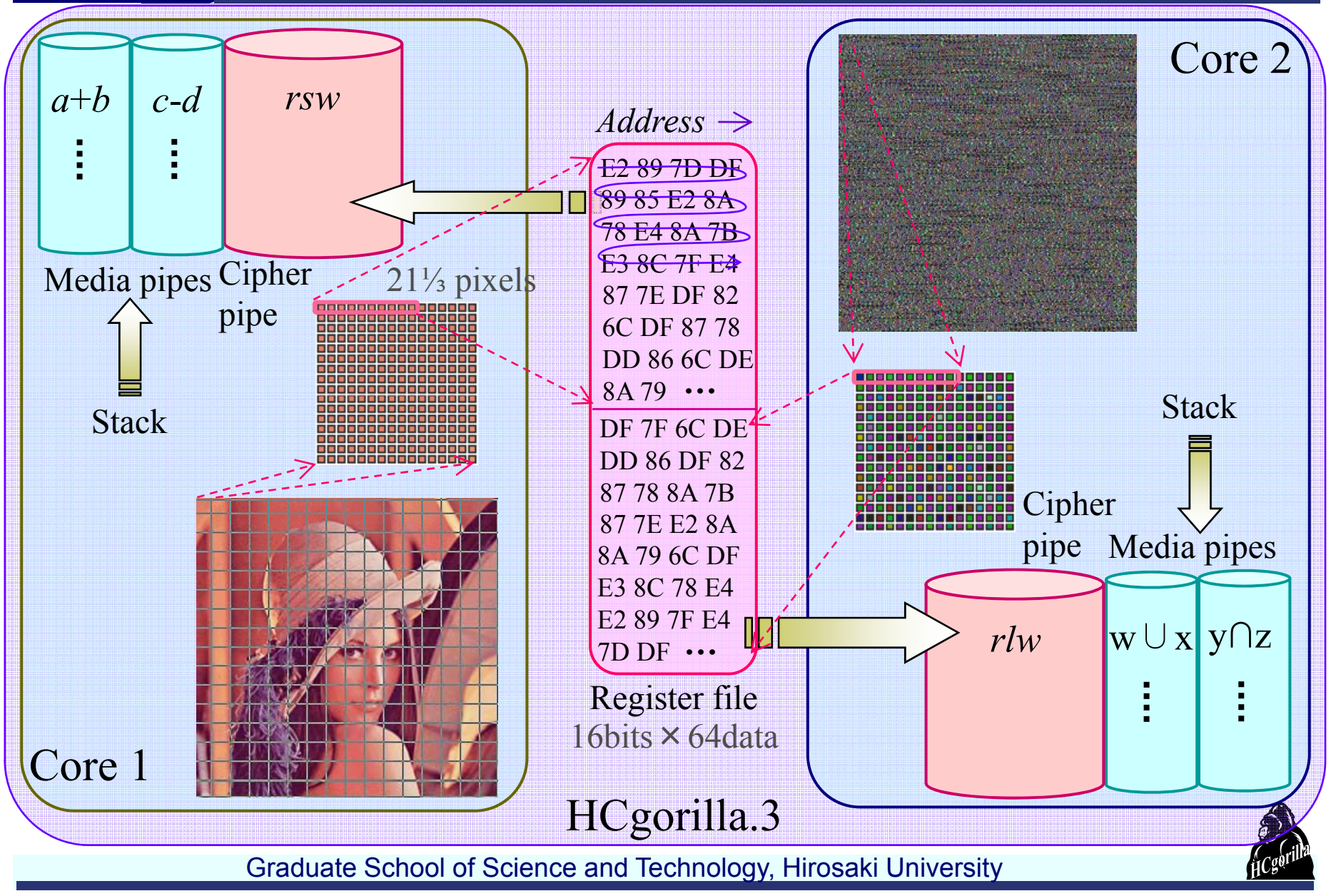
Versions of HCgorilla architecture and chip

				HCgorilla.1	HCgorilla.2	HCgorilla.3
Architecture	Name			HCgorilla.1	HCgorilla.2	HCgorilla.3
	ISA	Java compatible		16	61	
		Cipher	No.	2	2	
			Mode	SISD	SIMD	
Micro-architecture	Instruction cache			2 × 16bits × 16data	2 × 16bits × 8data	2 × 16bits × 32data
	Register file			16bits × 32data	16bits × 16data	16bits × 64data
	Data cache			64byte	64byte	256byte
	No. of gates			75k	94k	702K
	No. of transistors			255k	228k	1.7M
Chip	Name			HCgorilla035	HCgorilla018	HCgorilla018v3
	Process			ROHM 0.35μm	HITACH 0.18μm	ROHM 0.18μm
	Size			4.9mm square	2.8mm square	4.9mm × 7.9mm
	Core utilization			0.63	0.56	0.80
	Die photo					
	Voltage (V)			3.3	1.8	
	Clock (MHz)			150	400	330
	Power (mW)			230	40	122

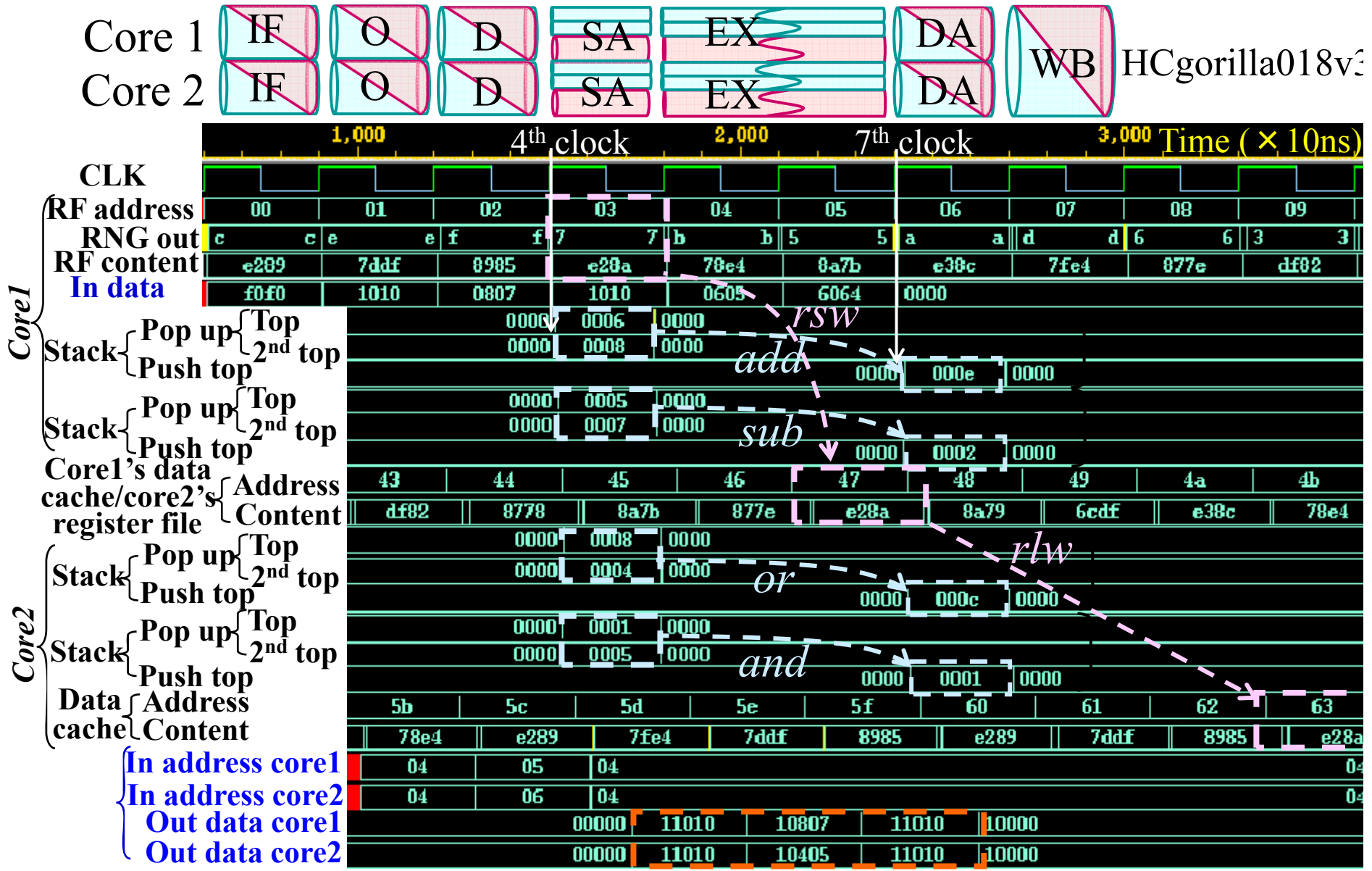
Organization of HCgorilla.3



Test bench X


a+b
c-d
rsw
Media pipes
Cipher pipe
Stack
21⅓ pixels
Core 1
Address
E2 89 7D DF
89 85 E2 8A
78 E4 8A 7B
E3 8C 7F E4
87 7E DF 82
6C DF 87 78
DD 86 6C DE
8A 79 •••
DF 7F 6C DE
DD 86 DF 82
87 78 8A 7B
87 7E E2 8A
8A 79 6C DF
E3 8C 78 E4
E2 89 7F E4
7D DF •••
Register file
16bits × 64data
Core 2
Stack
Cipher pipe
Media pipes
rlw
w ∪ x
y ∩ z
HCgorilla.3

HCgorilla018v3 simulation by the test bench *X*



Power dissipation of HCgorilla018v3 chip