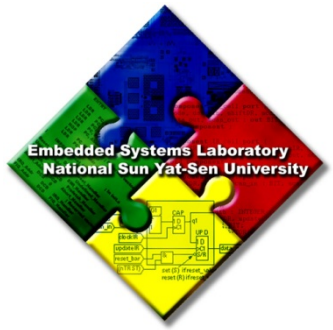
An 8.69 Mvertices/s 278 Mpixels/s Tile-based 3D Graphics SoC HW/SW Development for Consumer Electronics



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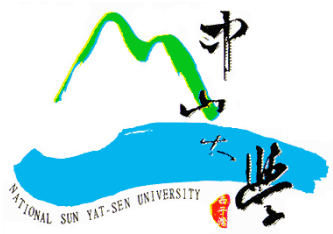
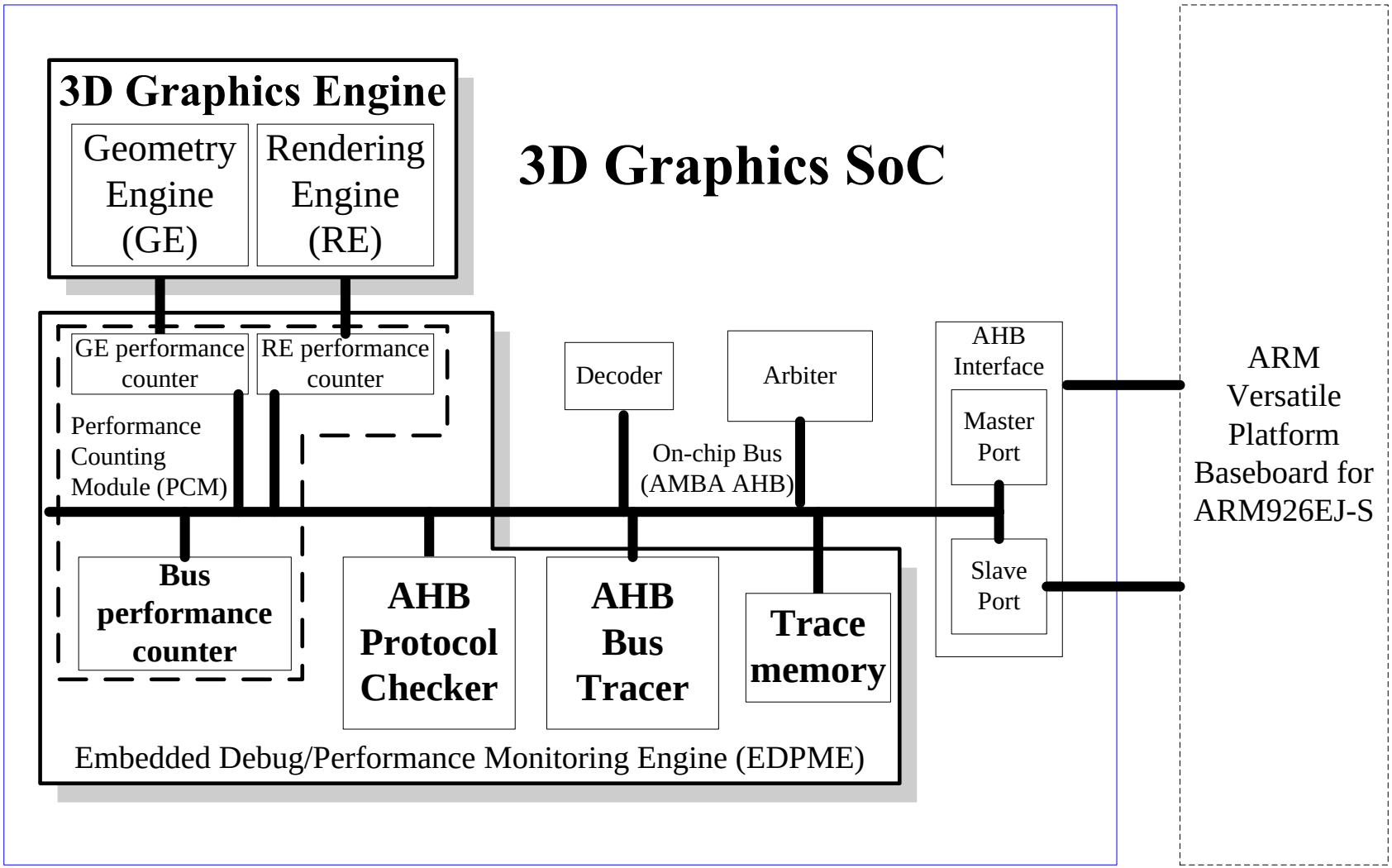
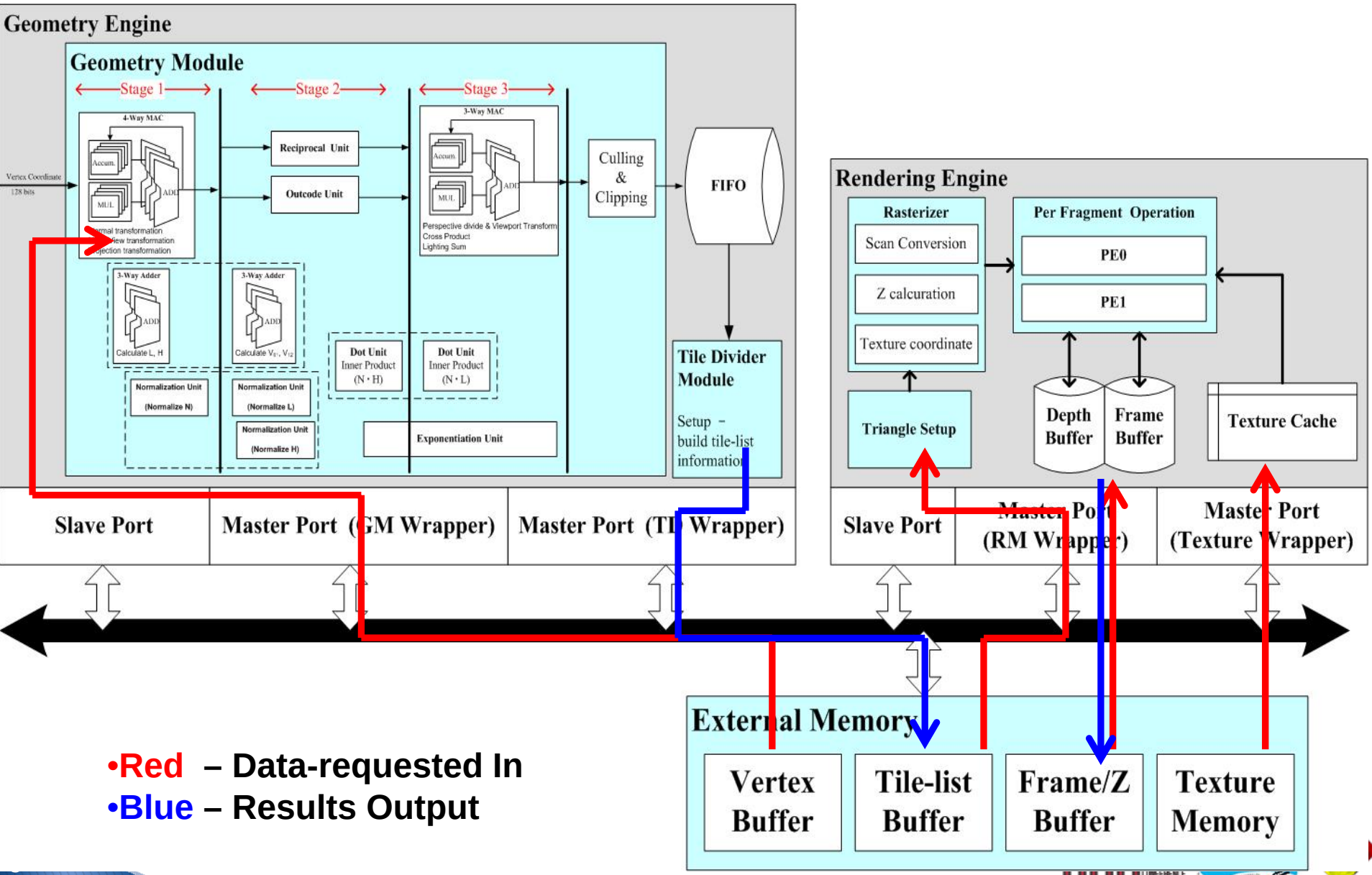


Presenter: Liang-Bi Chen

Block diagram of proposed 3DG SoC



Block diagram of GE and RE

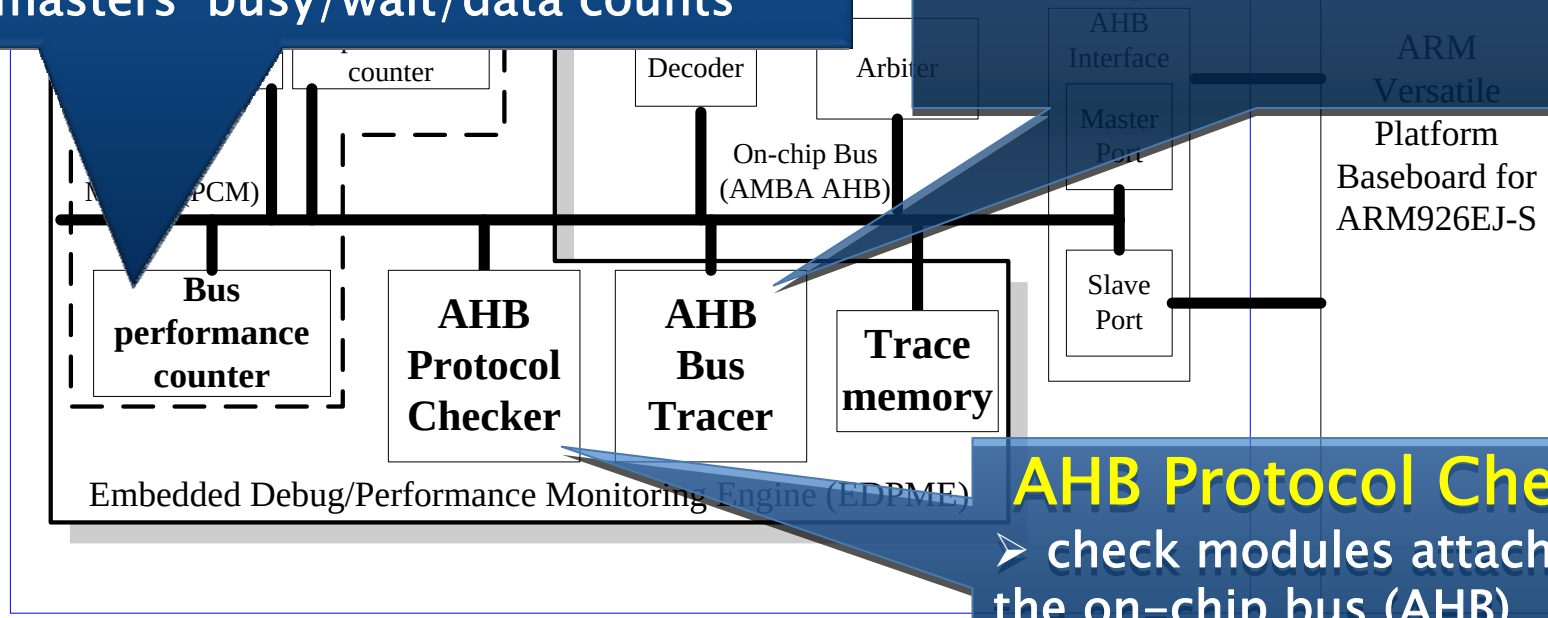


- **Red** – Data-requested In
- **Blue** – Results Output

- GE
  - cycles, triangles, reads, TD reads/writes, TD memory space
- RE
  - cycles, reads/writes, pre/post-fragment pixels, processed triangles
- On-chip bus
  - busy/idle/conflict counts, masters' busy/wait/data counts

AHB Bus Tracer

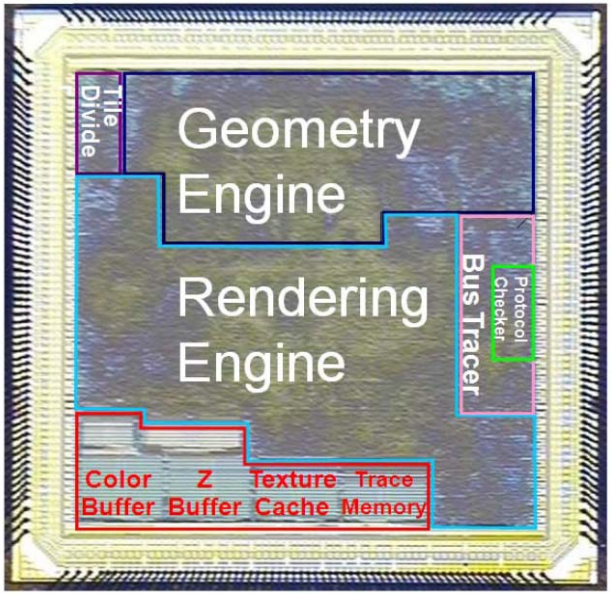
- capture bus tracers for debugging or performance analyses
  - cycle-level vs. transaction level
  - state-of-the-art compression ratio

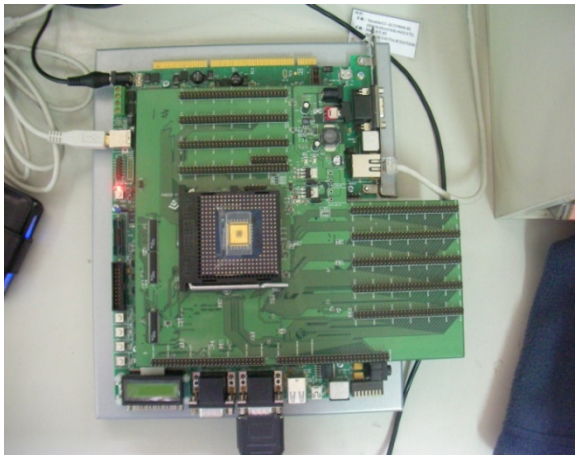


AHB Protocol Checker

- check modules attached to the on-chip bus (AHB)
  - protocol error
  - protocol inefficiency

Chip specification and characteristics





Chip Spec.	**Process Technology**	TSMC 0.18μm CMOS 1P6M
	Supply Voltage	1.8V for Core 3.3V for I/O Cells
	Power Consumption	476.6mW (core power)
	Gate Count	986.5K gates
	Die Size	$3.96 \times 3.96 mm^2$
	Package	PBGA 256 pin
	Operating Frequency	139MHz
3DG Engine	**3DG Performance**	8.69M vertices/s for GE, 278M pixels/s for RE, 278M texels/s for Texture
	Texture Mapping	Bilinear perspective correction
	3DG Operation	Fully support OpenGL-ES 1.0 functions
	Target Resolution	Up to 640x480
Embedded Debugging/ Performance Monitoring Engine	**Bus Tracer**	Provide 4 signal/timing abstraction levels
		Real-time compression
	Performance Counting Module	Provide GE/RE/System bus performance information, include triangle rate, pixel rate, bus idle/utilization/transfer rate and etc.
	Protocol Checker	Rule-based AHB protocol checker, total 73 rules
Software Features	OpenGL-ES API for provided hardware Device driver for Linux 2.6.11 Nano-X Windowing System 3DG Debugging/Performance Monitoring Tool (3DG DPM)	
Prototype	ARM Versatile platform baseboard for ARM926ES-S+Logic Tile FPGA	

Comparison of 3DG Chip performance

3DG Chips	Imai et al. ISSCC2004	Sohn et al. ISSCC2005	Kim et al. IEEE JSSC2006	Kim et al. ISSCC2007	Nam et al. ISSCC2007	Our Design
Triangle rate (Mvertices/s)	4.7 (parallel projection)	3.6 (full pipeline with lighting)	7.55 (single specular lighting) (5.45)+	NA	141 (peak for model transform, no lighting perf. available)	8.69 (full pipeline with lighting)
Pixels rate (Mpixels/s)	150 (bilinear)	50	166 (120)+	NA	50	278
Tixel rate (Mtexels/s)	600	200	1300 (939)+	400	200	278
Chip Area (mm^2)	75.43 (25.5025 for 3DG IP)	36 (core 23.04)	49.7 (19.4 for 3DG) (95.3/37.2)+	25	17.2	15.68 (11 for 3DG Engine)
Power (mW)	109.5	155	407 (780)+	379	52.4	472.6
Frequency (Mhz)	75	50-200/ 12.5-50 (VS/RE)	166/333 (3DG/RISC) (120/240)+	50	89-200 (RISC,VS) 20-50 (RE)	139
Silicon proc. (μm)	0.18	0.18	0.13 (Normalized to 0.18)+	0.18	0.18	0.18
Special features				3D Vision	Dynamic Volt. Freq. Scaling (DVFS)	Embedded debug /perf. Monitoring

Conclusion

- We develop a tile-based 3DG SoC and its related development tools.
  - In hardware design
    - Has better (compared with previous works) performances in the vertex rate and pixel rate, and is the smallest in hardware size.
  - Special features
    - On-chip bus integration
    - Real-time profiling
    - Debugging
    - Performance measurement / tuning
- Future Work
  - Further improve power consumption and texture performance
  - Upgrade to OpenGL ES 2.0