A Delay-Optimized Universal FPGA Routing Architecture

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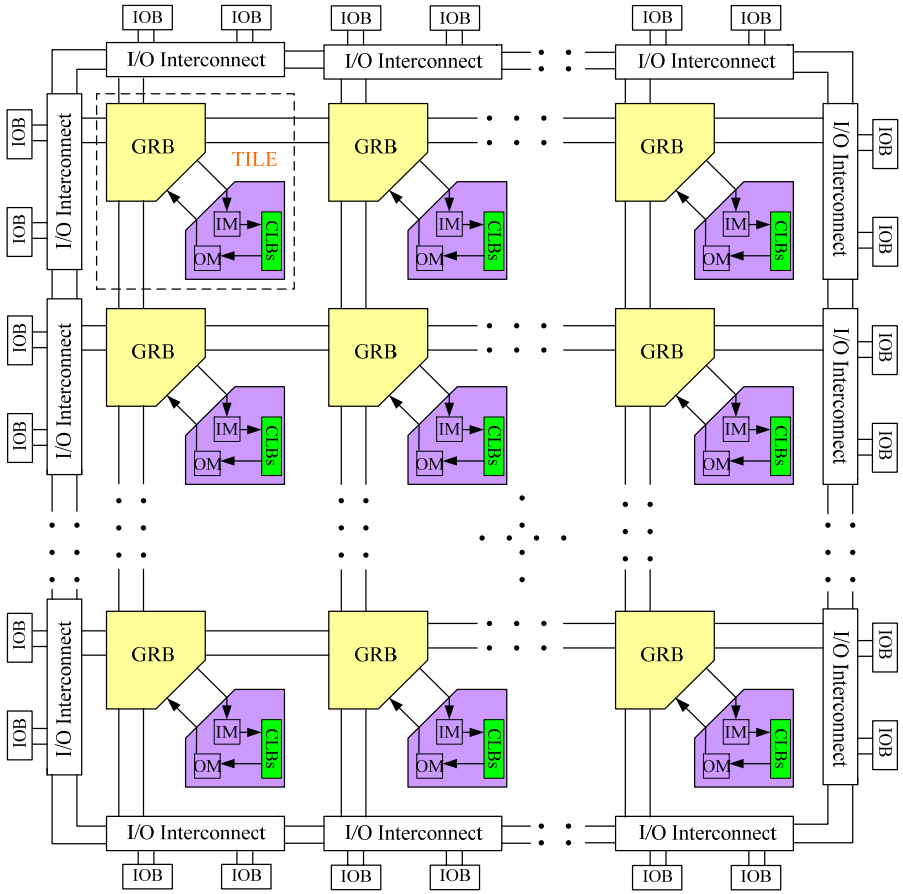
About the design

- A delay–optimized universal FPGA routing architecture is presented.
- Several kinds of routing strategy are used.
- The whole FPGA chip is highly repeatable
- The signal delay is uniform and predictable among the total chip.

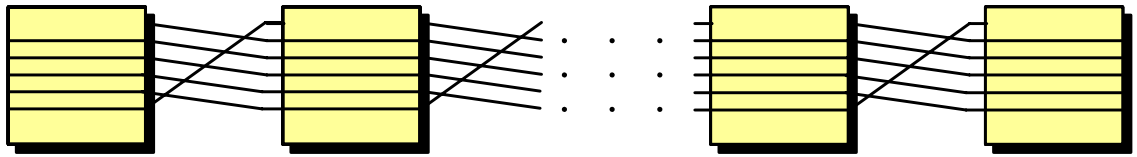
TILE Routing Architecture



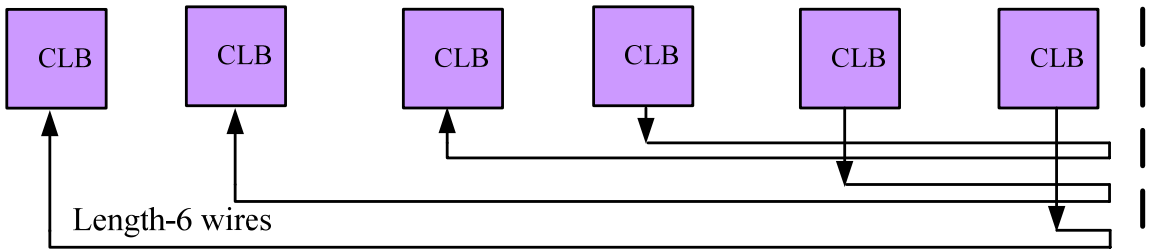
- Input Multiplexer
- Output Multiplexer
- General Routing Box
- Long lines
- Multi-length Lines
- Single lines

Routing strategy

- Offset by sets to the top level of the routing resource



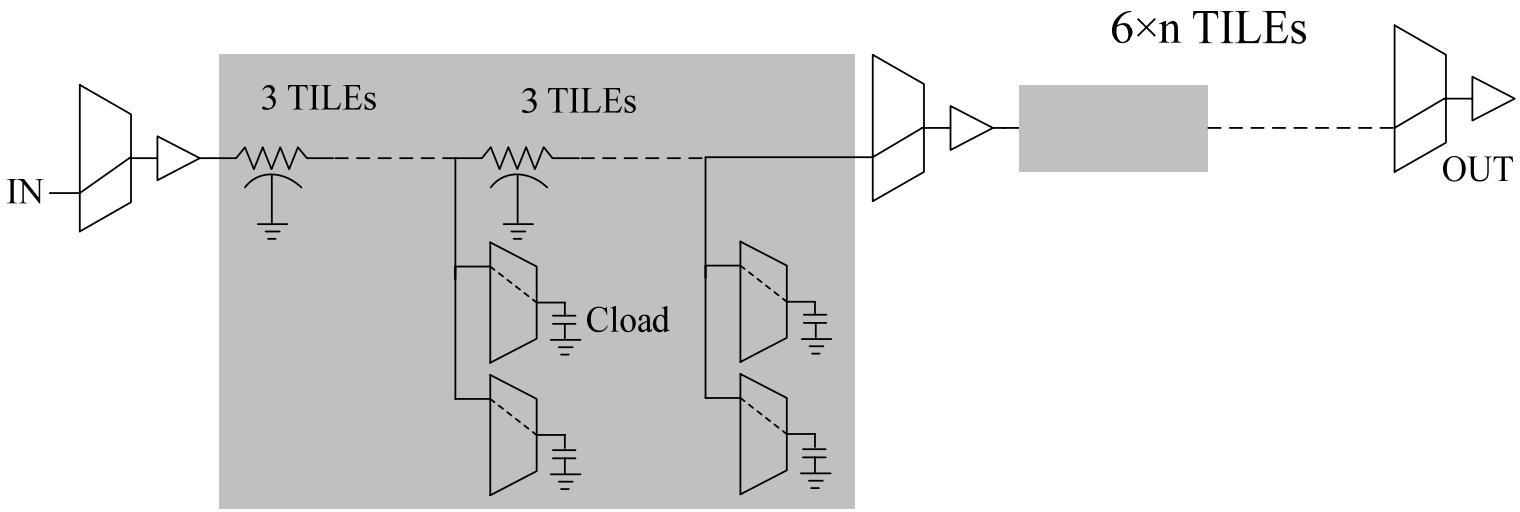
- Complementary hanged end-lines to the I/O routing resource



- Mux + Buffer architecture as routing switchesc

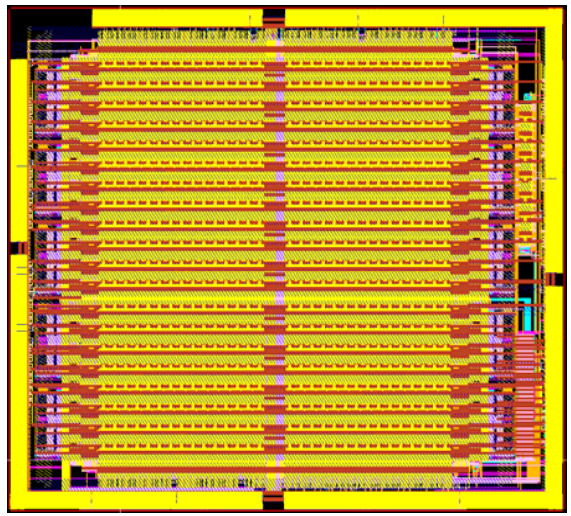
Modeling and Simulation

- RC parasitic parameters of the metal line are drawn from layout and taken into consideration to set up the simulation modules.

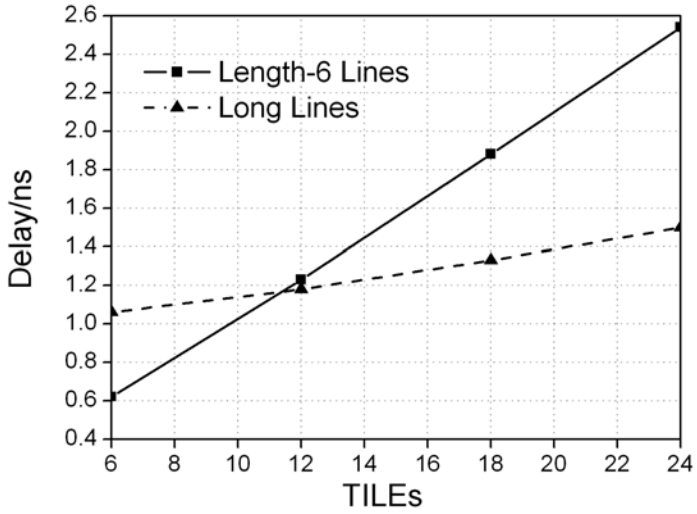


Layout

- SMIC 0.18um CMOS process and technology.
- Array of logic TILE is 20×30.
- The total layout area is 6.5mm×6.8mm
- Routing resource costs approximately 60% of the total area.



Test Result



- The linear relation between the number of TILEs that the length-6 lines or long lines span and the signal delay
- Long lines are better than length-6 lines at long distance signal transmission.