A 1 GHz CMOS Comparator with Dynamic Offset Control Technique

Xiaolei Zhu[1], Sanroku Tsukamoto[2], and Tadahiro Kuroda[1]

[1]Keio University

[2]Fujitsu Laboratories Limited

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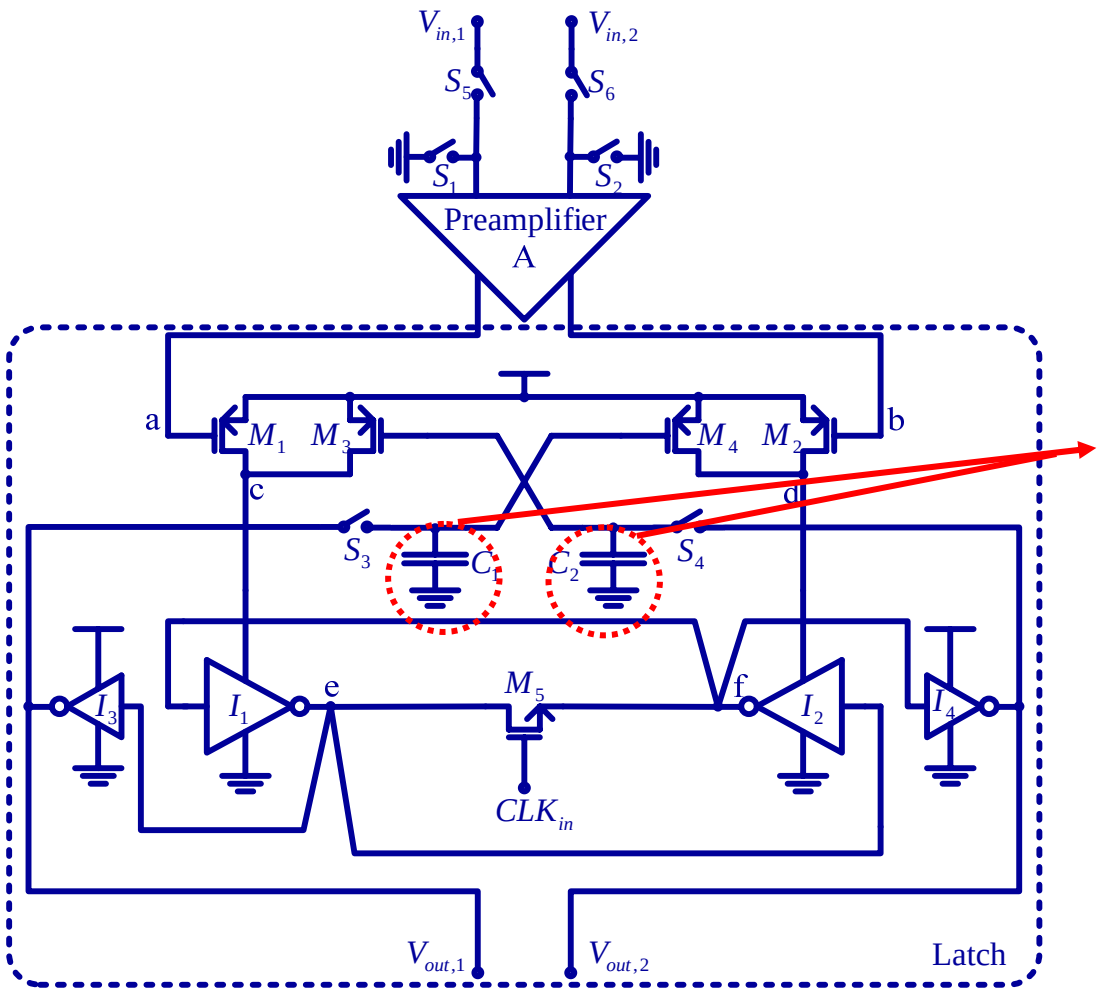
Motivation

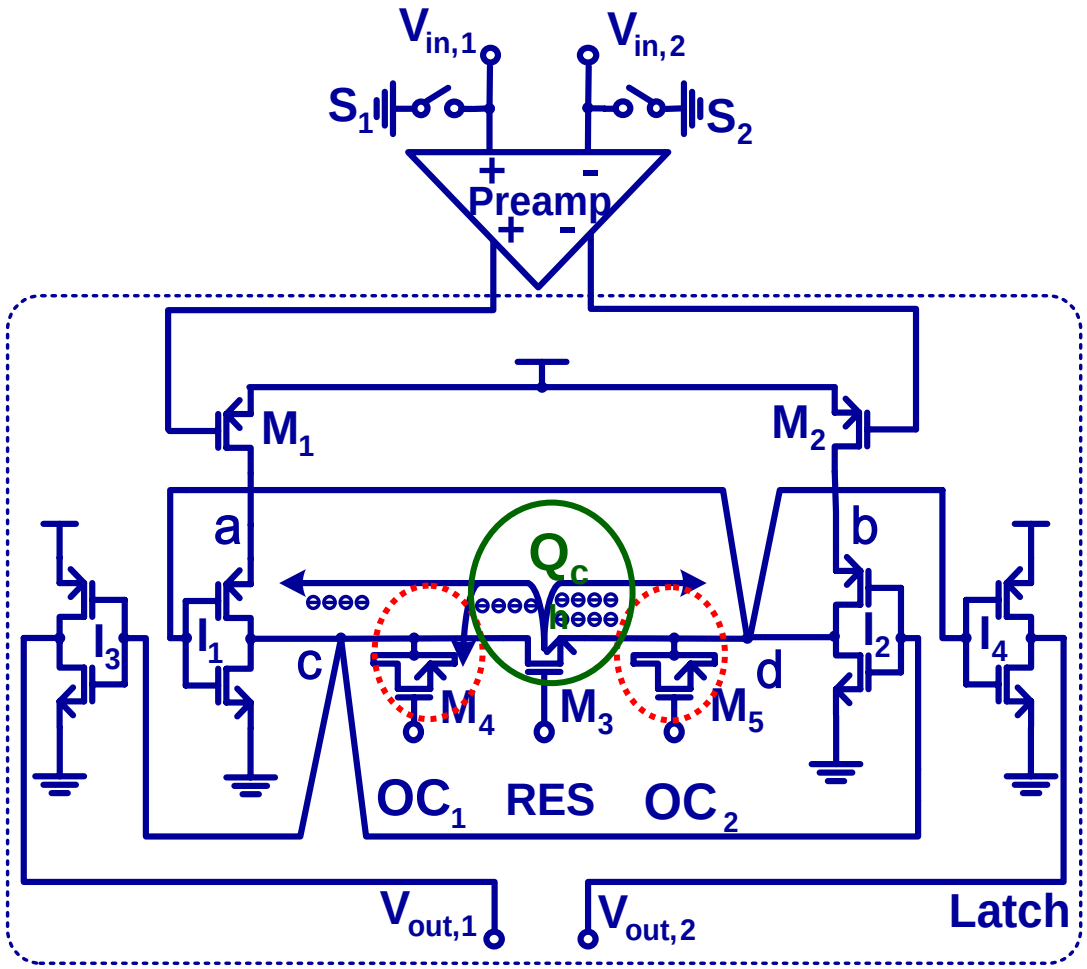


Drawback:

- **Requires quite large die area;**
- **Introduces a substantial amount of noise;**
- **Degrade the response.**

Comparator using capacitors based offset cancellation technique.

Charge Compensation Approach for Comparator Offset Control



Comparator with dynamic offset control technique

– The total charge Q_{ch} in the inversion layer of M_3 :
$Q_{ch}=LWC_{ox}(V_{RES}-V_C-V_{TH})=LWC_{ox}V_{od}$

(L: The effective channel length;
$C_{ox}W$: The total capacitance per unit length;
V_{TH}: The threshold voltage of M_3.)

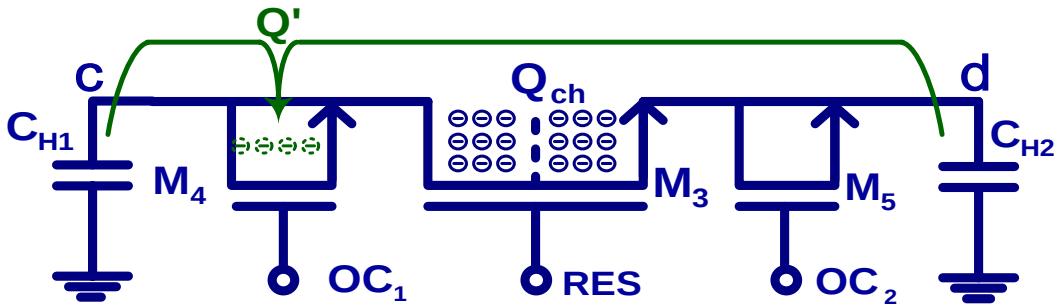
– Source-Drain connected transistors M_4, M_5 work as offset control transistors.

– Length of transistors $L_{M4}=L_{M5}=L_{M3}$;
Width of transistors $W_{M4}=W_{M5}=1/2\ W_{M3}$

– Charge absorbed by M_4, M_5 has a dependency on the over drive voltage.

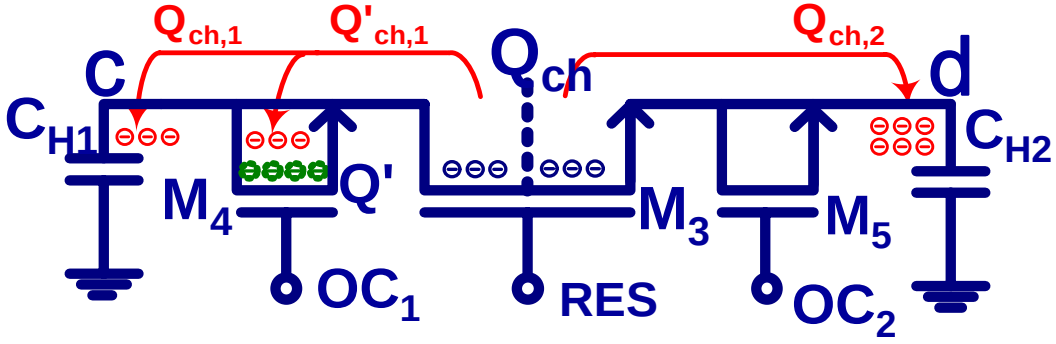
– Potentials at node c and d are influenced by the over drive voltage of M_4, M_5 at the moment M_3 turns off.

Mechanism of offset control by charge absorption



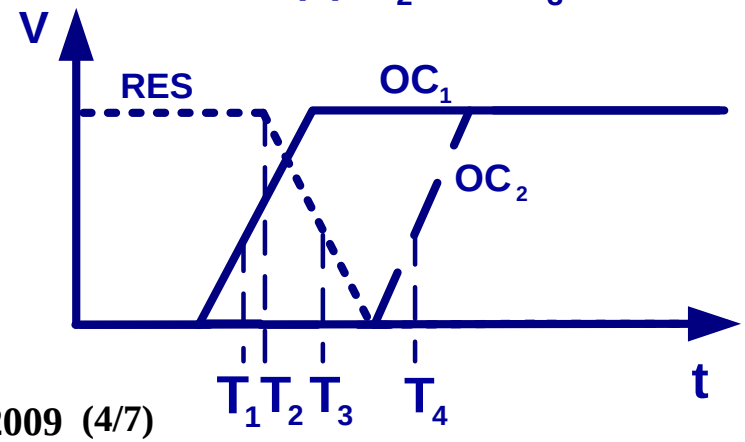
(a) $T_1 < t < T_2$

The charge absorption has approximately the same contribution to the potentials on nodes c and d.



(b) $T_2 < t < T_3$

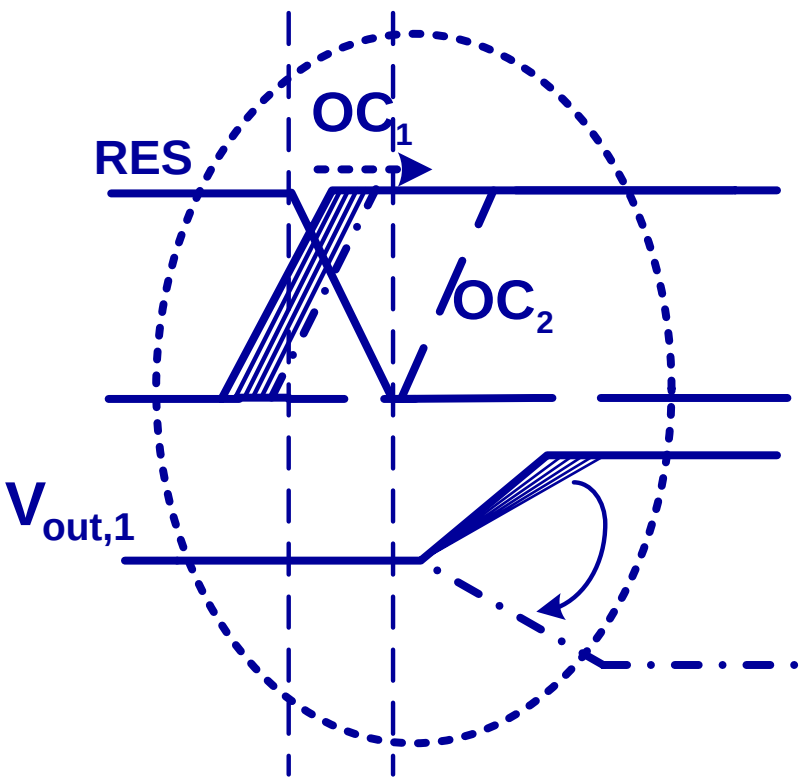
The charge absorption by M4 in this period contributes to generating a compensation voltage at the initial state of the latch regeneration.



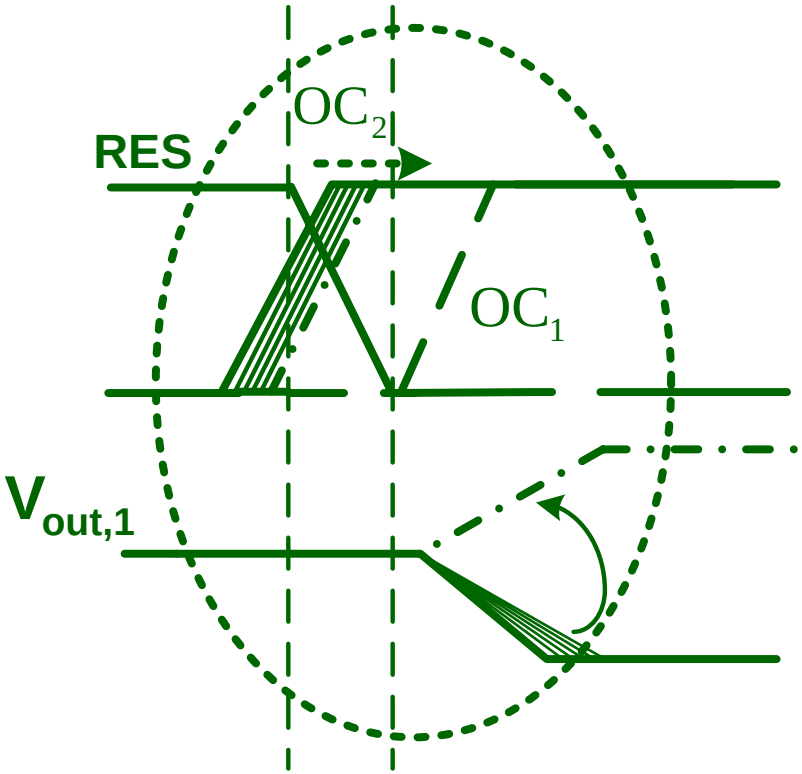
☆ $T_4 - T_3$ is large enough comparing to the regeneration time constant.

☆ The input signal along with the compensation voltage grows enough by the time when M5 starts to absorb charge from C_{H2} on node d.

Timing diagram of clock, offset control and output



In the case of positive offset



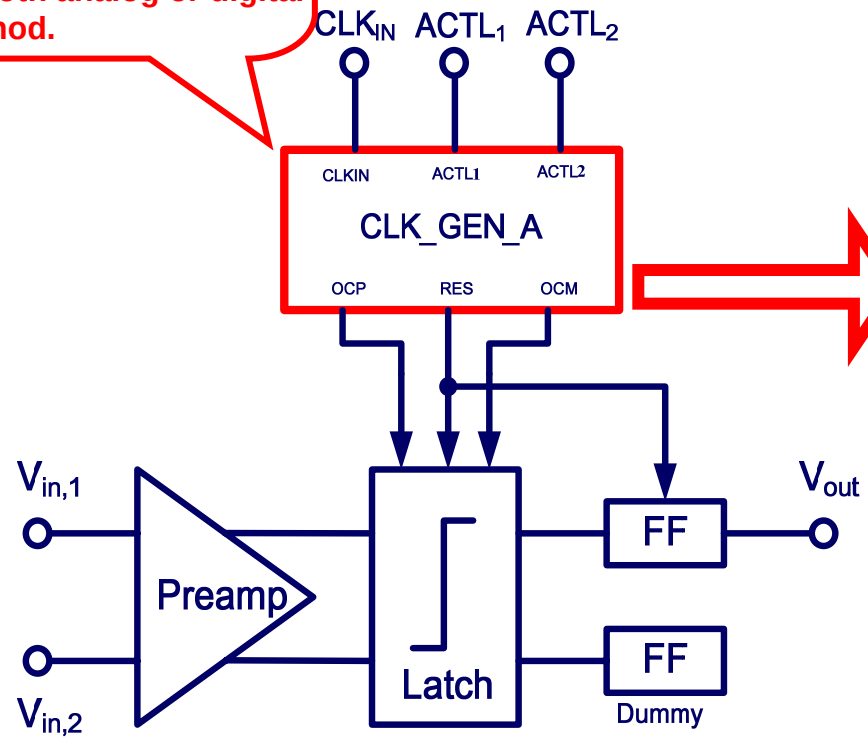
In the case of negative offset

The timing of signals OC1 and OC2 for offset control should be adjusted in time Domain in order to let two transistors M4 and M5 switch an appropriate manner to allocate the charge injected by M3 between nodes c and d so as to control the offset.

Circuits Implementation

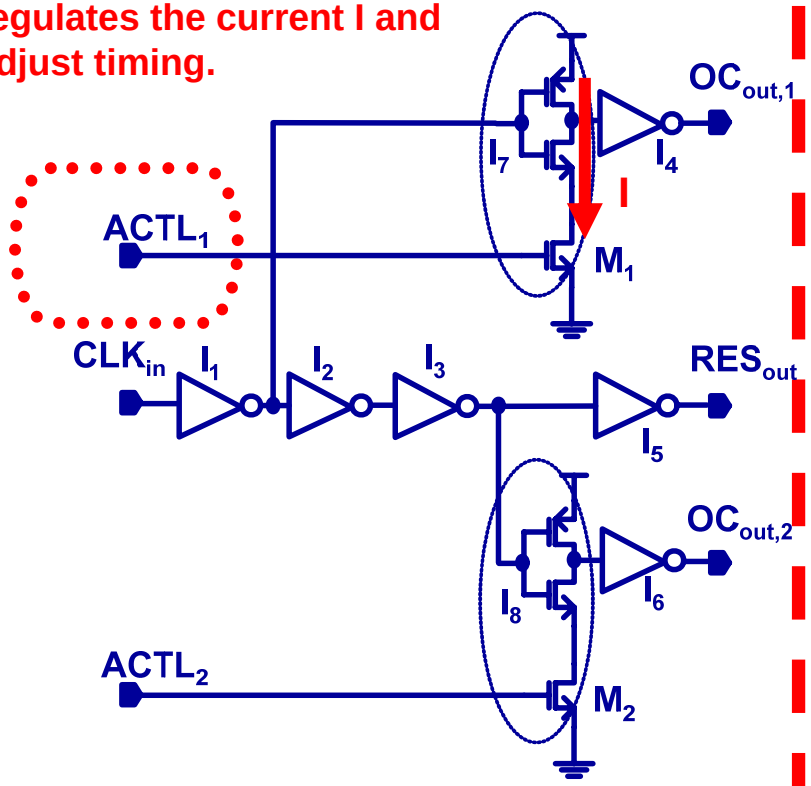
☆ Adjust timing among RES, OC_2 and OC_1;

☆ Can be implemented by both analog or digital method.



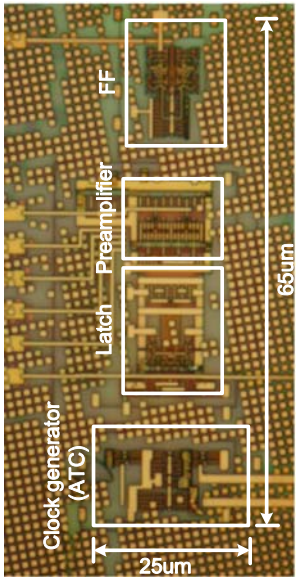
Top level diagram of comparator with offset control by Analog-to-Timing Convertor

Analog control signal $ACTL_1$ regulates the current I and adjust timing.

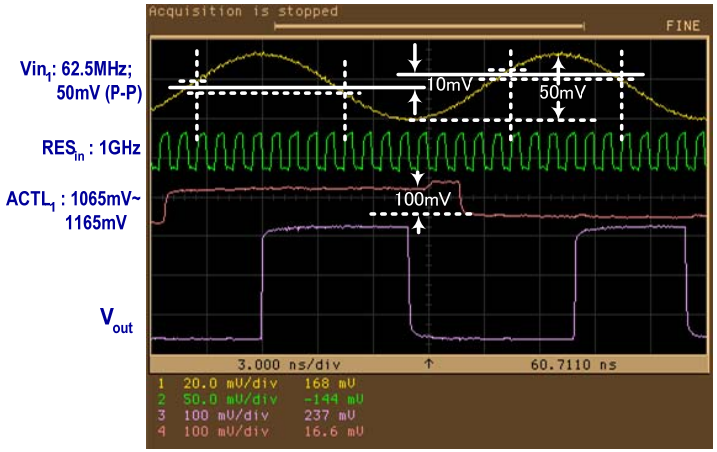


Clock Generator (Analog-to-Timing Convertor)

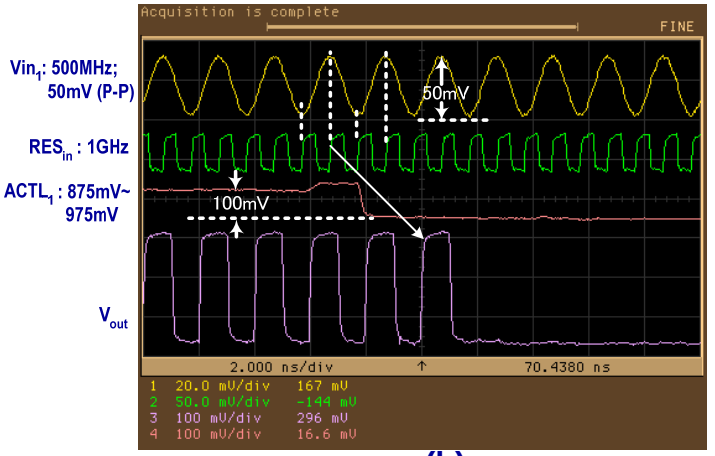
Chip Implementation and measurement results



65 nm CMOS process;
Area: 25 x 65 μm^2 .



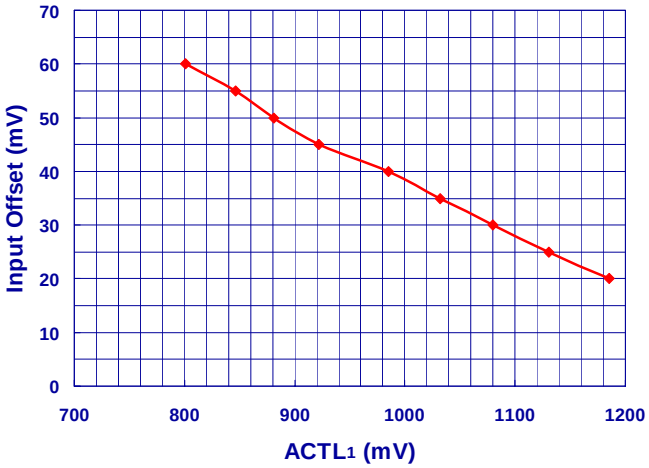
(a)



(b)

– Threshold level of the comparator response at 1 GS/s with 1.2V power supply;
– $ACTL_1$ is controlled with a 100 mV gap;
– An offset of 10 mV is controlled by 100 mV of $ACTL_1$ variation.

Response with a 500 MHz analog input frequency, synchronized to the 1 GHz clock.



☆ 1mV offset can be controlled by 10 mV of ACTL1.

☆ The controllable range and resolution is well balanced to control several tens of mV offset with mV order accuracy.

☆ The control ratio: $\Delta Voff / \Delta ACTL1 = 0.104$.