ASP-DAC 2009
University LSI Design Contest

Circuit Design using Stripe-Shaped PMELA TFT on Glass

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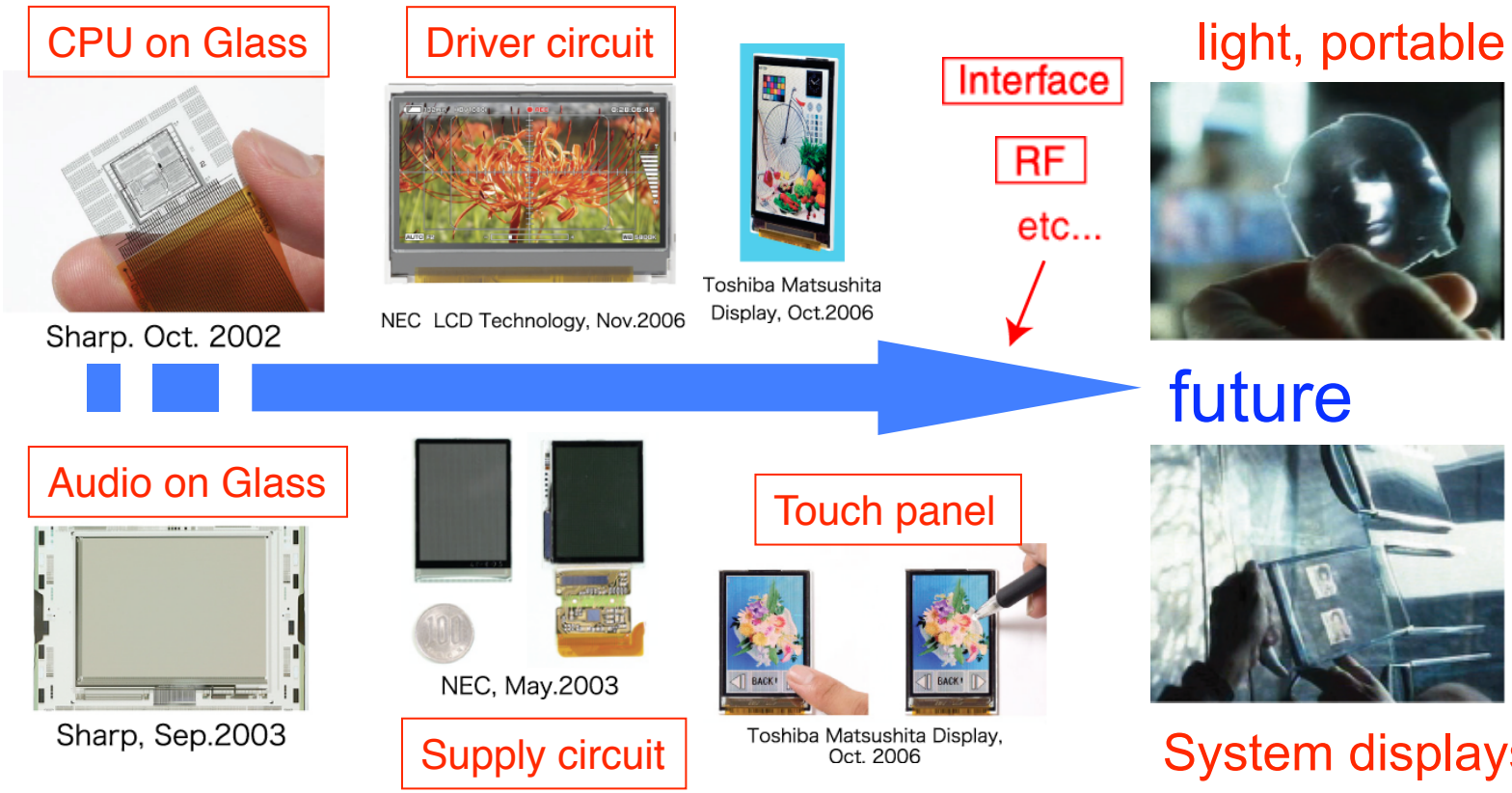
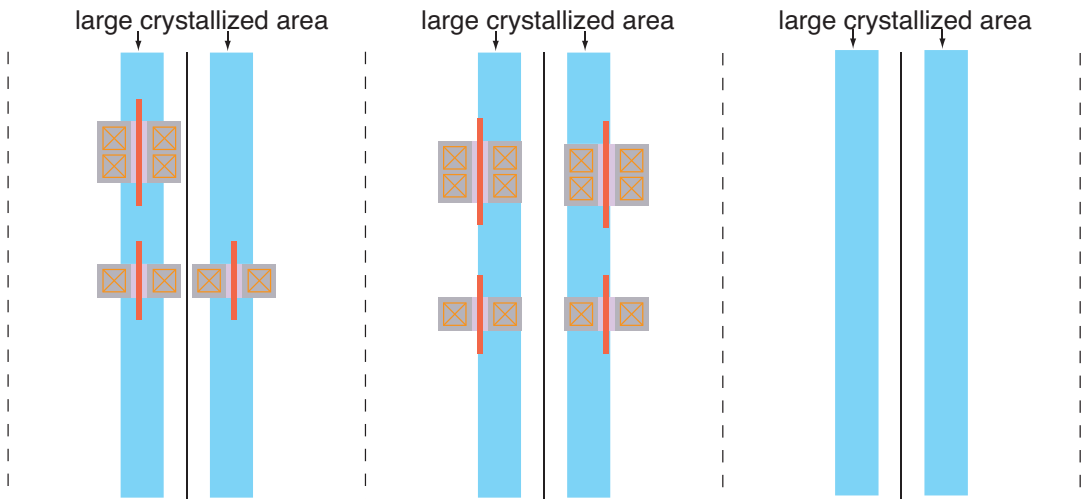
Background

- System-on-Glass (SOG)
  - Integrate the peripheral functions on glass substrate

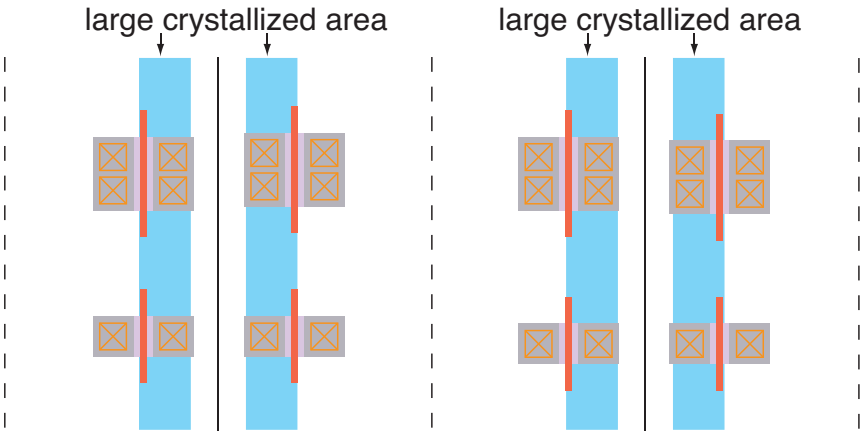


PMELA method

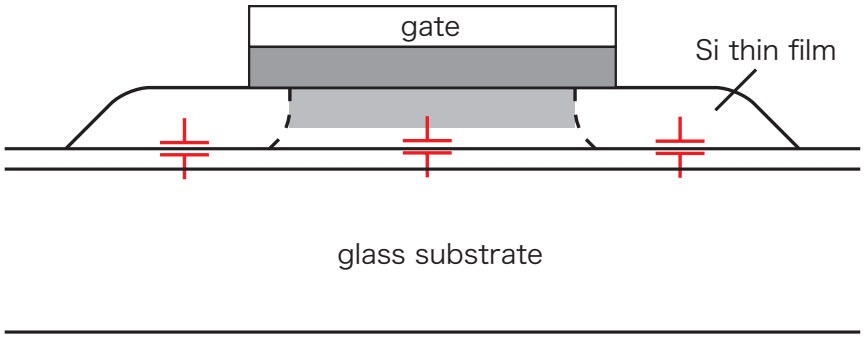
- Promising technique to realize SOG
  - Compatible with conventional TFT processes
  - Grow large Si grains with position control
- Large Si grains are formed periodically
  - Designers need to place TFTs on the areas



Main issues and targets



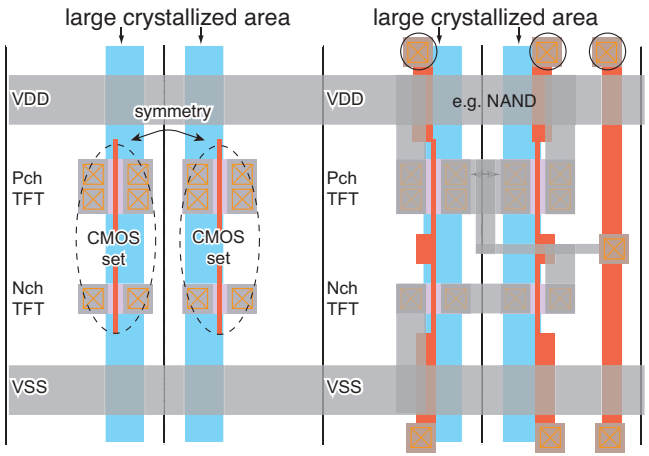
<PMELA process>
Have to place TFTs periodically



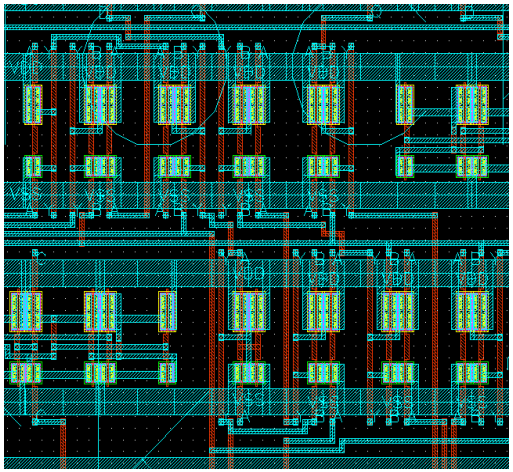
<Glass substrate>
Smaller ground capacitances
Than Si substrate

- Develop a design environment for automatically placing TFTs periodically on large Si grain areas
- Ground/parasitic capacitance modeling for post-layout simulation

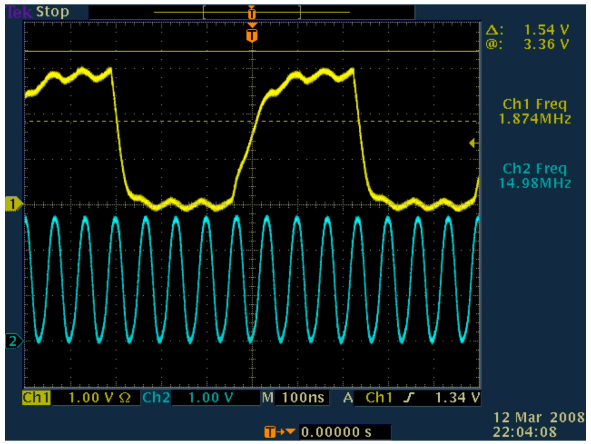
Placing TFTs periodically



<standard cell's layout>



<after place and route>

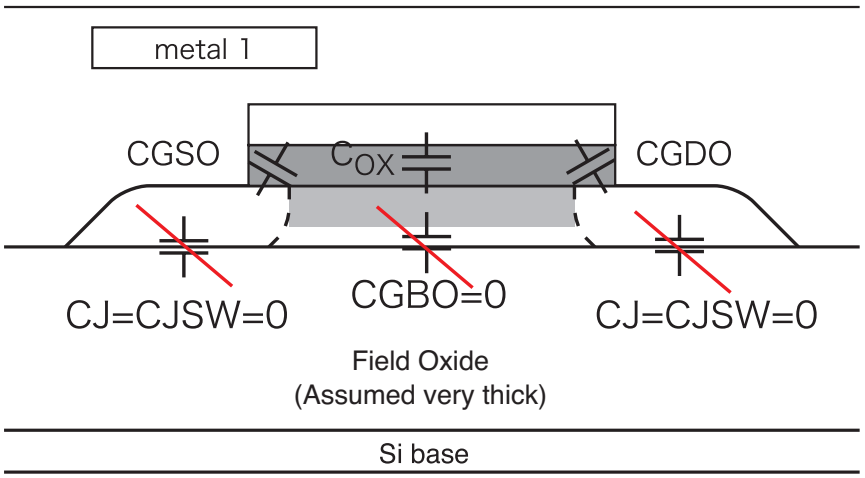


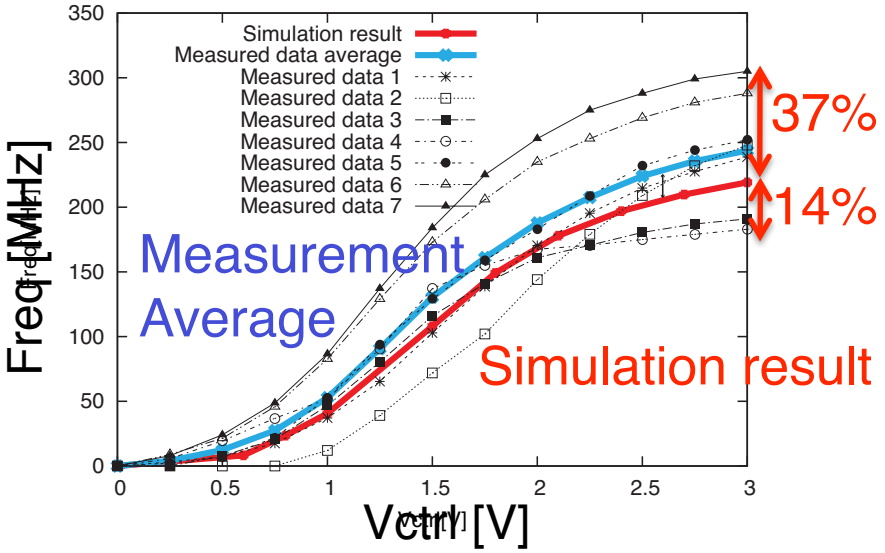
<successfully worked>

- Large crystallized Si area : 32um pitch
  - Standard cell's unit cell width are also designed as 32um
  - Poly for vertical, Metal 1 for horizontal wiring
  - Pins are placed above/below the Power/Gnd lines

⇨ TFTs are successfully placed on the large crystallized area

Simulation vs Measurement results





- Assumed the field oxide is very thick
- VCOs' measurement results
  - Error: < 70% (~1.5V), < 40% (~3V) (VDD=3V)
  - Averaged data : error is less than 15%
  - ⇨ The developed simulation environment is enough accurate for digital circuit design

Our Design is presented at poster session 1D-8.

Thank you.