HKUST Department of Electronic and Computer Engineering
The Hong Kong University of Science and Technology

# Low Energy Level Converter Design for Sub-$V_{th}$ Logics

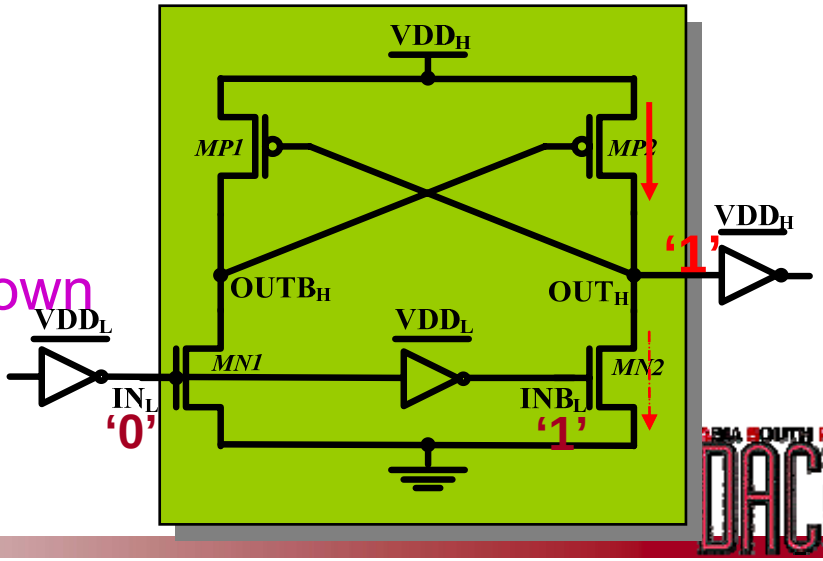
**Authors: Hui Shao and Chi-Ying Tsui**

Department of Electronic and Computer Engineering
The Hong Kong University of Science and Technology
Hong Kong SAR., P. R. China

ASIA SOUTH PACIFIC DESIGN AUTOMATION CONFERENCE

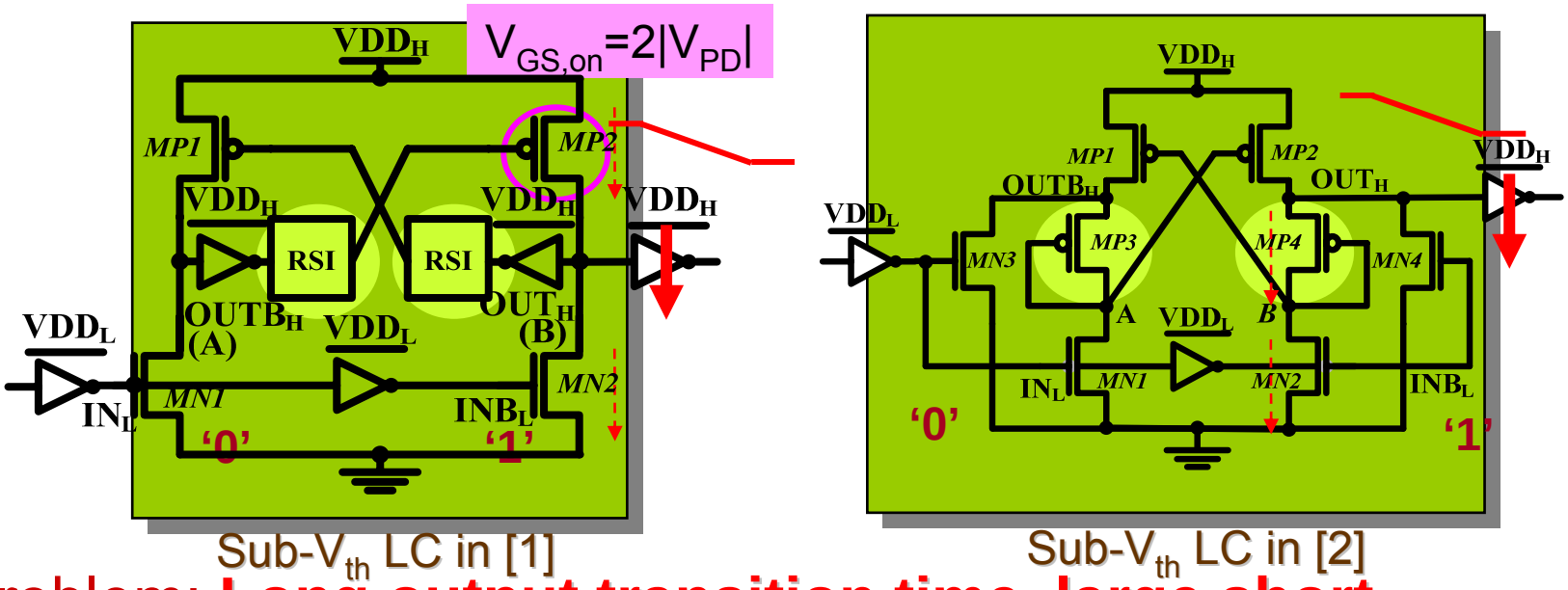
# Introduction

- Sub-$V_{th}$ logic operations can reduce the circuit power consumption dramatically
- Voltage difference between different voltage domains
  - Level converter (LC) is needed
    - > Sub-$V_{th}$ digital core <-> I/O interface
    - > Sub-$V_{th}$ digital core <-> analogue blocks …
- Conventional LC can not operate for sub-$V_{th}$ input signal
  - NMOS sub-$V_{th}$ conducting current cannot overcome the PMOS current
  - Output cannot be pulled down
  - Positive feedback cannot be triggered



# Previous Sub-$V_{th}$ LC Designs

- Limit the PMOS current so that the NMOS sub-$V_{th}$ conducting current can trigger the positive feedback
  - LC in [1]: RSI to limit the PMOS $|V_{GS}|$ voltage
  - LC in [2]: PMOS diodes to limit the PMOS pull up strength

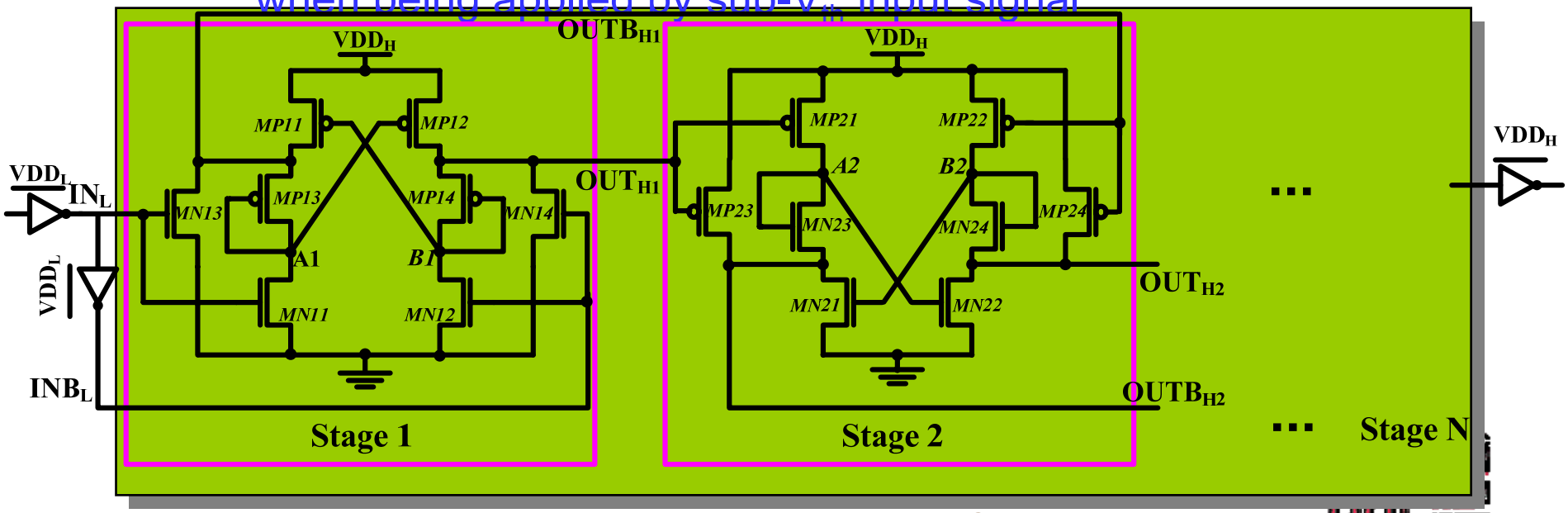



- Problem: **Long output transition time, large short circuit current through output logics**


[1] I. J. Chang, et al., "Robust level converter design for sub-threshold logic", ISLPED'06
[2] H. Shao, et al., "A robust, input voltage adaptive and low energy consumption level converter for sub-threshold logic", ESSCIRC'07

# Proposed Multi-stage Sub-$V_{th}$ LC

- Circuit structure:
  - Odd stage: previously proposed sub-$V_{th}$ LC in [2]
    - > Output '0'→'1' transition is always earlier than '1' to '0' transition when being applied by sub-$V_{th}$ input signal
  - Even stage: sub-$V_{th}$ LC with upside down connections
    - > Output '1'→'0' transition is always earlier than '0' to '1' transition when being applied by sub-$V_{th}$ input signal




Proposed multi-stage sub-$V_{th}$ LC

# Operation of Multi-stage Sub-$V_{th}$ LC

$t_0$: $IN_L$ changes from '0' to sub-$V_{th}$ '1'.

$t_1$: $OUT_{H1}$ goes firstly to $VDD_H$.

MP21,MP23 off, Short circuit current though the left branch of the 2nd stage is eliminated.

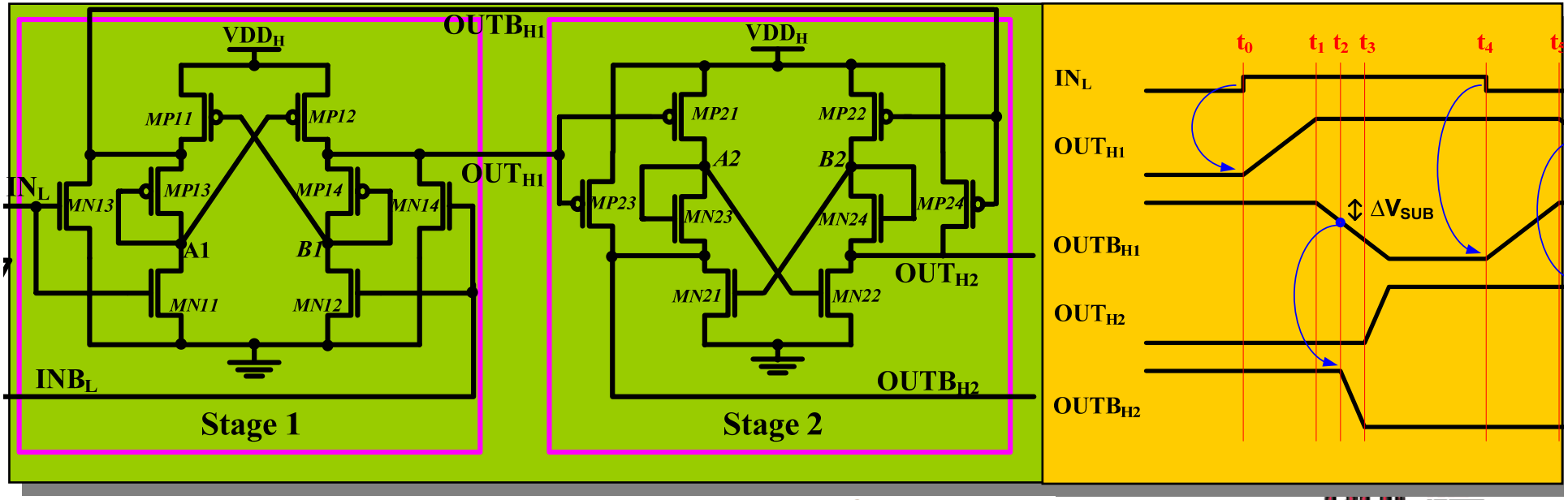
$t_2$: $OUTB_{H1}$ keeps being discharged which triggers the positive feedback in 2nd stage

$OUTB_{H2}$ is pulled down by the positive feedback in 2nd stage.

MN22 off. Short circuit current through the right branch of the 2nd stage is greatly reduced.

$t_3$: $OUTB_{H1}$ keeps decreasing.

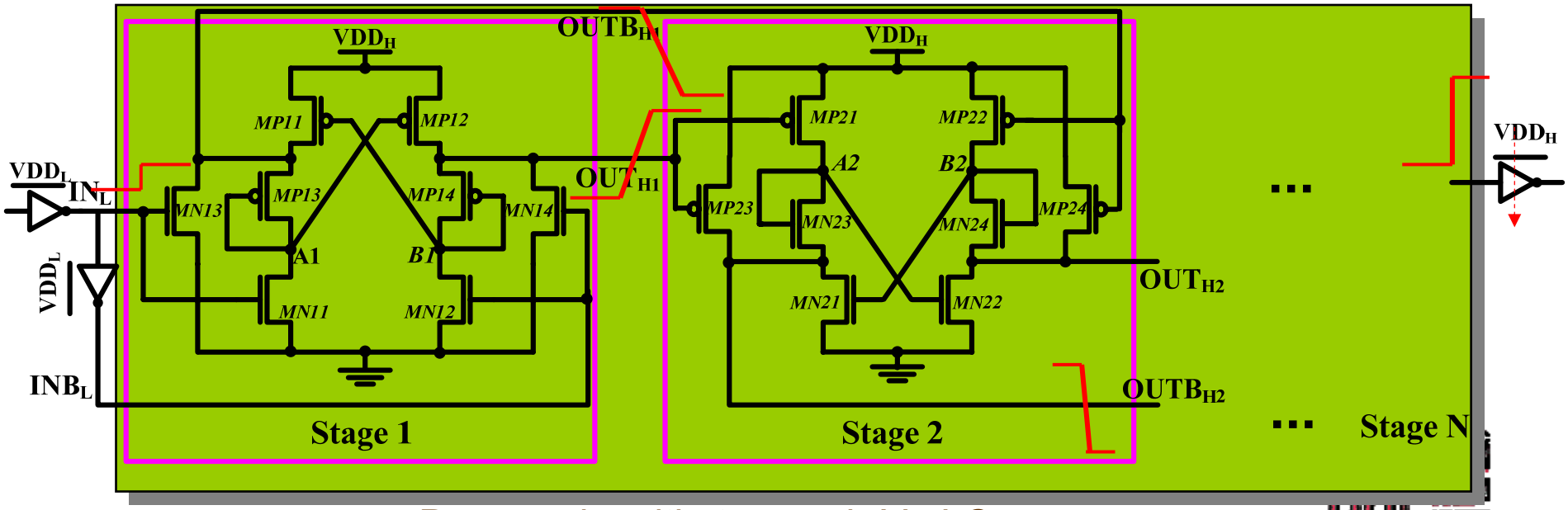
Output of the 2nd stage flips faster than that of 1st stage.




Proposed multi-stage sub-$V_{th}$ LC

# Operation of Multi-stage Sub-$V_{th}$ LC

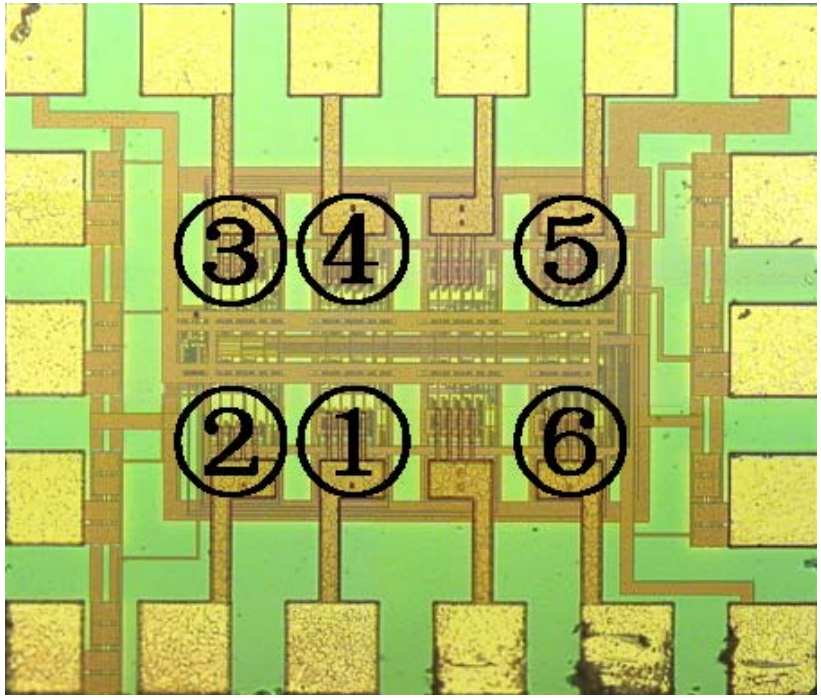
- Operation of the multi-stage LC
  - 1st stage: convert sub-$V_{th}$ signal to nominal high voltage
  - 2nd-Nth stages: Sharpen the LC output with positive feedback in each stages
  - The energy overhead due to multi-stage structure is small
- Circuit total energy reduction (incl. output logics) is reduced




Proposed multi-stage sub-$V_{th}$ LC

# Experimental Results

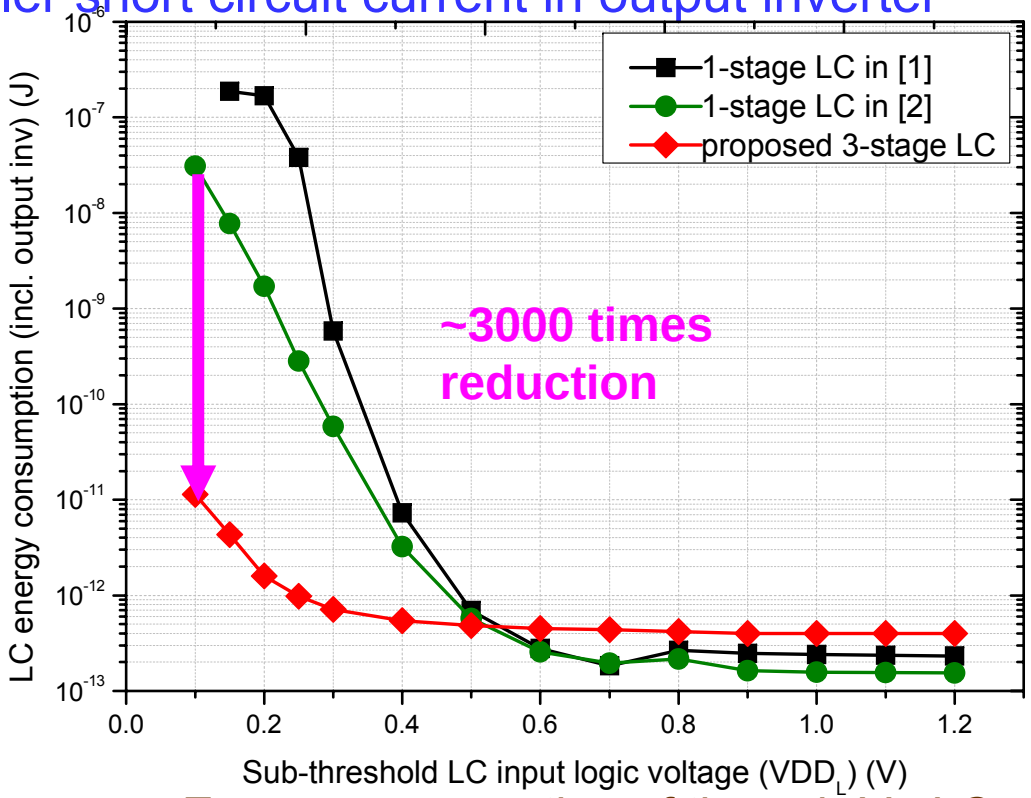
- Different sub-$V_{th}$ LCs were designed (TSMC 0.18 μm)
  - ►Same transistor sizes for different LC schemes
    - ①sub-$V_{th}$ LC in [1]
    - ②sub-$V_{th}$ LC in [2]
    - ④proposed 3-stage sub-$V_{th}$ LC




Test chip for different sub-$V_{th}$ LCs

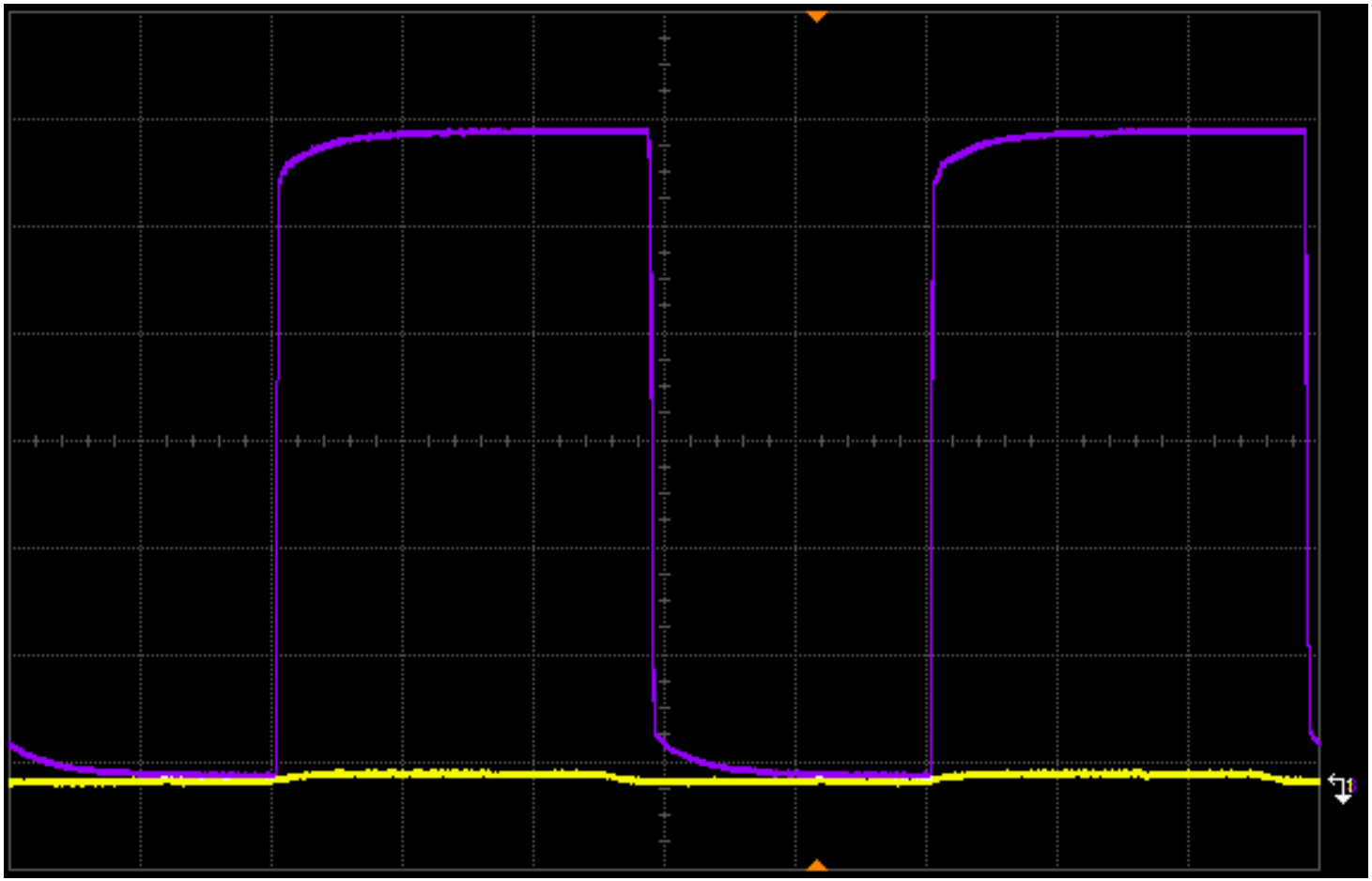
# Measurement Results

- A typical sized inverter is connect to LC output, and the short circuit energy consumption is included
  - ►Multi-stage LC has a lower energy than single stage LC
    - > Smaller short circuit current in output inverter




Energy consumption of the sub-$V_{th}$ LC

# Experimental Results



Input (100mV) and output (1.8V) waveforms of the proposed 3-stage sub-$V_{th}$ LC (measurement)