Flexible and Abstract Communication and Interconnect Modeling for MPSoC

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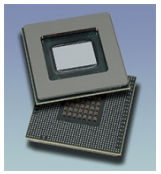
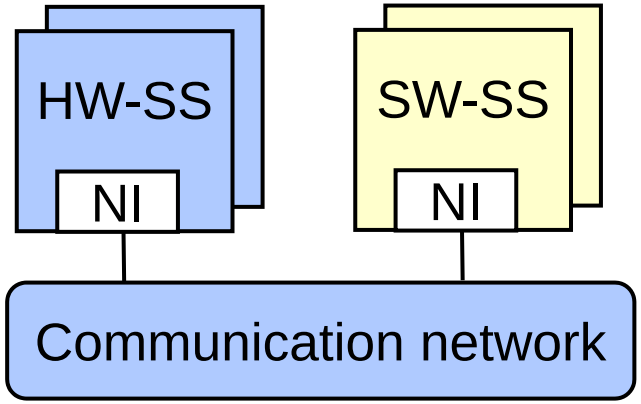
The MathWorks

Context

- Multiprocessor System-on-Chip (MPSoC) are required by current embedded systems
  - HW subsystems + SW subsystems
  - Complex communication network





MPSoC generic architecture

- **Programming Model: shared memory, message passing**
- **Blocking vs. Non-blocking**
- **Synchronous vs. Asynchronous**
- **Buffered vs. Un-buffered data transfer**
- **Communication buffer mapping**
- **Synchronization**
- **Type of interconnection: point-to-point, bus, Network-on-Chip (NoC)**

Motivation

- Problems:
  - Large set of parameters and communication design choices
    - Design space exploration to find the best communication architecture
  - Low level (cycle accurate) design space exploration is time consuming and requires too much effort
    - Early and High level exploration is required to reduce design time
    - Intermediate simulations to bridge the gap between functional and cycle accurate simulations
- Contribution:
  - High level communication models, that allow:
    - Early validation of the communication architecture through intermediate simulation steps
    - Exploration of the different communication buffer mapping and interconnect schemes

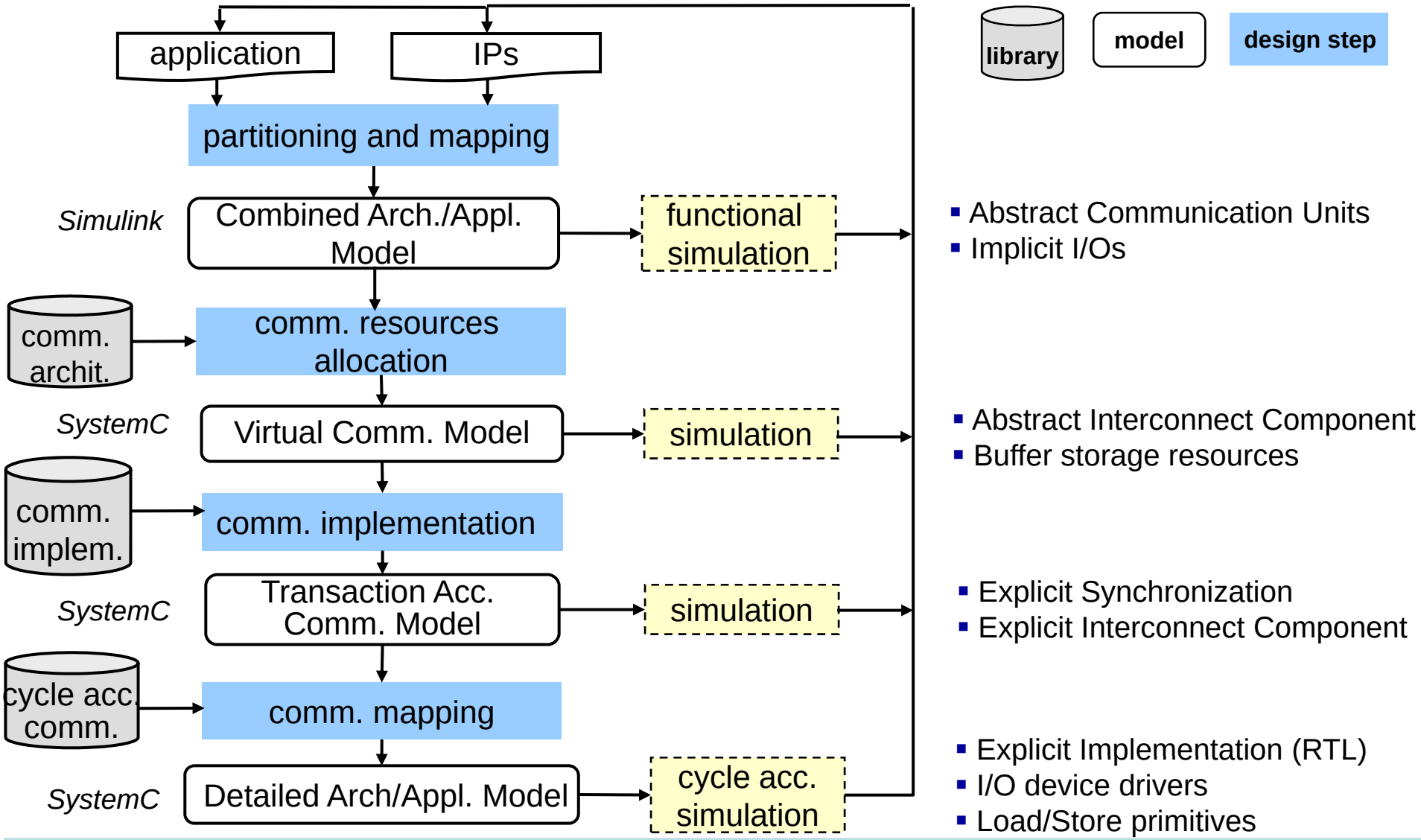
State of the Art

- Communication exploration and mapping tools:
  - Murali et al. “SUNMAP” automatic mapping tool of IP cores onto NoC
  - Xu et al. methodology to evaluate NoC architectures at low level
  - Dumitrascu et al. fast interconnect exploration: distributed memory server (DMS), AMBA and Octagon NoC
  - Shin et al. TLM generation from abstract input to refine the communication architecture
- Our proposal:
  - 2 high level communication models with automatic generation from Simulink for fast exploration of interconnect (bus, NoC) and communication mapping schemes

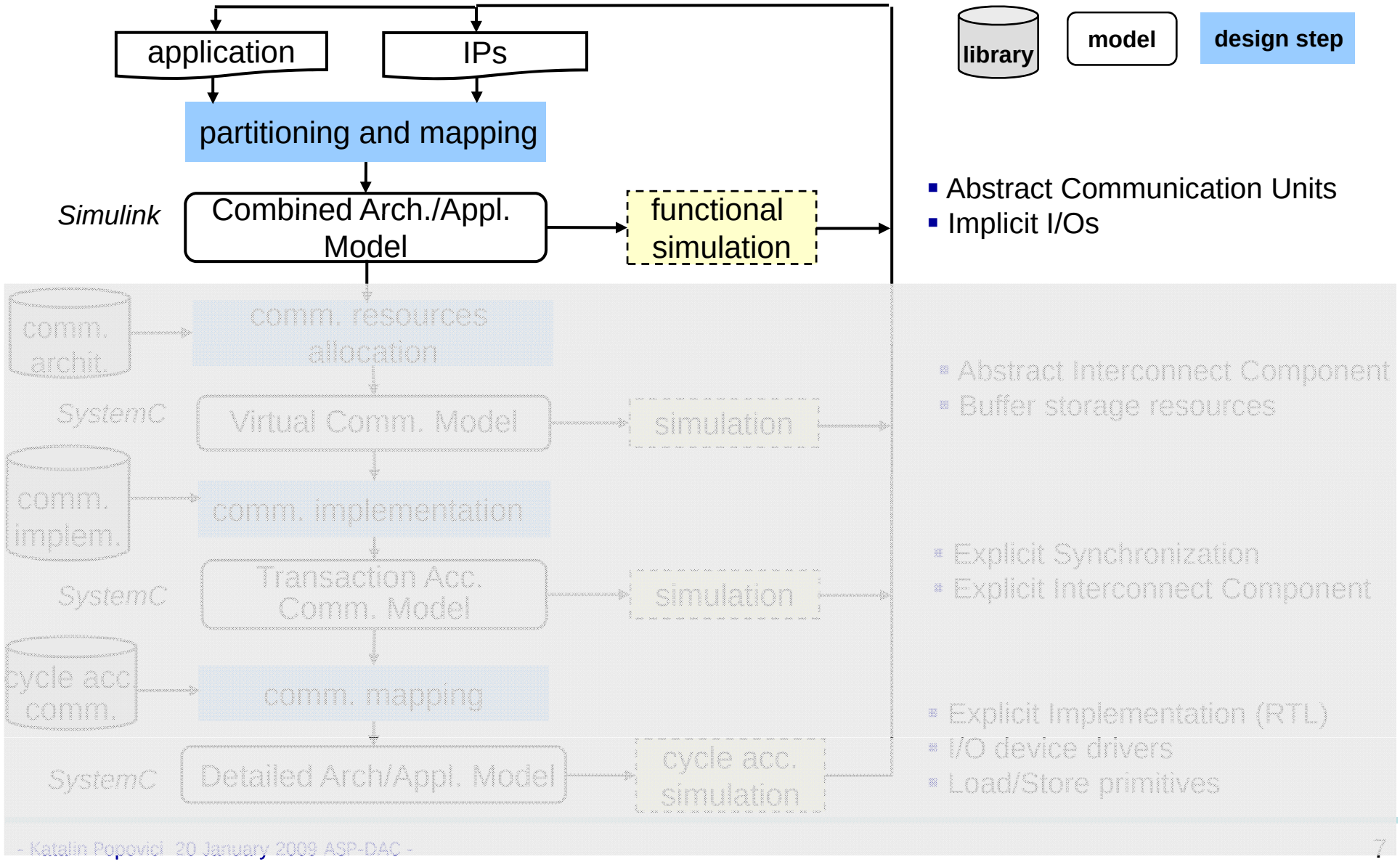
Outline

- **Communication modeling for MPSoC at different abstraction levels**
- Experiments with H.264 Encoder
- Conclusions

MPSoC Communication Modeling Abstraction Levels



MPSoC Communication Modeling Abstraction Levels



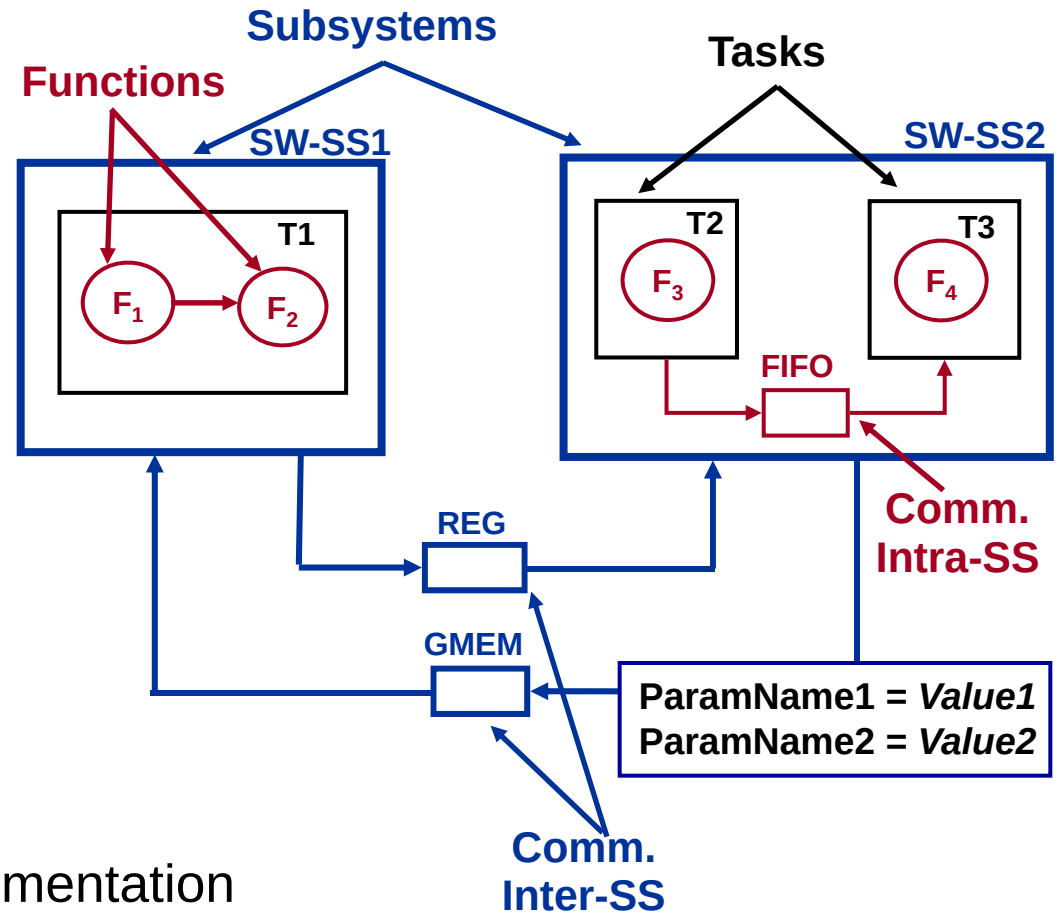
Combined Application/Architecture Model

- Captures application mapping on architecture

- Subsystem
  - Set of tasks

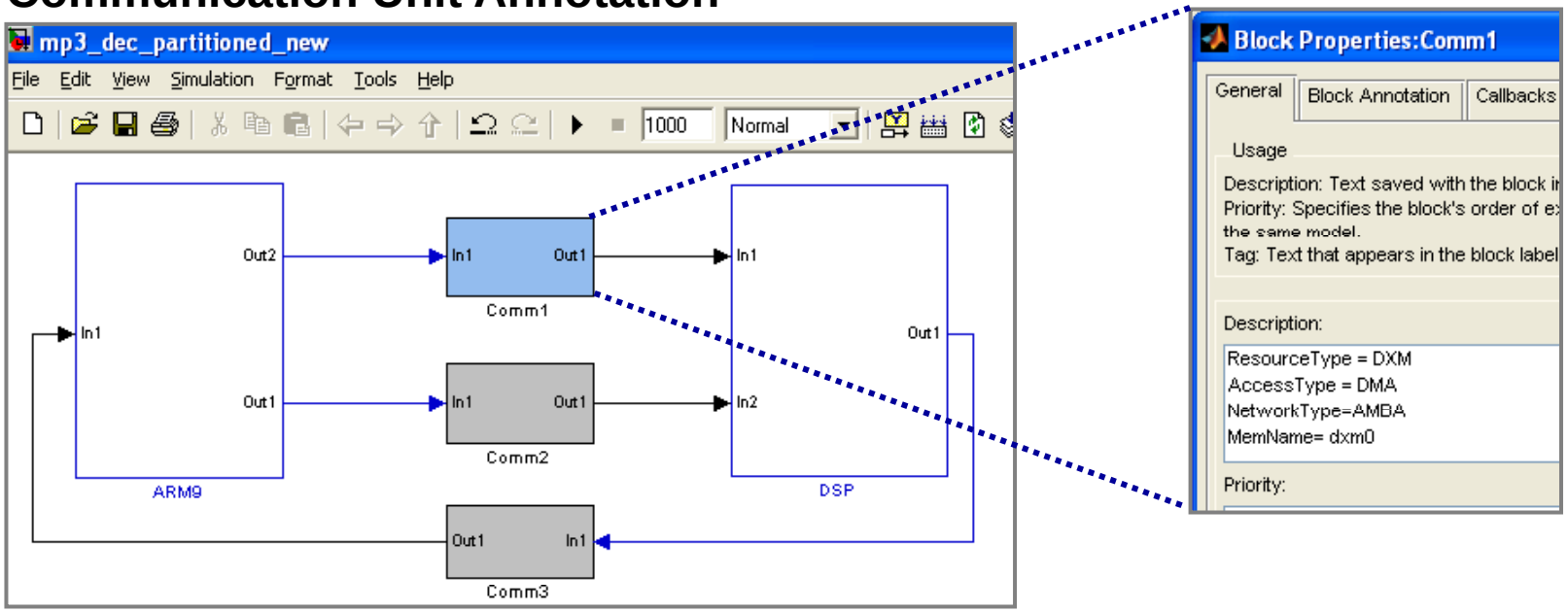
- Abstract communication types:
  - Intra-SS
  - Inter-SS

- Communication protocol:
  - Generic Simulink I/Os
  - Explicit annotation for implementation



Example of Combined Appl./Arch. in Simulink

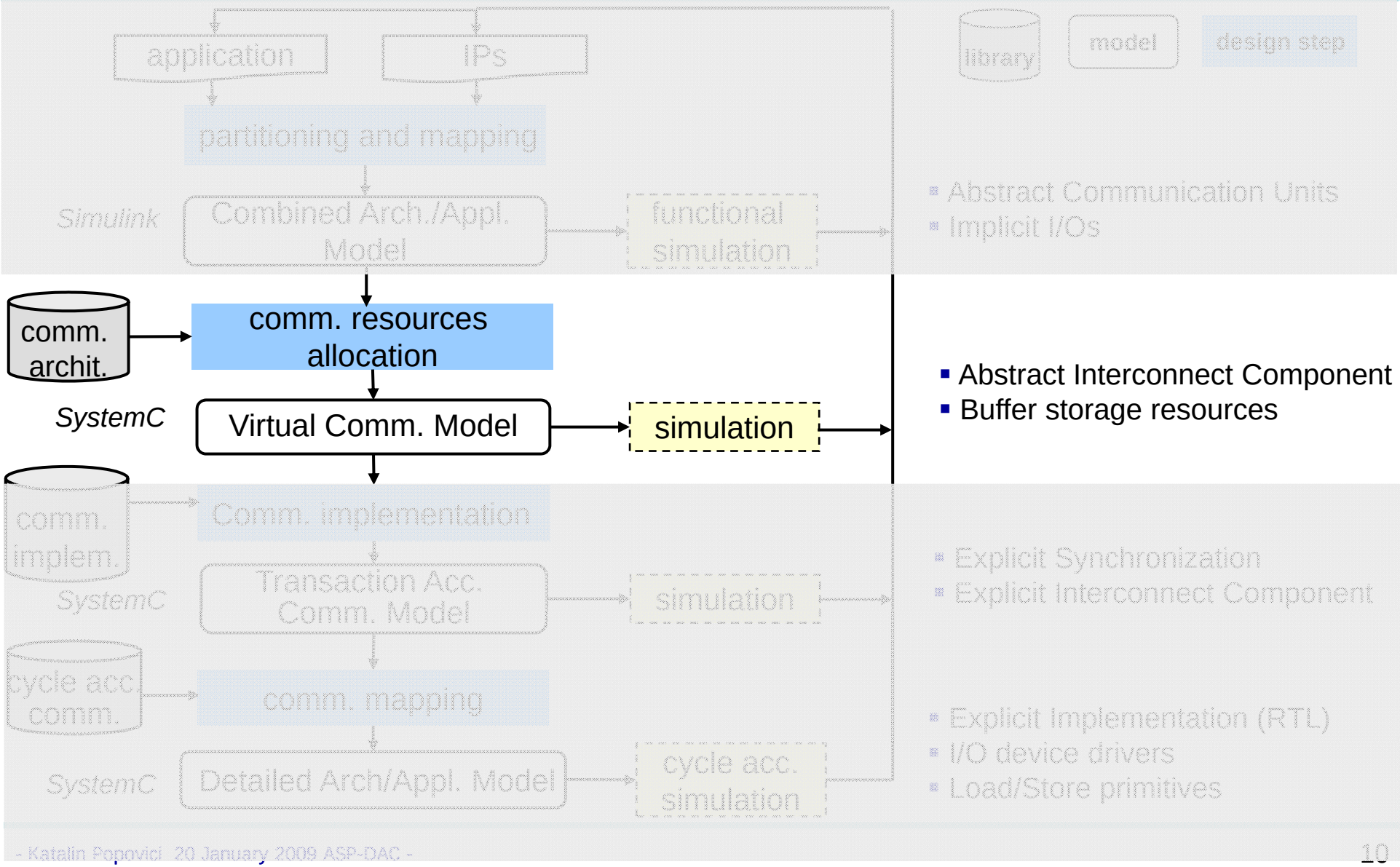
Communication Unit Annotation



- Communication units annotated with architecture parameters using *Block Properties*
- Communication Units are Simulink Signals
- Number of Comm. Units depends on Application

- Architecture parameters annotating the model:
  - ResourceType: FIFO, local/global memory
  - NetworkType: AMBA, Hermes NoC
  - AccessType: DMA, direct
  - MemName

MPSoC Communication Modeling Abstraction Levels



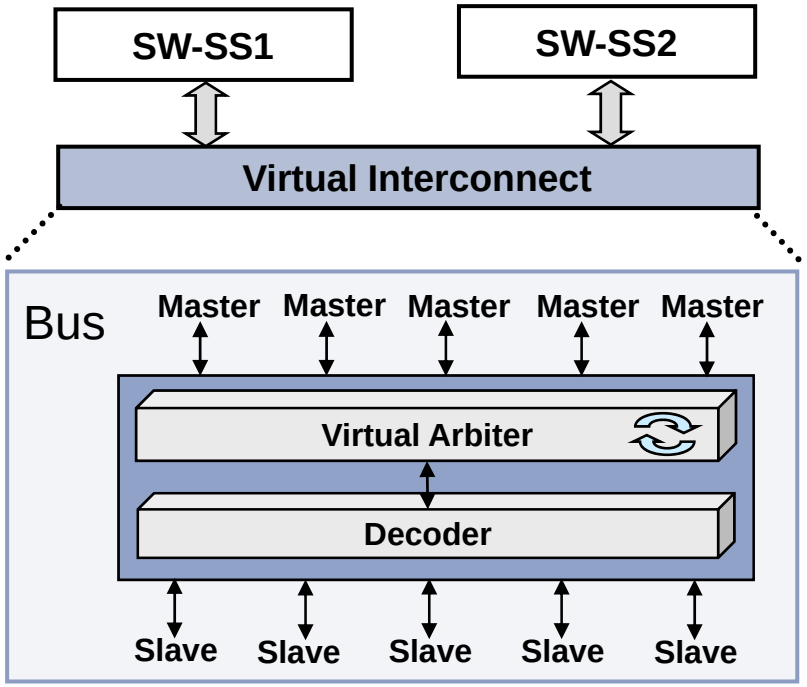
Virtual Communication and Interconnect Modeling

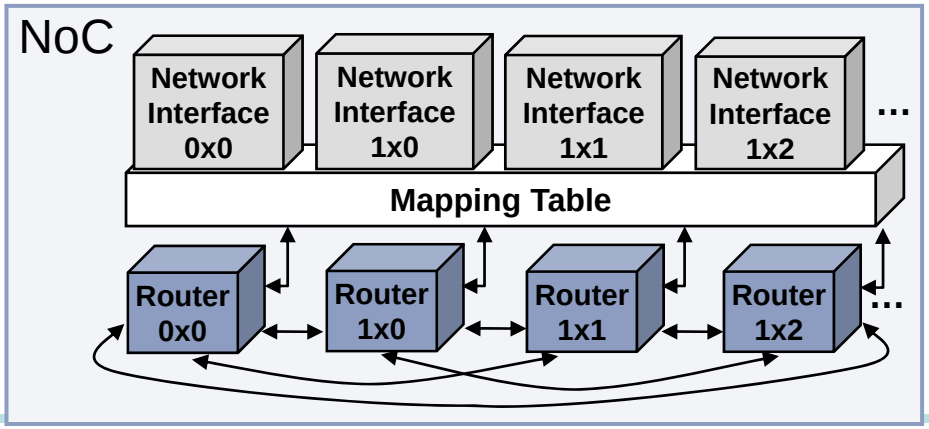
- SystemC TLM, message accurate model
- Interconnects abstract subsystems

- Inter-SS communication units partially mapped on resources
- Intra-SS communication units become software communication channels

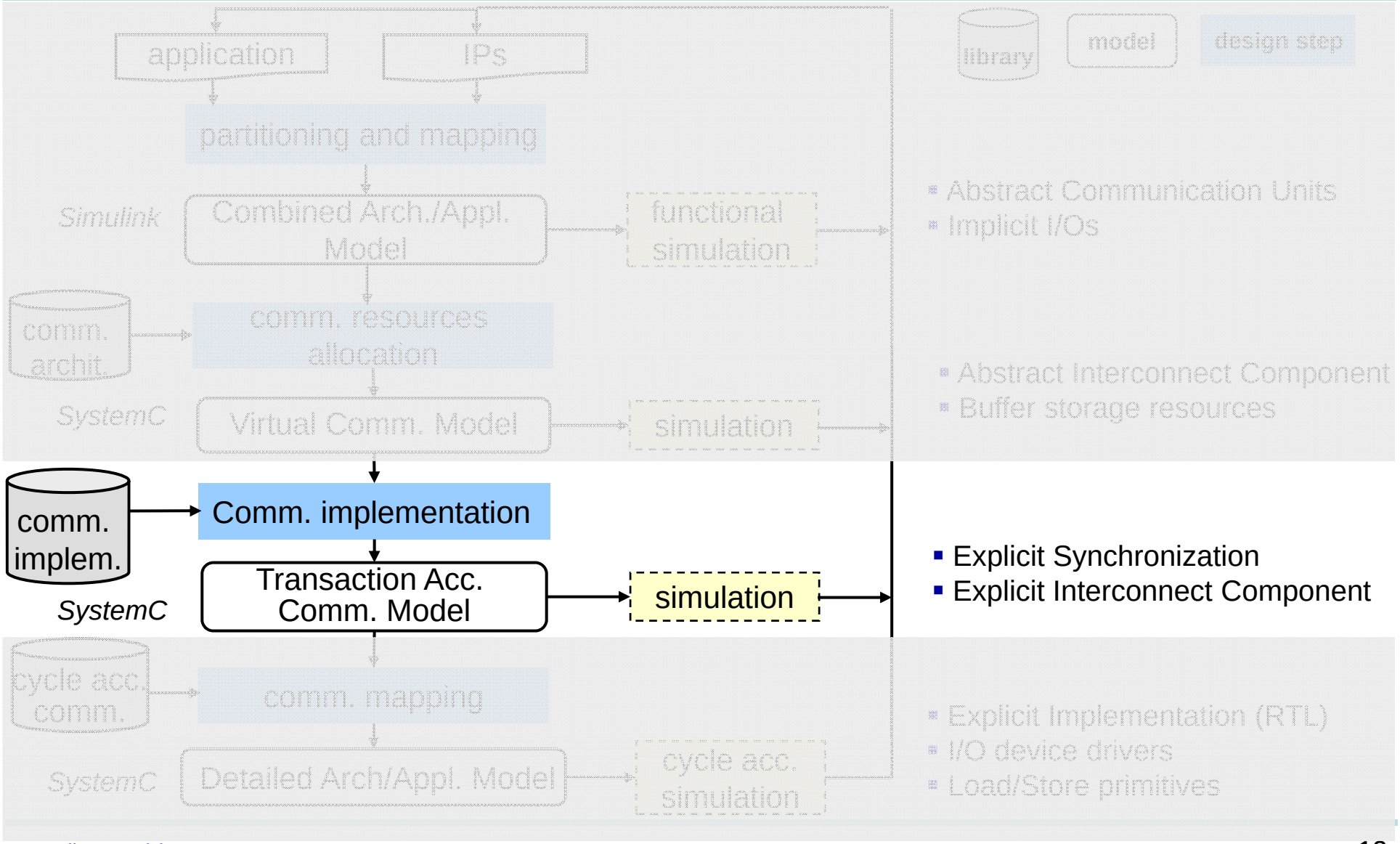
- Virtual interconnect component
  - **virtual bus**: virtual arbiter + address decoder
  - **virtual NoC**: NI, router, mapping table

  - parameterized, scalable, part of library
  - simulation: nb bytes exchanged



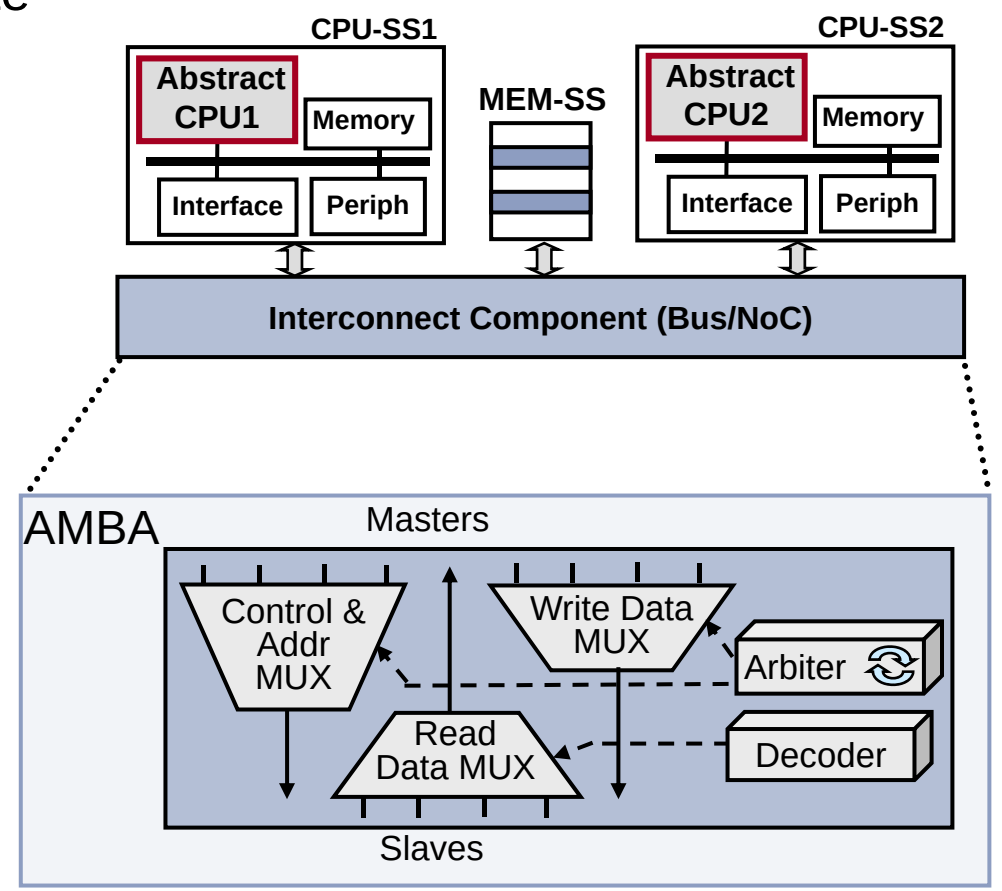


MPSoC Communication Modeling Abstraction Levels



Transaction Accurate Communication and Interconnect Modeling

- SystemC TLM, transaction accurate model
- Interconnects subsystems:
  - Detailed local architecture
  - Abstract CPU cores
- Inter-SS communication units fully mapped on explicit resources
- Explicit communication protocol & synchronization mechanism
- Explicit interconnect component
  - Bus: arbitration, burst mode
  - NoC: topology, routing algorithm, buffer size
  - Parameterized, scalable, part of a library
  - Simulation: conflicts in the bus, NoC congestion, routing requests

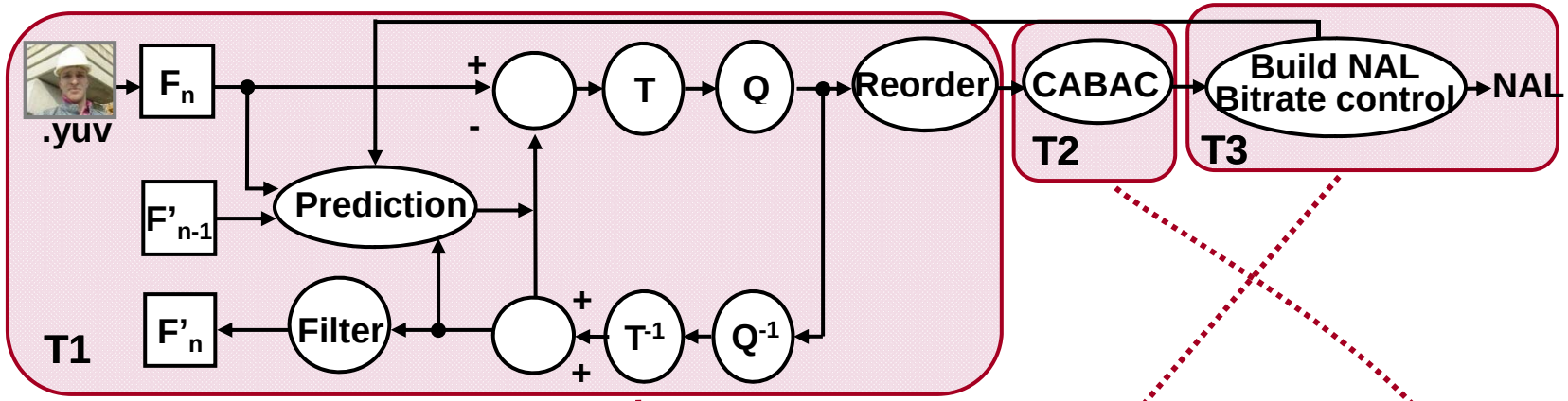


Outline

- Communication modeling for MPSoC at different abstraction levels
- **Experiments with H.264 Encoder**
- Conclusions

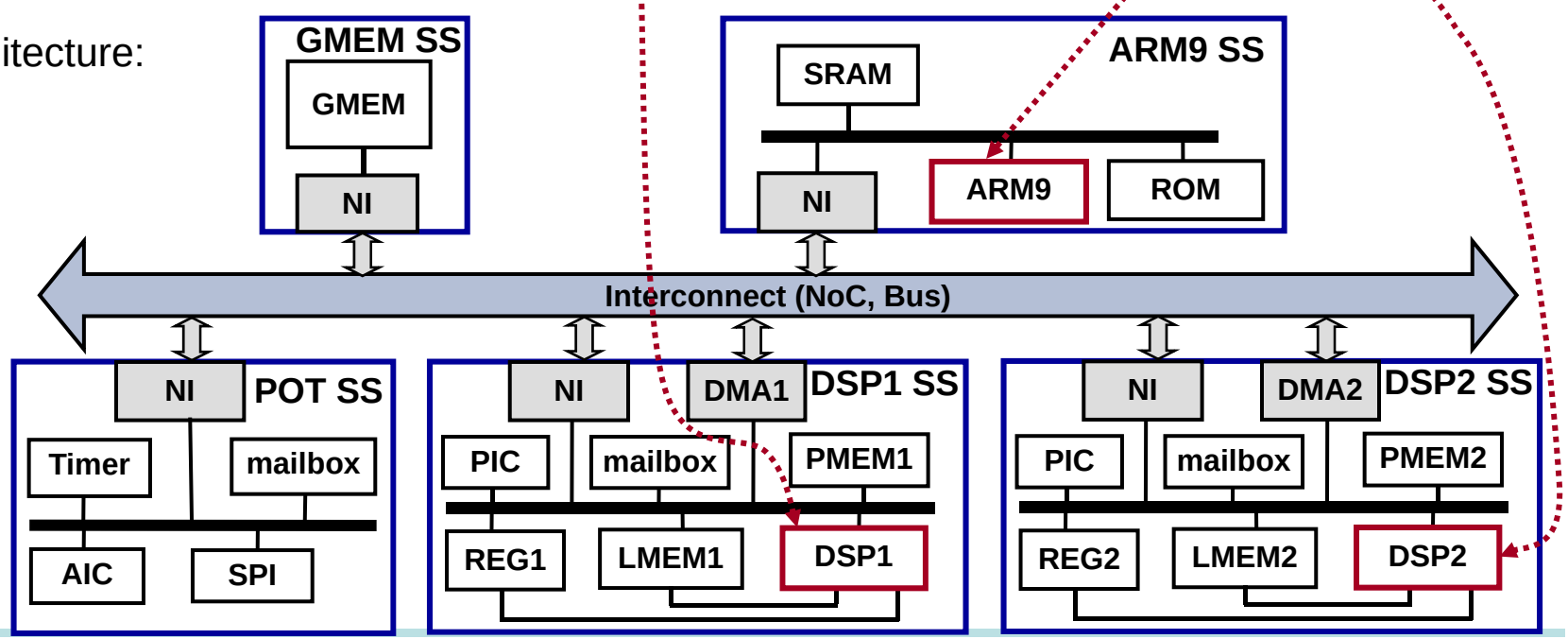
H.264 Encoder application

- Application Specification (Main Profile)



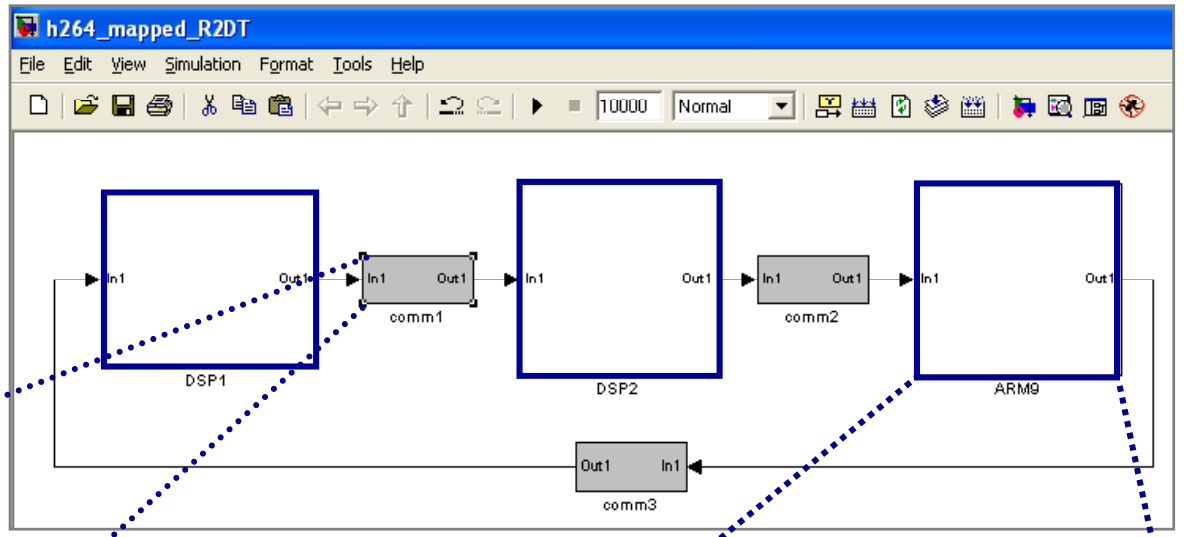
- Target Architecture:

1 ARM9-SS
2 DSP-SS
1 GMEM-SS
1 POT-SS
Interconnect

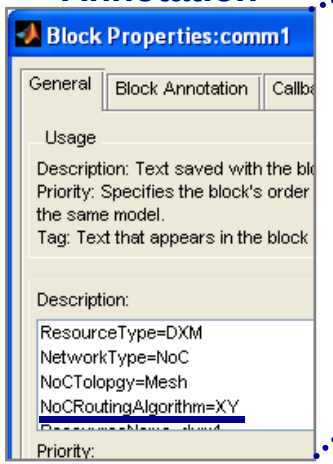


Combined Architecture/Application Model for H.264 Encoder in Simulink

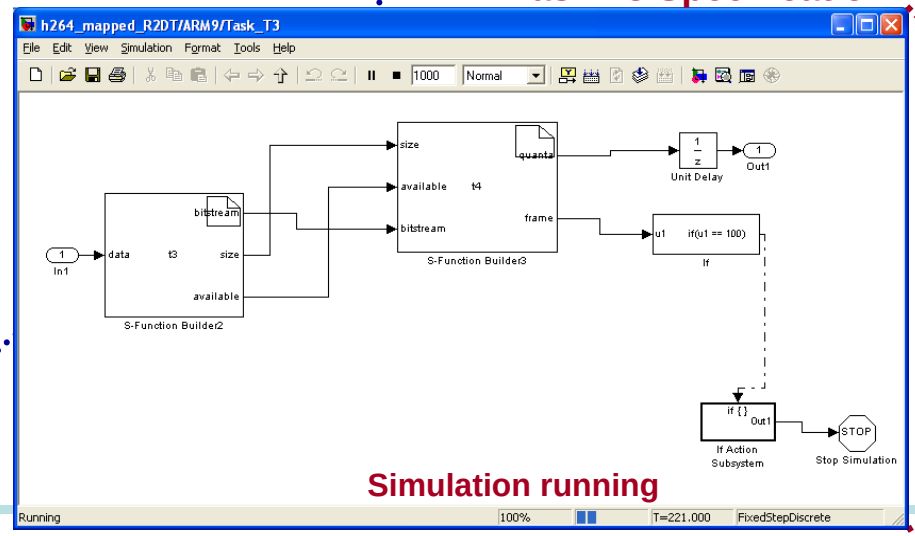
- 4 S-Functions
- **3 Inter-SS communication units**
- 10 frames QCIF YUV 420
- Simulation time: 30s on PC 1.73GHz, 1GBytes RAM



Parameters Annotation

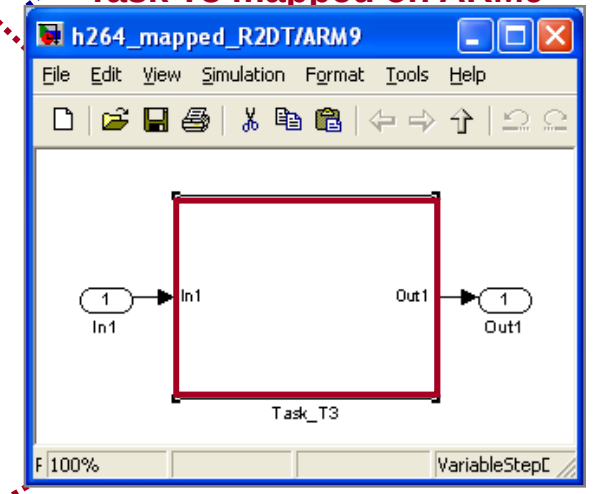


Task T3 Specification



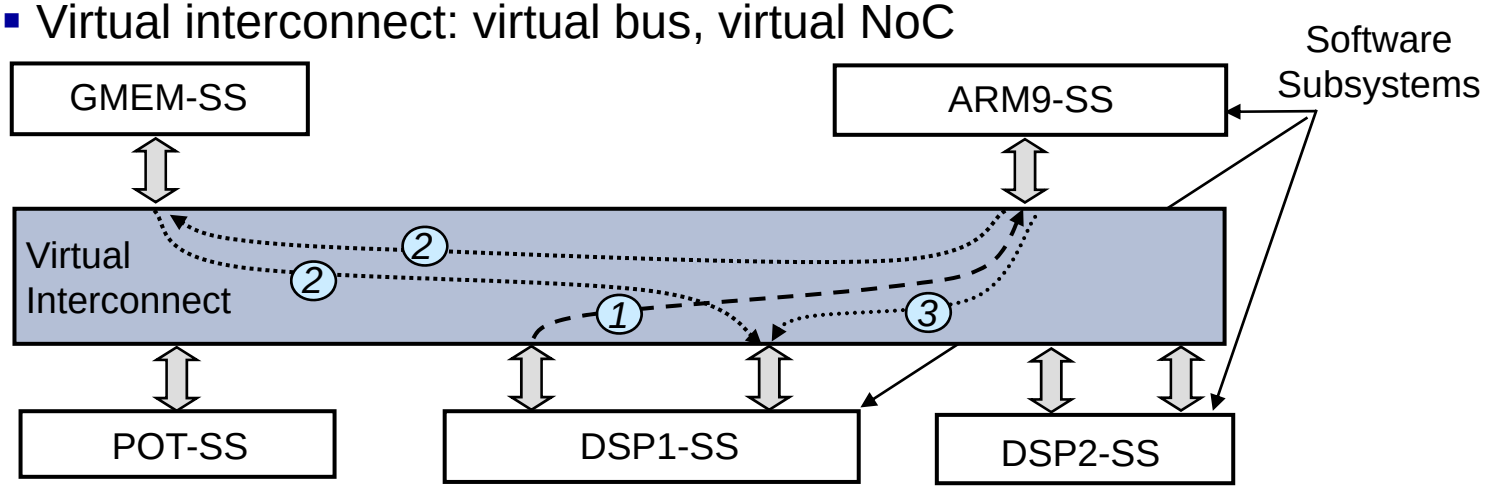
Simulation running

Task T3 mapped on ARM9

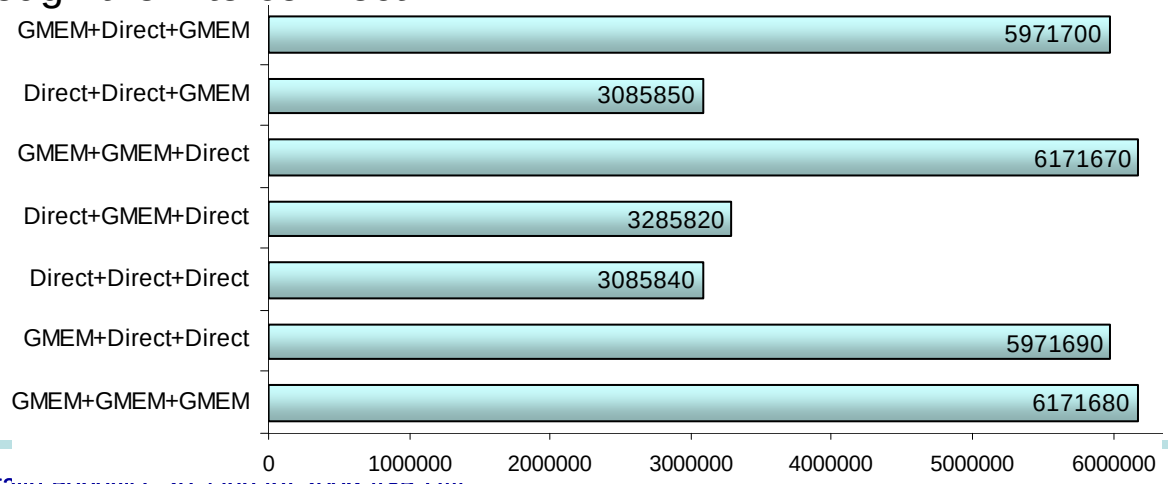


Virtual Communication Model for H.264

- Interconnects 5 abstract subsystems
- Virtual interconnect: virtual bus, virtual NoC



- 7 different mapping schemes of the 3 Inter-SS communication units: total Words transmitted through the Interconnect:

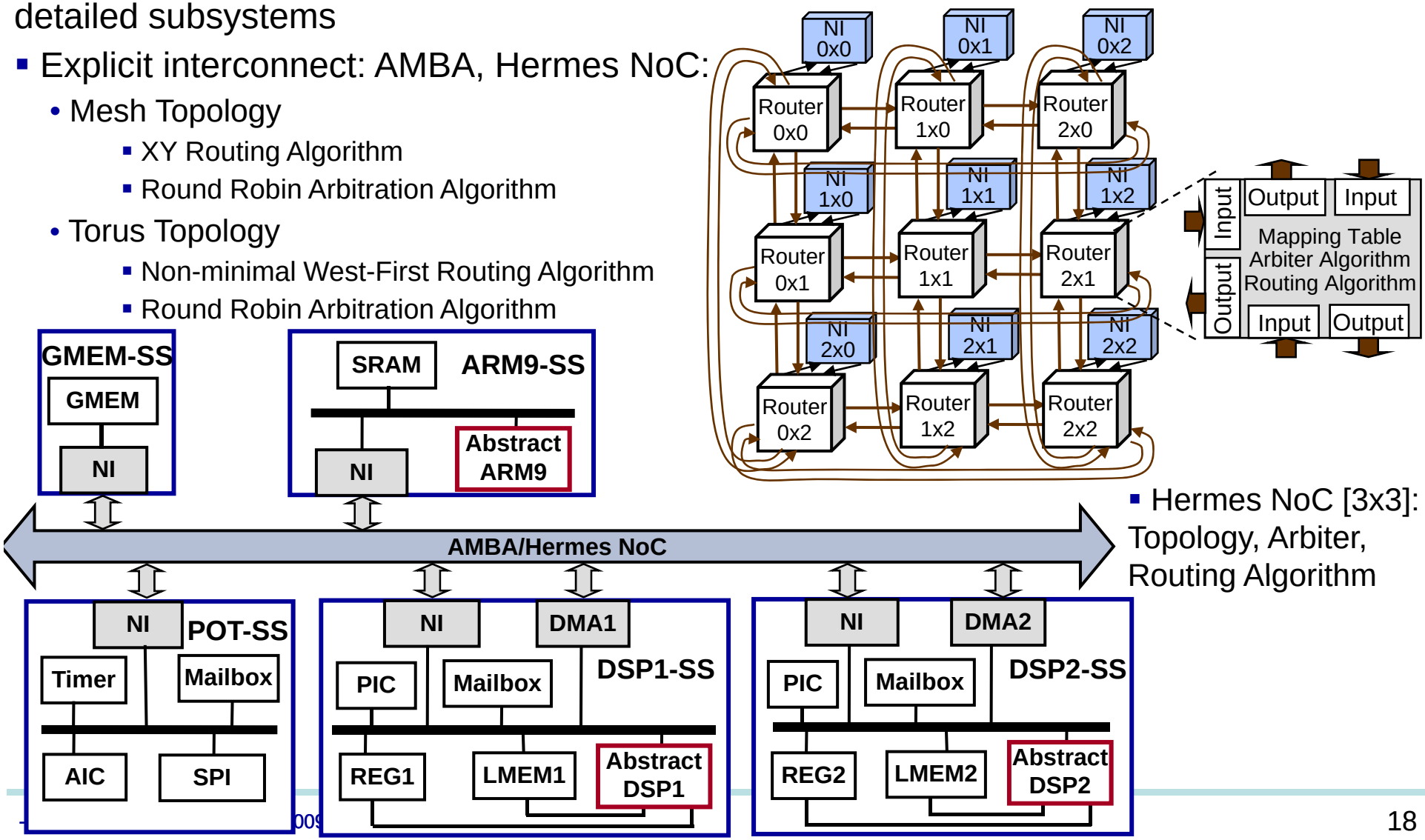


GMEM+GMEM+GMEM:

- simulation time: ~ 20s virtual bus, ~ 30s virtual NoC
- 58 conflicts in the virtual bus

Transaction Accurate Communication Model for H.264

- Full end-to-end communication path between detailed subsystems
- Explicit interconnect: AMBA, Hermes NoC:
  - Mesh Topology
    - XY Routing Algorithm
    - Round Robin Arbitration Algorithm
  - Torus Topology
    - Non-minimal West-First Routing Algorithm
    - Round Robin Arbitration Algorithm

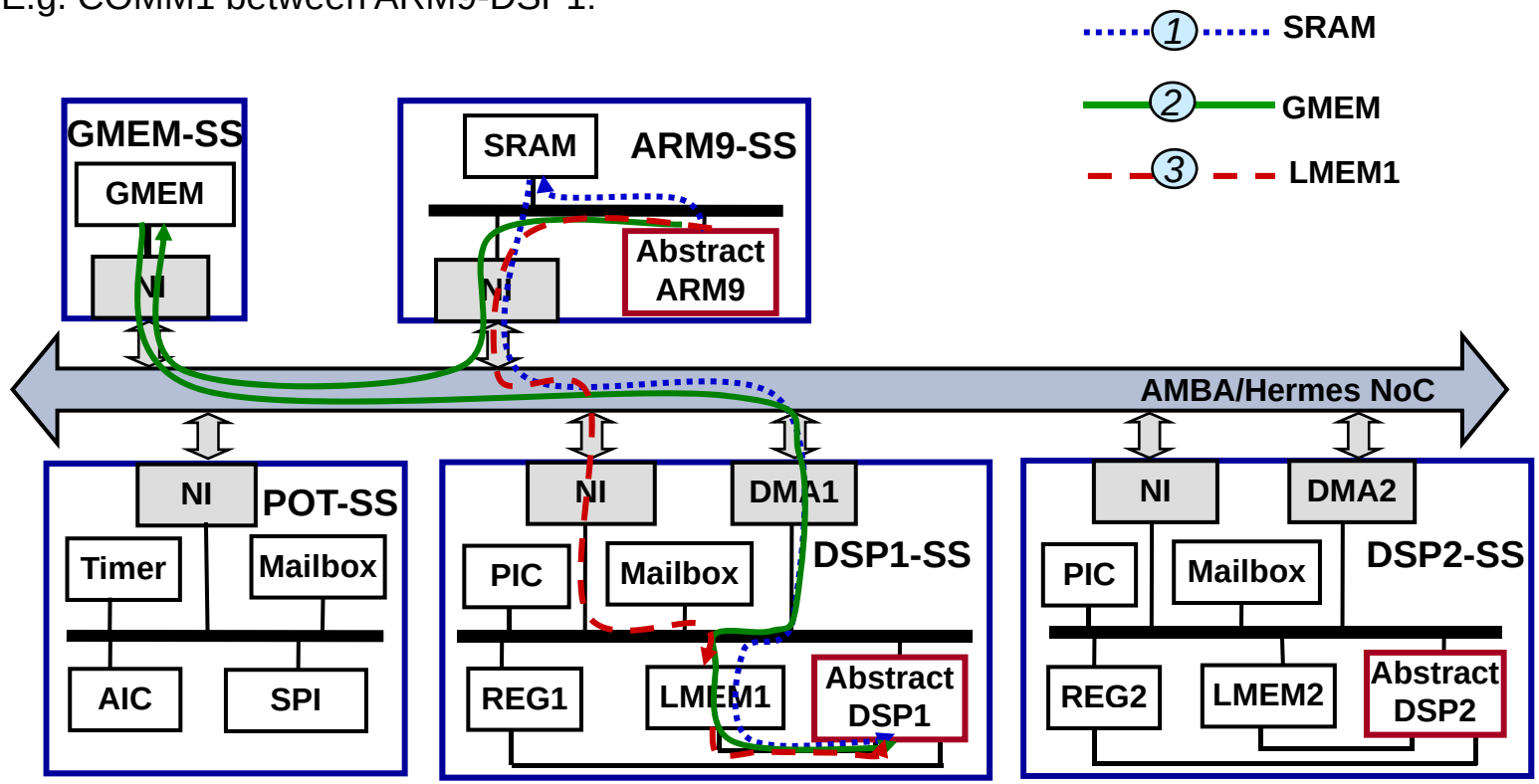


- Hermes NoC [3x3]: Topology, Arbiter, Routing Algorithm

Communication mapping schemes for H.264

- Full end-to-end communication path
- Explicit interconnect: AMBA, Hermes NoC

- **Multiple communication buffer mapping schemes:**
  - E.g. COMM1 between ARM9-DSP1:



Results for Transaction Accurate Communication Model for H.264

- Different Communication and IP Mapping Schemes for Interconnect components:
  - Hermes NoC [3x3] Torus, Mesh with 2 IP mapping schemes over NoC:

Scheme A

Y \ X	0	1	2
0	GMEM-SS	POT-SS	-
1	ARM9-SS	DMA1	DMA2
2	-	DSP1-SS	DSP2-SS

Scheme B

Y \ X	0	1	2
0	DMA1	-	-
1	ARM9-SS	GMEM-SS	DSP2-SS
2	POT-SS	DSP1-SS	DMA2

  - **AMBA bus**

Communication Mapping Scheme	Interconnect	IPs Mapping over NoC	Execution Time at 100MHz [ns]	Simulation Time [min]	Execution Cycles	NoC Routing Requests	Average Interconnect Latency [Cycles/Word]
GMEM+GMEM+GMEM	Mesh	**Scheme A**	64.028.725	36min	3.201.436	96.618.508	25
GMEM+GMEM+GMEM	Torus	**Scheme A**	46.713.986	28min29s	2.335.699	78.217.542	16
LMEM1+LMEM2+SRAM	Mesh	**Scheme A**	28.573.705	12min54s	1.428.685	13.118.044	10
LMEM1+LMEM2+SRAM	Torus	**Scheme A**	26.193.039	12min	1.309.652	12.674.692	9
LMEM1+SRAM+GMEM	Mesh	**Scheme A**	26.233.039	14min55s	1.594.237	13.144.538	11
LMEM1+SRAM+GMEM	Torus	**Scheme A**	26.193.040	14min48s	1.309.652	14.479.723	10
GMEM+GMEM+GMEM	Mesh	**Scheme B**	35.070.577	18min34s	1.753.529	24.753.610	9
GMEM+GMEM+GMEM	Torus	**Scheme B**	35.070.587	19min8s	1.753.529	24.753.488	9
LMEM1+LMEM2+SRAM	Mesh	**Scheme B**	31.964.760	17min8s	1.598.238	18.467.386	13
LMEM1+LMEM2+SRAM	Torus	**Scheme B**	31.924.752	16min14s	1.595.238	15.213.557	13
LMEM1+SRAM+GMEM	Mesh	**Scheme B**	31.964.731	18min38s	1.598.237	18.512.403	15
LMEM1+SRAM+GMEM	Torus	**Scheme B**	31.924.750	16min42s	1.596.238	18.115.966	14
GMEM+GMEM+GMEM	**AMBA**	-	17.436.640	8min24s	871.832	-	9
LMEM1+LMEM2+SRAM	**AMBA**	-	17.435.445	7min18s	871.772	-	9
LMEM1+SRAM+GMEM	**AMBA**	-	17.435.476	7min17s	871.774	-	9

Outline

- Communication modeling for MPSoC at different abstraction levels
- Experiments with H.264 Encoder
- **Conclusions**

Conclusions

- Communication modeling for MPSoC at several abstraction levels:
  - Combined Architecture/Application Model in Simulink
  - Virtual Communication and Interconnect Models in SystemC
  - Transaction Accurate Communication and Interconnect Models in SystemC
- Hardware simulation models automatically generated from Simulink
- Allows early and fast communication architecture exploration
- Several communication buffer mapping and interconnection schemes

Thank you!

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