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Variability-Aware Robust Design Space Exploration of Chip Multiprocessor Architectures

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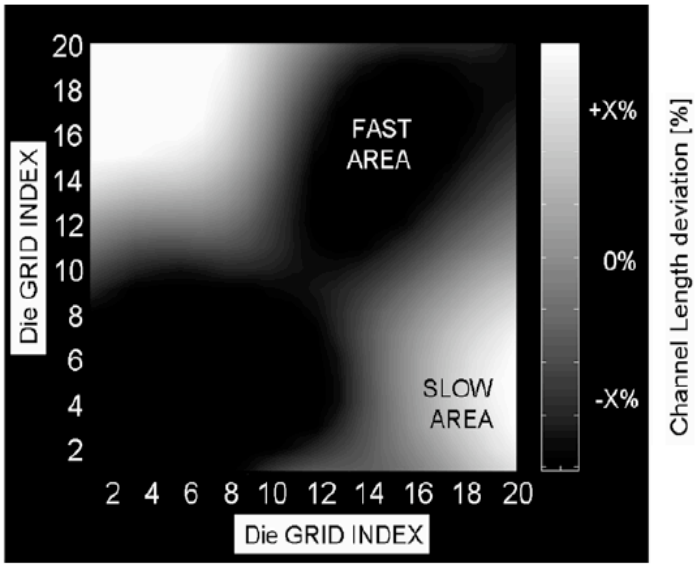
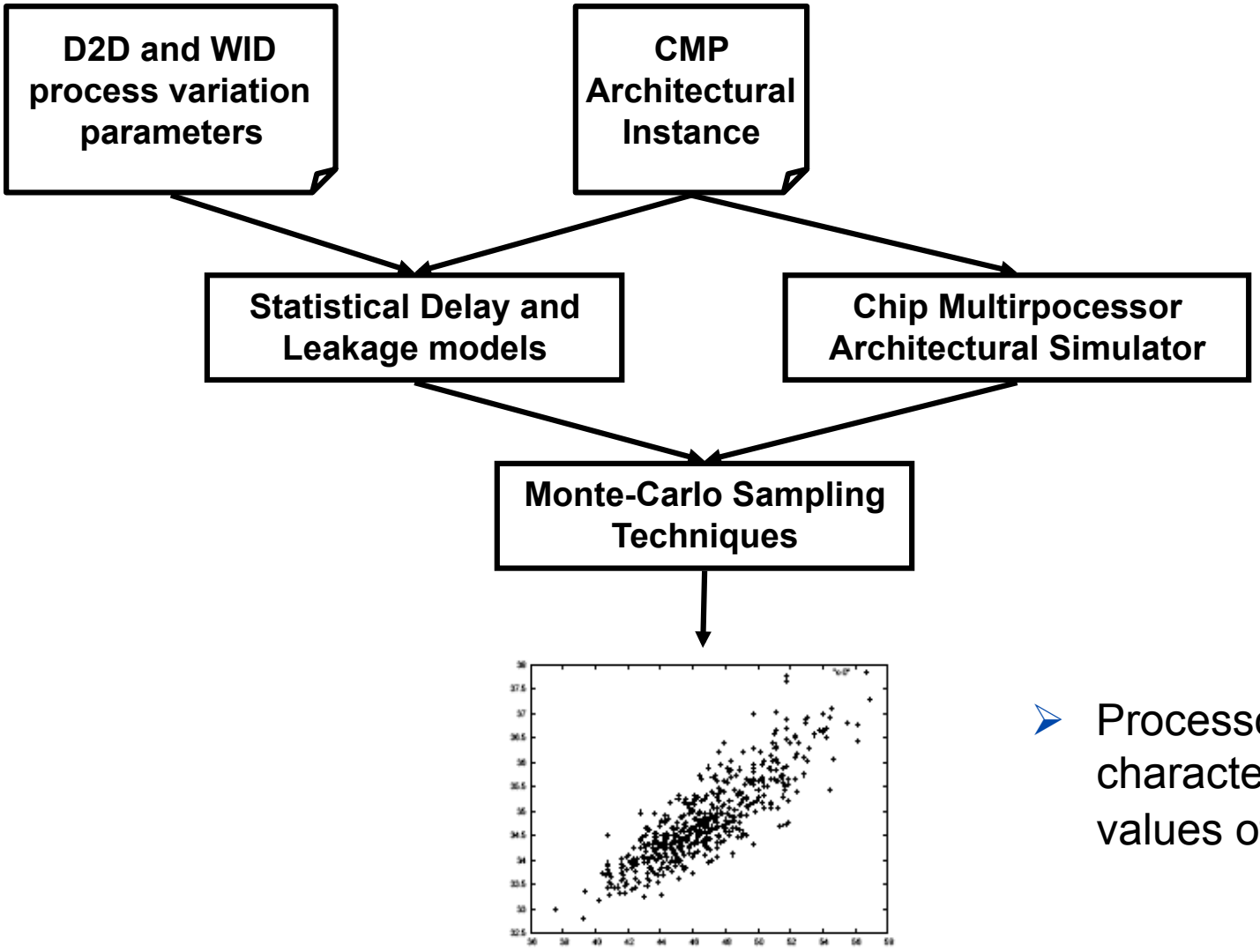
Motivation: Process Variability

- One of the most significant design challenges in next generation technologies is the management of process variability
- In designing high-performance multicore, there is a need of accurately estimate the impact of process variation since it is directly related to the company's overall revenue
  - The underestimation of these effects can impact to the system performances and to the design yield
  - On the other side, the overestimation can impact the design and manufacturing effort
- Estimation ASAP in the design flow!



- Image From: Y. Abulafia, A. Kornfeld, "Estimation of FMAX and ISB in microprocessors," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on* , vol. 13, no.10, pp. 1205-1209, Oct. 2005

Variability-Aware CMP Architecture Evaluation



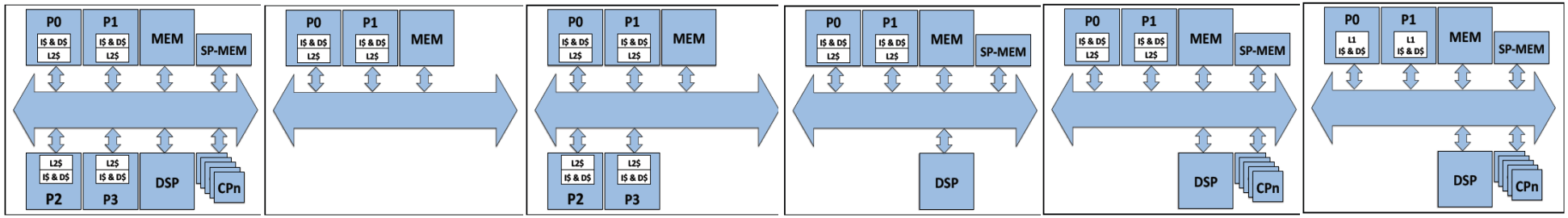
- Processors are not more characterized by single values of metrics!

Outline

- Motivations
- Introduction
  - Design Space Exploration
  - Robust Design
- Robust Design Space Exploration
- MPEG2 Decode Case Study
- Conclusions

Platform-based Design

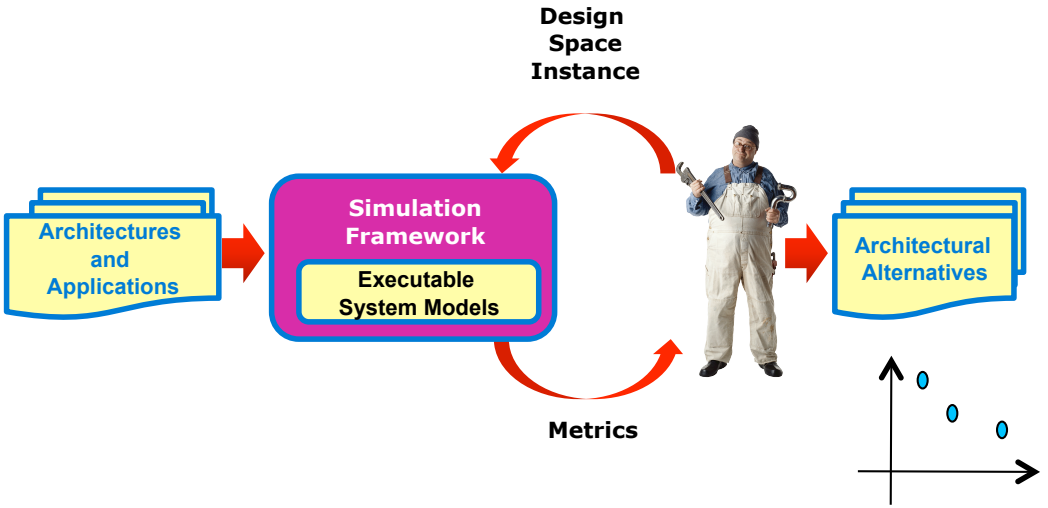
- *Hardware platforms* are used by vendors as reference designs for family of applications
  - ! Easy and fast customization to customers' requirements

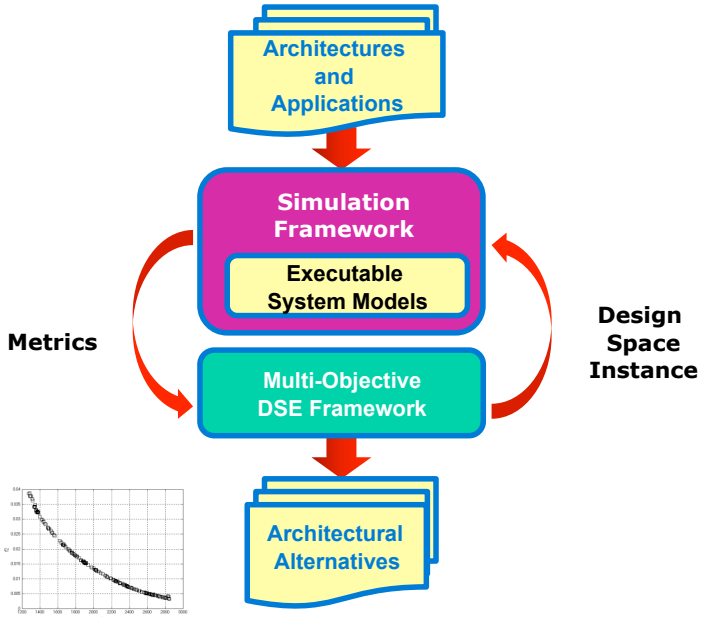


- The design based on *Hardware Platforms* enable:
  - Design-time customization targeted to a specific application
  - Pre-verified configurable IPs are instantiated and sized in order to meet application-specific constraints
  - Enables low-risk deployment while meeting time-to-market constraints
- The tuning process is called *Design Space Exploration*

Design Space Exploration

- **Common view of the DSE problem**
  - Configurable Hw Platform
  - *Manual* Optimization by Designer Experience
- **Enhanced view of the DSE problem**
  - *High* Configurable Hw Platform
  - *Automatic* Optimization Framework
  - Previous framework:
    - Esteco modeFRONTIER
    - ETH - PISA

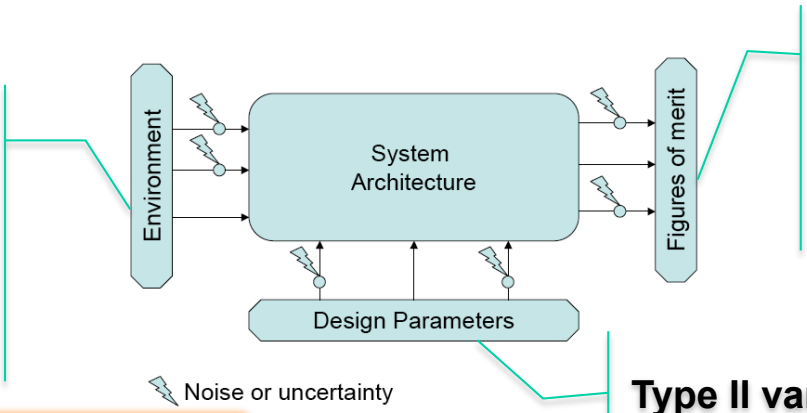




Robust Design

- *Robust design* is a discipline which aims at optimizing the target design by taking into account the uncertainty factors
- The resulting designs are optimal over the set of considered uncertainty scenarios
- Classification of the uncertainty factors:

Type I variation: Due to the environment in which the system operates (e.g. Workloads and dataset applied to the system).



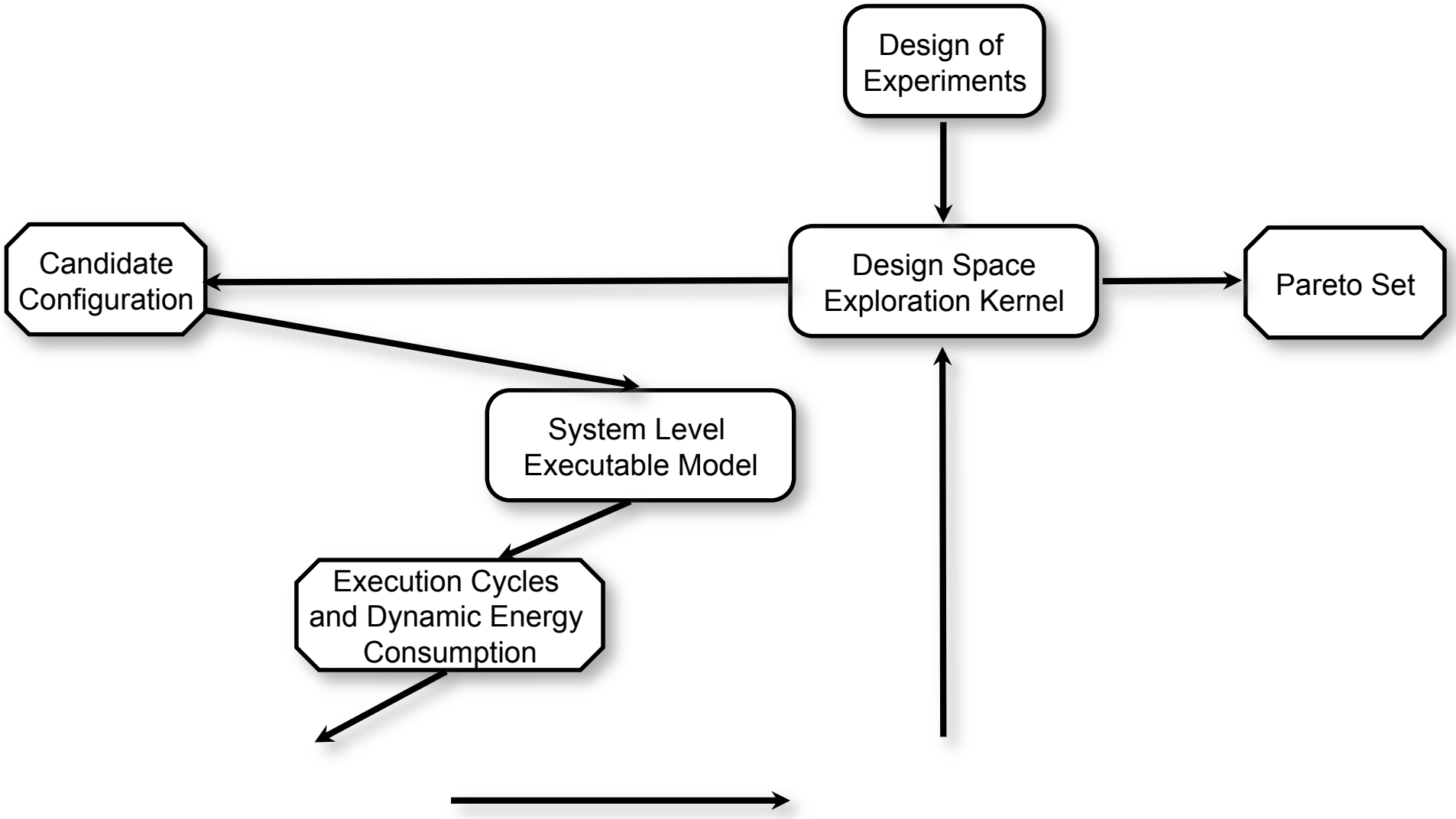
Variations of the figures of merit: Due to the imprecision in the system evaluation of the figures of merit (e.g. simulation accuracy and measurement errors)

Type II variations: Due to the tolerances in the physical implementation of the current system configurations and are represented by variations of the design parameters.

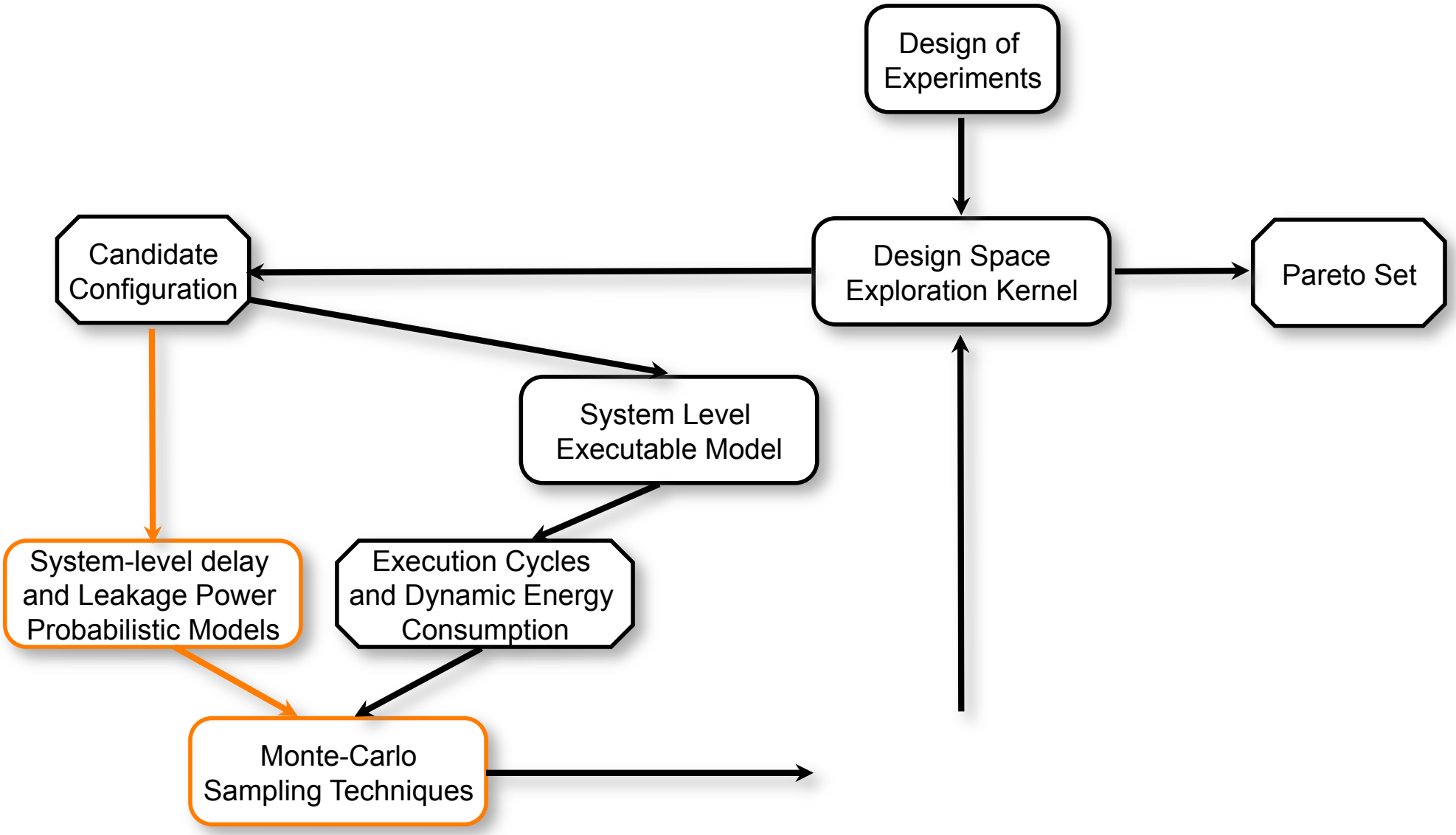
Observed system function of the design parameters:

$$f_o = \sigma[f(x+\delta, \xi)]$$

Robust Design Space Exploration Flow (1/4)



Robust Design Space Exploration Flow (2/4)



Robust Design Space Exploration

- We modify the standard DSE techniques in order to tackle also the variability problem and yield
- Both average case and functions distribution need to be optimized
- Following the TAGUCHI theory of quality design we introduce a quality function QY of a response function Y as follows:
  - For “as small as possible” problems for Y:

$$Q_y = 10^{\frac{SN_y}{10}} = \frac{1}{\left(\frac{1}{N}\sum_{i=1}^{N} y_i^2\right)}$$

  - For “as large as possible” problems for Y:

$$Q_y = 10^{\frac{SN_y}{10}} = \frac{1}{\left(\frac{1}{N}\sum_{i=1}^{N} \frac{1}{y_i^2}\right)}$$

    Where N is the number of sample of the random variable Y

- The new objective functions of the DSE phase are composed of the Quality metrics and the Yield that have to be maximized

Yield Definition

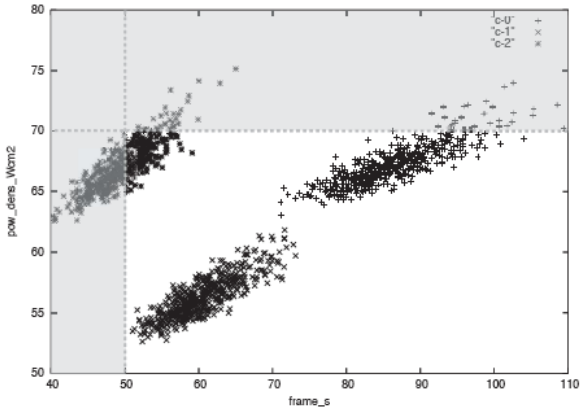
- Percentage of dies which does not violated physical constraints typically expressed in terms of Critical Path Delay (D) and Power (P):

$$Yield = Pr[\, D \leq D_0,\ P \leq P_0]$$

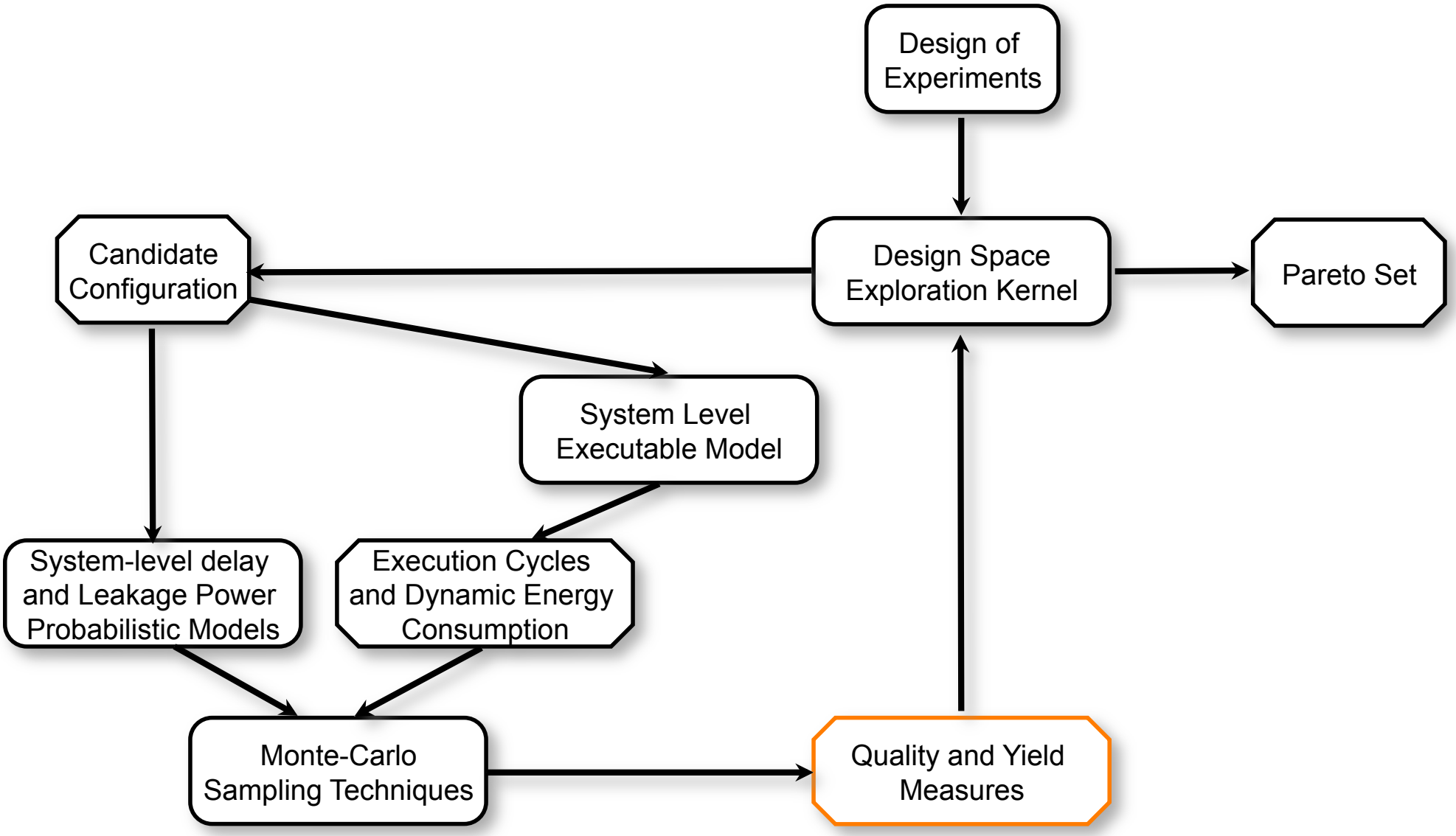
- The yield can be expressed also in terms of application requirements (e.g. throughput and QoS)

$$Yield = Pr[\, M_{0Min} \leq M_0 \leq M_{0Max},\ \ldots,\ M_{nMin} \leq M_n \leq M_{nMax}]$$

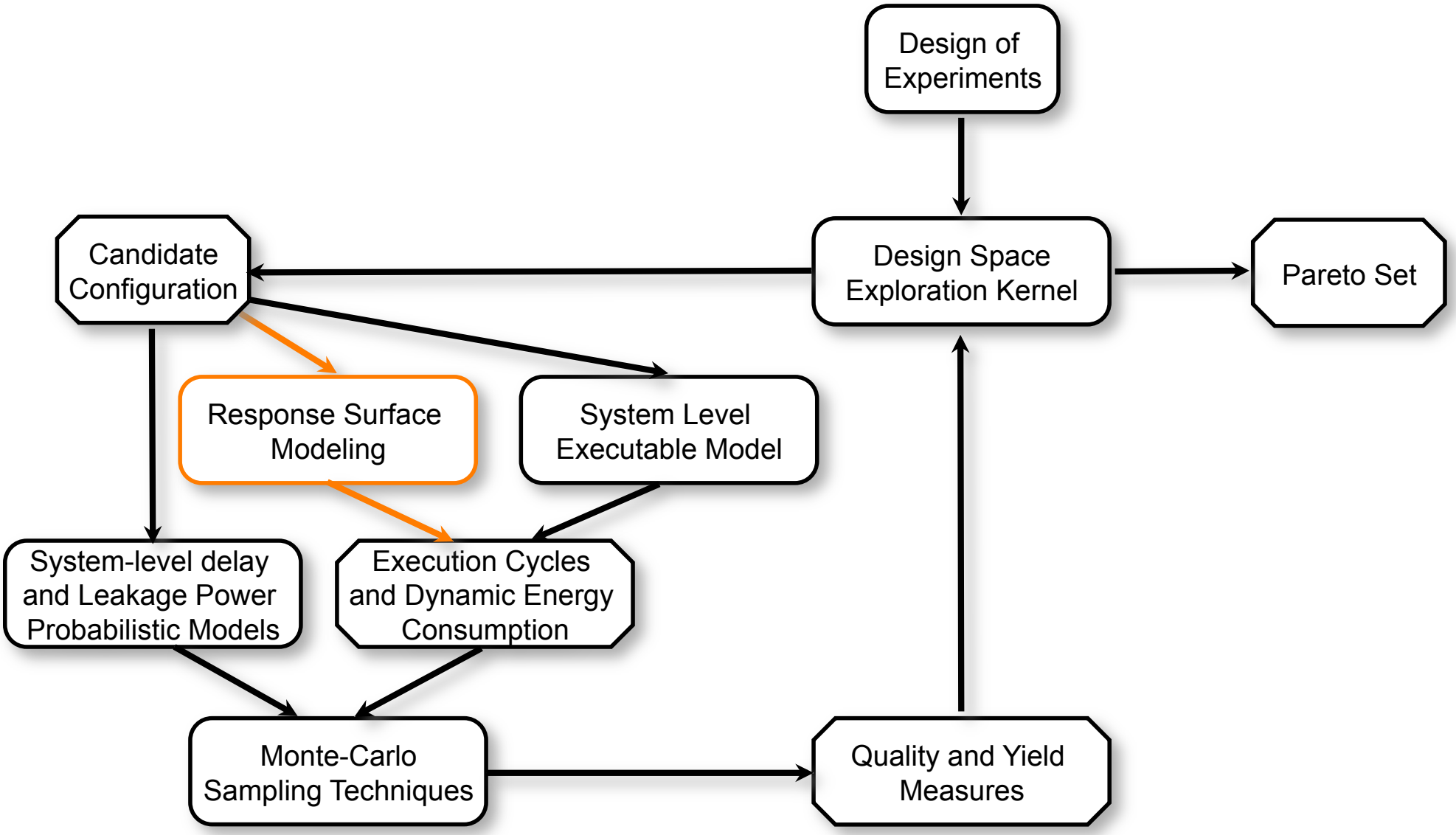
Where $M_0 \ldots M_n$ are architecture/application Metrics subject to constraints/requirements



Robust Design Space Exploration Flow (3/4)



Robust Design Space Exploration Flow (4/4)



Robust DSE: MPEG2 Dec Case Study

- We apply the proposed methodology to the optimization of a shared memory CMP architecture with private L2$ running an MPEG2 Decoder playing a 640x480 video

Parameter	Min.	Max.
# Processors	2	16
Processor issue width.	1	8
L1 instruction cache size	2K	16K
L1 data cache size	2K	16K
L2 private cache size	32K	256K
L1 instruction cache assoc.	1w	8w
L1 data cache assoc.	1w	8w
L2 private cache assoc.	1w	8w
I/D/L2 block size	16	32

2^{17} Design Points

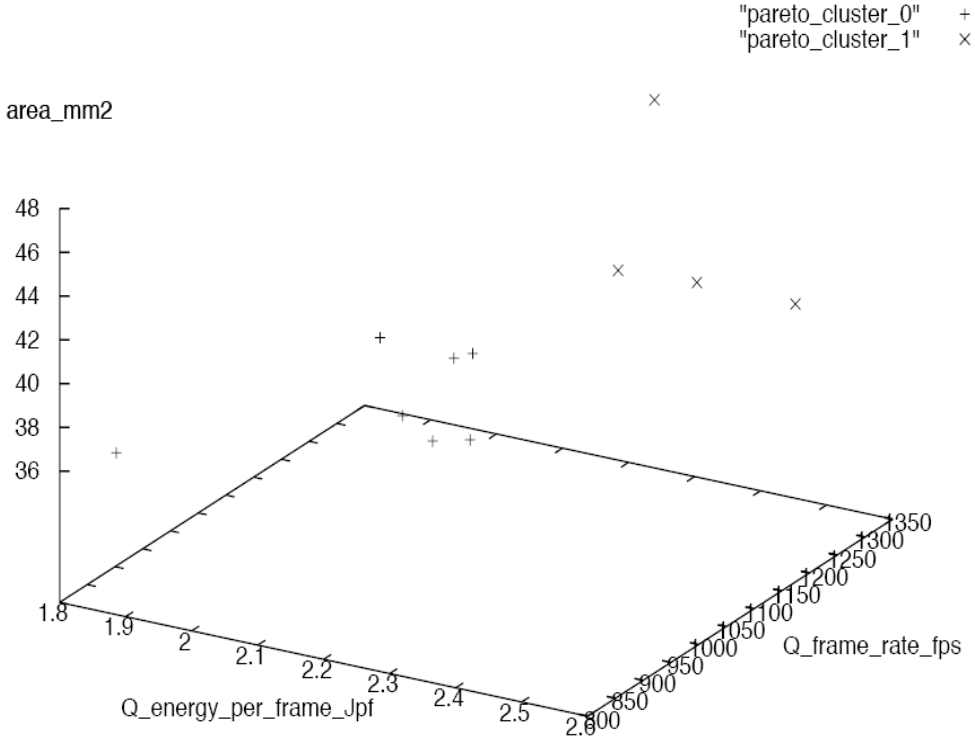
- The multiprocessor architectural simulator we used to derive nominal performance and power value is SESC
  - Power models are derived from WATTCH and CACTI
  - Area models are tuned with respect to IBM Power5 processor

Exploration Results

- We formalize the problem as:

$$\max_{\vec{x} \in X} \begin{bmatrix} \frac{1}{total\_system\_area}(\vec{x}) \\ Q_{energy\_per\_frame}(\vec{x}) \\ Q_{frame\_rate}(\vec{x}) \\ Y(\vec{x}) \end{bmatrix}$$

11 Pareto Points
Clustered into 2 set



where the Yield is defined as:

$$Y = Pr[frame\_rate(\vec{x}) \geq 25, P_{dens} \leq 60W/cm^2, P \leq 25W]$$

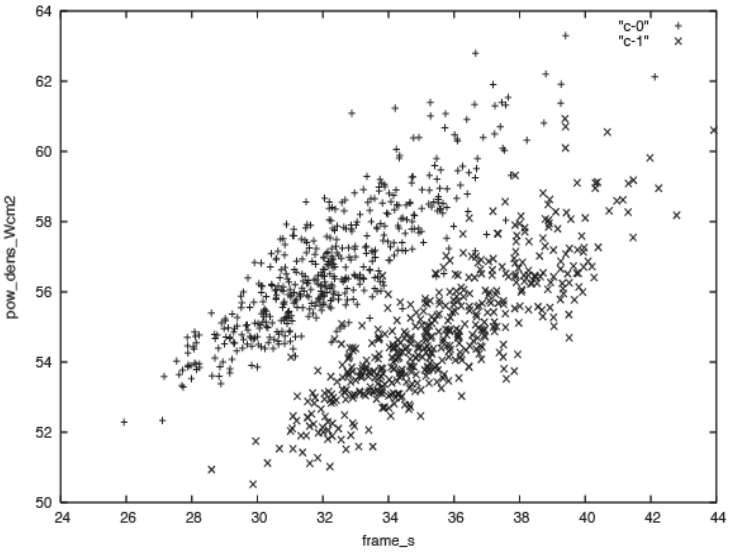
and subject to the following constraints

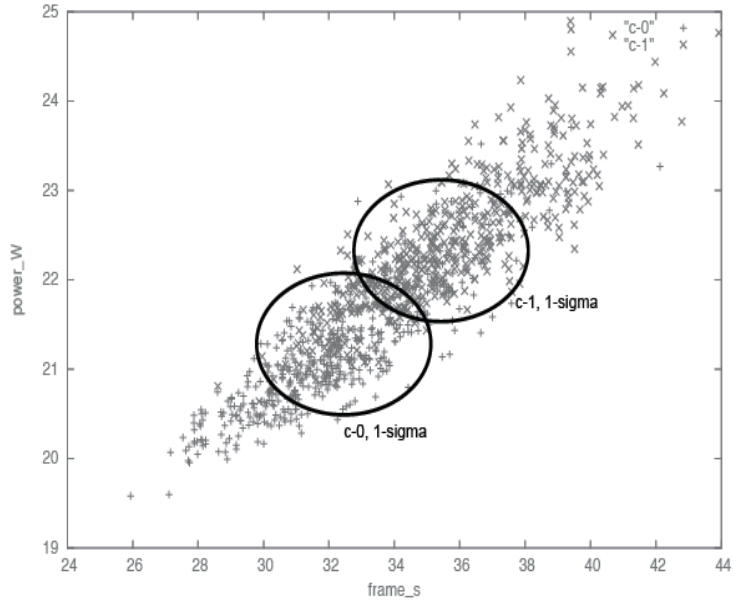
$$total\_system\_area(\vec{x}) \leq 85mm^2$$

$$Y(\vec{x}) \geq 0.85$$

The Champion for each Cluster

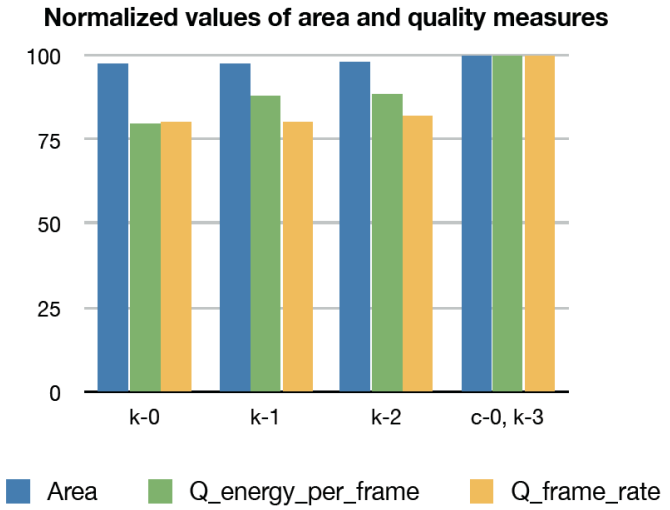
Parameter/metric	Cluster 0	Cluster 1
# Processors	4	4
Processor issue width.	1	1
L1 instruction cache size	2K	16K
L1 data cache size	8K	8K
L2 private cache size	64K	128K
L1 instruction cache assoc.	2w	1w
L1 data cache assoc.	8w	8w
L2 private cache assoc.	4w	2w
I/D/L2 block size	16B	16B
total_system_area $[mm^2]$	37.5	40.9
Q_energy_per_frame $[J/f]^{(-2)}$	2.3	2.5
Q_frame_rate $[fps]^2$	1036.2	1253.2
Yield	0.95	0.99
frame rate (μ, σ) $[fps]$	32.5, 2.7	35.7, 2.7
power density (μ, σ) $[W/cm^2]$	56.74, 1.9	54.95, 1.9
power (μ, σ) $[W]$	21.3, 0.7	22.5, 0.8





Comparison with conventional approach

- The constraints have been strengthened by taking into account the expected standard deviation for the Frame Rate, Average Power Consumption and Power Density
  - Optimization on the nominal values of the metrics
  - Adding a bound of 3σ to the constraints
    - NO SOLUTION FOUND!
  - Adding a bound of 2σ to the constraints
    - Found just 4 solutions (11 Pareto Solutions using our methodology)
      - One is the C-1, while the other three are very close to the first one
      - Yield =0.99



Conclusions

- We presented a technique to tackle the variation-aware design of Chip-Multiprocessor architectures at system level
- We extended the conventional DSE flow to become robust with respect to the problem of the variability and yield
- We proved the effectiveness of the Robust DSE applied at the architecture level with respect to the conventional approach
- *This work is part of the ICT-FP7 EU project MULTICUBE*
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Limits of the presented paper

- Process Variability Model
  - No modeling of process variability effects on the switching power
- Estimation accuracy is not considered

Model	Avg. Error	Data	Technology
Inverter-gate delay	$\leq$ 30%	Spice	30nm $\rightarrow$ 200nm
Critical path distrib.	$\leq$ 50%	Intel processor	250nm
Execution cycles	$\leq$ 7%	MIPS R10K processor	-
Dynamic power	$\leq$ 30%	MIPS R10K, Alpha 21264, Intel Pentium Pro	350nm
Leakage power	$\leq$ 10%	ISCAS, MCNC benchmarks	130nm
Area	$\leq$ 25%	IBM Power5 processor	130nm

- Fully synchronous design
- No compensation approaches has been considered