Variability-Aware Robust Design Space Exploration of Chip Multiprocessor Architectures

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Motivation: Process Variability

- One of the most significant design challenges in next generation technologies is the management of process variability.
- In designing high-performance multicore, there is a need of accurately estimate the impact of process variation since it is directly related to the company’s overall revenue.
  - The underestimation of these effects can impact to the system performances and to the design yield.
  - On the other side, the overestimation can impact the design and manufacturing effort.
- Estimation ASAP in the design flow!

Variability-Aware CMP Architecture Evaluation

- D2D and WID process variation parameters
- Statistical Delay and Leakage models
- Monte-Carlo Sampling Techniques
- CMP Architectural Instance
- Chip Multiprocessor Architectural Simulator

- Processors are not more characterized by single values of metrics!
Motivations
Introduction
  • Design Space Exploration
  • Robust Design
Robust Design Space Exploration
MPEG2 Decode Case Study
Conclusions
Platform-based Design

- **Hardware platforms** are used by vendors as reference designs for family of applications
  - Easy and fast customization to customers’ requirements

- The design based on **Hardware Platforms** enable:
  - Design-time customization targeted to a specific application
  - Pre-verified configurable IPs are instantiated and sized in order to meet application-specific constraints
  - Enables low-risk deployment while meeting time-to-market constraints

- The tuning process is called **Design Space Exploration**
Design Space Exploration

- Common view of the DSE problem
  - Configurable Hw Platform
  - Manual Optimization by Designer Experience

- Enhanced view of the DSE problem
  - High Configurable Hw Platform
  - Automatic Optimization Framework
  - Previous framework:
    - Esteco modeFRONTIER
    - ETH - PISA
Robust design is a discipline which aims at optimizing the target design by taking into account the uncertainty factors.

The resulting designs are optimal over the set of considered uncertainty scenarios.

Classification of the uncertainty factors:

**Type I variation:** Due to the environment in which the system operates (e.g., Workloads and dataset applied to the system).

**Type II variations:** Due to the tolerances in the physical implementation of the current system configurations and are represented by variations of the design parameters.

**Observed system function of the design parameters:**

\[ f_o = \sigma[f(x + \delta, \xi)] \]
Robust Design Space Exploration Flow (1/4)

- Candidate Configuration
- System Level Executable Model
- Execution Cycles and Dynamic Energy Consumption
- Design of Experiments
- Design Space Exploration Kernel
- Pareto Set
Robust Design Space Exploration Flow (2/4)

- Candidate Configuration
- System Level Executable Model
- System Level delay and Leakage Power Probabilistic Models
- Execution Cycles and Dynamic Energy Consumption
- Monte-Carlo Sampling Techniques
- Design of Experiments
- Design Space Exploration Kernel
- Pareto Set
We modify the standard DSE techniques in order to tackle also the variability problem and yield.

Both average case and functions distribution need to be optimized.

Following the TAGUCHI theory of quality design we introduce a quality function $Q_Y$ of a response function $Y$ as follows:

- For “as small as possible” problems for $Y$:
  \[ Q_y = 10 \left( \frac{SN_y}{10} \right) = \frac{1}{\left( \frac{1}{N} \sum_{i=1}^{N} y_i^2 \right)} \]

- For “as large as possible” problems for $Y$:
  \[ Q_y = 10 \left( \frac{SN_y}{10} \right) = \frac{1}{\left( \frac{1}{N} \sum_{i=1}^{N} \frac{1}{y_i^2} \right)} \]

Where $N$ is the number of samples of the random variable $Y$.

The new objective functions of the DSE phase are composed of the Quality metrics and the Yield that have to be maximized.
Yield Definition

- Percentage of dies which does not violate physical constraints typically expressed in terms of Critical Path Delay (D) and Power (P):

\[ \text{Yield} = \text{Pr}[D \leq D_0, \ P \leq P_0] \]

- The yield can be expressed also in terms of application requirements (e.g. throughput and QoS)

\[ \text{Yield} = \text{Pr}[M_0\text{Min} \leq M_0 \leq M_0\text{Max}, \ldots, M_n\text{Min} \leq M_n \leq M_n\text{Max}] \]

Where \(M_0\ldots M_n\) are architecture/application Metrics subject to constraints/requirements
Robust Design Space Exploration Flow (3/4)

- Candidate Configuration
- System Level Executable Model
  - System-level delay and Leakage Power Probabilistic Models
  - Execution Cycles and Dynamic Energy Consumption
- Monte-Carlo Sampling Techniques
- Quality and Yield Measures
- Design of Experiments
  - Design Space Exploration Kernel
  - Pareto Set
Robust Design Space Exploration Flow (4/4)

- Candidate Configuration
- Response Surface Modeling
- System-level delay and Leakage Power Probabilistic Models
- Monte-Carlo Sampling Techniques
- Design of Experiments
- System Level Executable Model
- Execution Cycles and Dynamic Energy Consumption
- Quality and Yield Measures
- Design Space Exploration Kernel
- Pareto Set
We apply the proposed methodology to the optimization of a shared memory CMP architecture with private L2$ running an MPEG2 Decoder playing a 640x480 video.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
</tr>
</thead>
<tbody>
<tr>
<td># Processors</td>
<td>2</td>
<td>16</td>
</tr>
<tr>
<td>Processor issue width</td>
<td>1</td>
<td>8</td>
</tr>
<tr>
<td>L1 instruction cache size</td>
<td>2K</td>
<td>16K</td>
</tr>
<tr>
<td>L1 data cache size</td>
<td>2K</td>
<td>16K</td>
</tr>
<tr>
<td>L2 private cache size</td>
<td>32K</td>
<td>256K</td>
</tr>
<tr>
<td>L1 instruction cache assoc.</td>
<td>1w</td>
<td>8w</td>
</tr>
<tr>
<td>L1 data cache assoc.</td>
<td>1w</td>
<td>8w</td>
</tr>
<tr>
<td>L2 private cache assoc.</td>
<td>1w</td>
<td>8w</td>
</tr>
<tr>
<td>I/D/L2 block size</td>
<td>16</td>
<td>32</td>
</tr>
</tbody>
</table>

$2^{17}$ Design Points

The multiprocessor architectural simulator we used to derive nominal performance and power value is SESC.

- Power models are derived from WATTCH and CACTI.
- Area models are tuned with respect to IBM Power5 processor.
We formalize the problem as:

\[
\begin{align*}
\max_{\bar{x} \in X} & \quad \frac{1}{total\_system\_area(\bar{x})} \\
& \quad \frac{Q_{energy\_per\_frame}(\bar{x})}{Q_{frame\_rate}(\bar{x})} \\
& \quad Y(\bar{x})
\end{align*}
\]

where the Yield is defined as:

\[Y = Pr[frame\_rate(\bar{x}) \geq 25, P_{dens} \leq 60W/cm^2, P \leq 25W]\]

and subject to the following constraints

\[total\_system\_area(\bar{x}) \leq 85\text{mm}^2\]

\[Y(\bar{x}) \geq 0.85\]
## The Champion for each Cluster

<table>
<thead>
<tr>
<th>Parameter/metric</th>
<th>Cluster 0</th>
<th>Cluster 1</th>
</tr>
</thead>
<tbody>
<tr>
<td># Processors</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>Processor issue width</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>L1 instruction cache size</td>
<td>2K</td>
<td>16K</td>
</tr>
<tr>
<td>L1 data cache size</td>
<td>8K</td>
<td>8K</td>
</tr>
<tr>
<td>L2 private cache size</td>
<td>64K</td>
<td>128K</td>
</tr>
<tr>
<td>L1 instruction cache assoc.</td>
<td>2w</td>
<td>1w</td>
</tr>
<tr>
<td>L1 data cache assoc.</td>
<td>8w</td>
<td>8w</td>
</tr>
<tr>
<td>L2 private cache assoc.</td>
<td>4w</td>
<td>2w</td>
</tr>
<tr>
<td>I/D/L2 block size</td>
<td>16B</td>
<td>16B</td>
</tr>
<tr>
<td>total_system_area $[mm^2]$</td>
<td>37.5</td>
<td>40.9</td>
</tr>
<tr>
<td>Q_energy_per_frame $[J/f]$ $[-2]$</td>
<td>2.3</td>
<td>2.5</td>
</tr>
<tr>
<td>Q_frame_rate $[fps]^2$</td>
<td>1036.2</td>
<td>1253.2</td>
</tr>
<tr>
<td>Yield</td>
<td>0.95</td>
<td>0.99</td>
</tr>
<tr>
<td>frame rate $(\mu, \sigma) [fps]$</td>
<td>32.5, 2.7</td>
<td>35.7, 2.7</td>
</tr>
<tr>
<td>power density $(\mu, \sigma) [W/cm^2]$</td>
<td>56.74, 1.9</td>
<td>54.95, 1.9</td>
</tr>
<tr>
<td>power $(\mu, \sigma) [W]$</td>
<td>21.3, 0.7</td>
<td>22.5, 0.8</td>
</tr>
</tbody>
</table>
Comparison with conventional approach

- The constraints have been strengthened by taking into account the expected standard deviation for the Frame Rate, Average Power Consumption and Power Density
  - Optimization on the nominal values of the metrics
  - Adding a bound of $3\sigma$ to the constraints
    - NO SOLUTION FOUND!
  - Adding a bound of $2\sigma$ to the constraints
    - Found just 4 solutions (11 Pareto Solutions using our methodology)
      - One is the C-1, while the other three are very close to the first one
      - Yield = 0.99
Conclusions

- We presented a technique to tackle the variation-aware design of Chip-Multiprocessor architectures at system level

- We extended the conventional DSE flow to become robust with respect to the problem of the variability and yield

- We proved the effectiveness of the Robust DSE applied at the architecture level with respect to the conventional approach

- *This work is part of the ICT-FP7 EU project MULTICUBE*
  www.multicube.eu
Limits of the presented paper

- Process Variability Model
  - No modeling of process variability effects on the switching power
- Estimation accuracy is not considered

<table>
<thead>
<tr>
<th>Model</th>
<th>Avg. Error</th>
<th>Data</th>
<th>Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter-gate delay</td>
<td>&lt; 30%</td>
<td>Spice</td>
<td>30nm → 200nm</td>
</tr>
<tr>
<td>Critical path distrib.</td>
<td>&lt; 50%</td>
<td>Intel processor</td>
<td>250nm</td>
</tr>
<tr>
<td>Execution cycles</td>
<td>&lt; 7%</td>
<td>MIPS R10K processor</td>
<td>-</td>
</tr>
<tr>
<td>Dynamic power</td>
<td>&lt; 30%</td>
<td>MIPS R10K, Alpha 21264, Intel Pentium Pro</td>
<td>350nm</td>
</tr>
<tr>
<td>Leakage power</td>
<td>&lt; 10%</td>
<td>ISCAS, MCNC benchmarks</td>
<td>130nm</td>
</tr>
<tr>
<td>Area</td>
<td>&lt; 25%</td>
<td>IBM Power5 processor</td>
<td>130nm</td>
</tr>
</tbody>
</table>

- Fully synchronous design
- No compensation approaches has been considered