Three-Dimensional Integration Technology and Integrated Systems

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Outline

1. Background
2. Wafer-to-Wafer 3D Integration Technology in Tohoku University
3. 3D LSI Test Chip Fabrication
4. Super-Chip Integration
5. 3-D Integration Using Self-Assembly Technique
6. Summary

	Device/Process	3D IC Technology
1978	3D DRAM (Hitachi,Koyanagi)(1978) Laser anneal	
	SOI (SIMOX)(NTT, Izumi)(1979) Laser recrystallization	
1980	Stacked CMOS(Stanford) Laser anneal MOS (Hitachi, Koyanagi) (1979) 3D SRAM Wafer bonding (NEC・Nakamura)	3D IC National Project (1981～1990) (Japan) Laser anneal 3D (Mitsubishi) Wafer bonding 3D(Transfer) (NEC) Wafer bonding 3D (Non-transfer) (Tohoku Univ.)
1990	SOI (Wafer bonding) (Hughs) SOI (Smart Cut)(Latti)	Wafer bonding 3D(Buried interconnection) (Tohoku Univ.) Wafer/Chip bonding 3D (Tohoku Univ., Fraunhofer) Wafer bonding 3D(SOI) (Motorola etc.) ASET Project(1999～2003) (Japan) Chip bonding 3D
2000	CMP (IBM) Damascene Cu wiring (IBM)	Wafer bonding 3D (Cu bonding) (RPI etc.) a-Si/Poly-Si 3D (Stanford Univ., Matrix Semi.) Wafer bonding 3D(SOI) (IBM)

Major Players in Research and Development of 3-D Technology

3-D PROCESSES									
	RPI	Fraunhofer-Munich	ASET Japan	Tohoku University Japan	IBM	Infineon	MCNC-RDI	Toshiba	Tezzaron
Wafer to wafer	X			X				X	X
Chip to wafer		X				X	X		
Chip to chip			X				X		
SOI or bulk wafer	SOI		Bulk		SOI		Bulk	Bulk	
Via size (μm)	2 × 2	2.5	10	2.5			4	30	
Via etch process	SF_6		SF_6	SF_6			SF_6	SF_6	SF_6
Peripheral vias			X					X	
Area array vias	X	X				X	X		X
Via dielectric	SiO_2	SiO_2	SiO_2	SiO_2		SiO_2	Polymer	SiO_2	SiO_2
Barrier layer	TiN	TiN	TiN			TiN	TiN	TiN	TiN
Metal plug	Cu	W or Cu	Cu	Poly-Si or W	Cu	Cu	Cu	Cu	Cu
Handle wafer	No	Yes	Yes	Yes	Yes	No			No
Bonding scheme	Polymer	Cu-Sn eutectic	Cu-Sn eutectic	In/Au bumps	Si fusion	Cu-Sn-Cu	Polymer or bumps	Bumps	Cu-Cu

After Philip Garrou, MCNC Research & Development Institute, Research Triangle Park, N.C. -- 2/1/2005
Semiconductor International

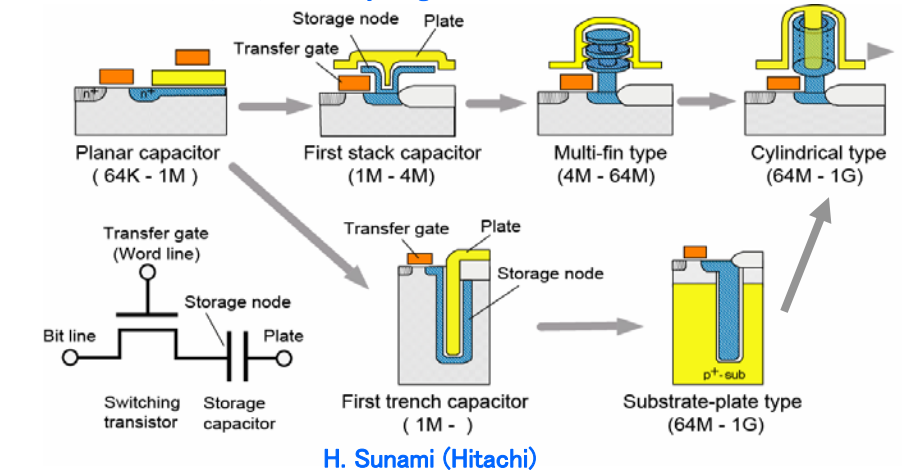
Research and Development of 3-D Technology in the World

After：EMC-3D Technical Symposium (April 23-27, 2007)

Evolution of DRAM Memory Cell

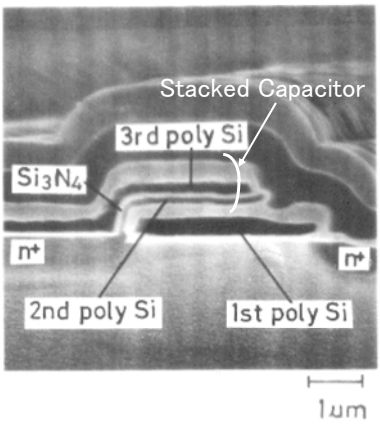
2D (1975–1985)　　3D (1985 –　)

Dr. R. H. Dennard (IBM)　M. Koyanagi (Hitachi)



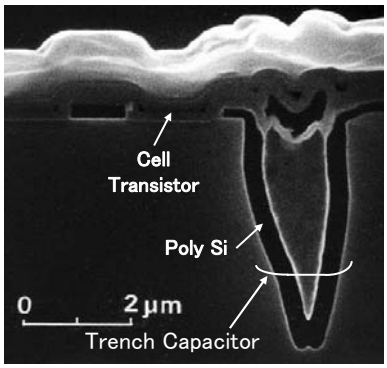
H. Sunami (Hitachi)

SEM Cross-Sectional View of 3D-DRAM Cells



Stacked Capacitor DRAM

After M. Koyanagi, 1978 IEDM

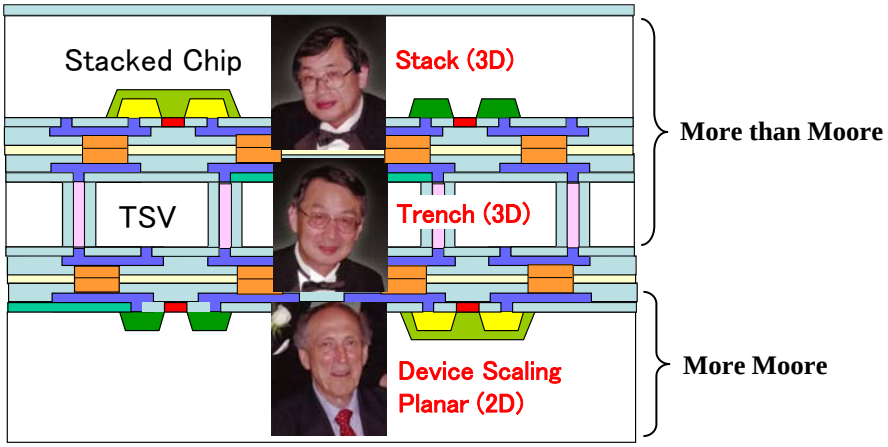


Trench Capacitor DRAM

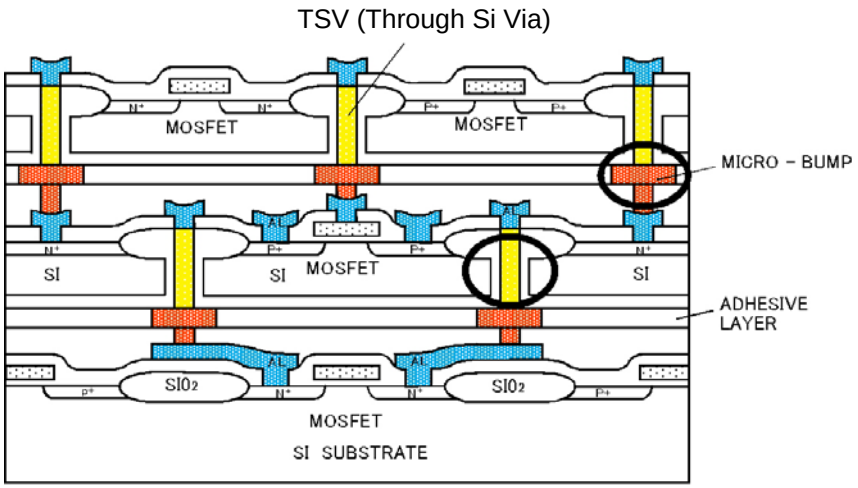
After H. Sunami, 1983 IEDM

IEEE Junichi-Nishizawa Medal (2006)

Evolution from 3D Stacked DRAM Cells to 3D Stacked LSI

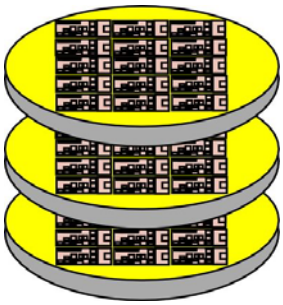


Cross-Sectional Structure of 3-D LSI



3D Technology Based on Wafer-to-Wafer Bonding in Tohoku University

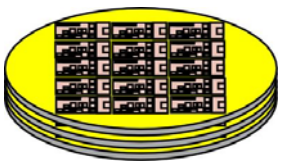
Completed LSI wafers with TSV's



Wafer-to-wafer bonding

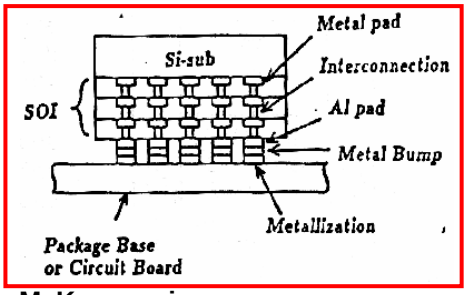
Wafer thinning

3D LSI



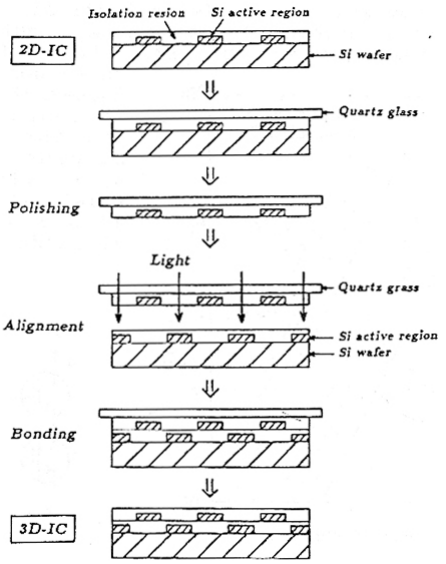
First Proposal of Wafer-to-Wafer Bonding with TSV (1989)

3D Integration Technology Using Wafer Bonding and Thinning



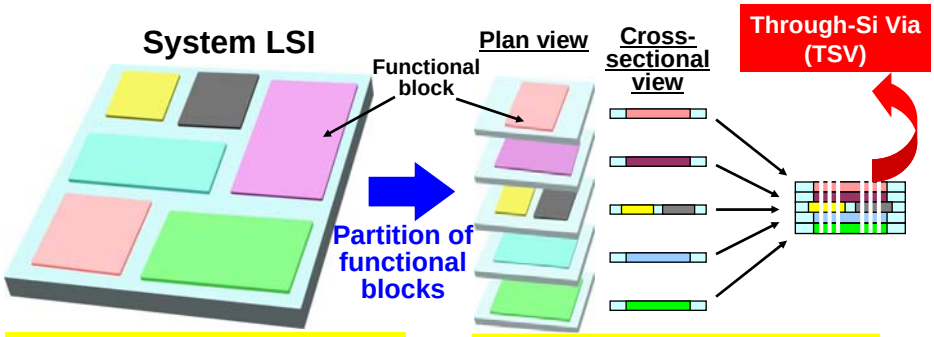
M. Koyanagi,
Proc. 8th Symposium on Future Electron Devices, pp.50-60
(Oct. 1989)

H. Takata, M. Koyanagi et. al.,
Proc. Intern. Semiconductor Device Research Symposium, pp.327-330
(Dec. 1991)



Background on 3D Integration

1. High packing density
2. Size & weight reduction
3. Short interconnect length
4. High-speed operation
5. Low power consumption
6. Parallel processing
7. New functionality
8. New applications



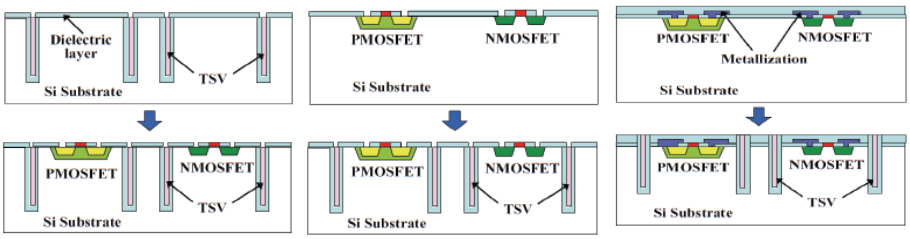
Big concerns: Long wiring, Global wiring

Conventional 2D LSI

Replaced by short vertical interconnections

3D stacked LSI

TSV Fabrication Process Sequences for 3-D LSIs



(a) Via first

Poly-Si TSV

(b) Via before BEOL

W TSV

W/ poly-Si TSV

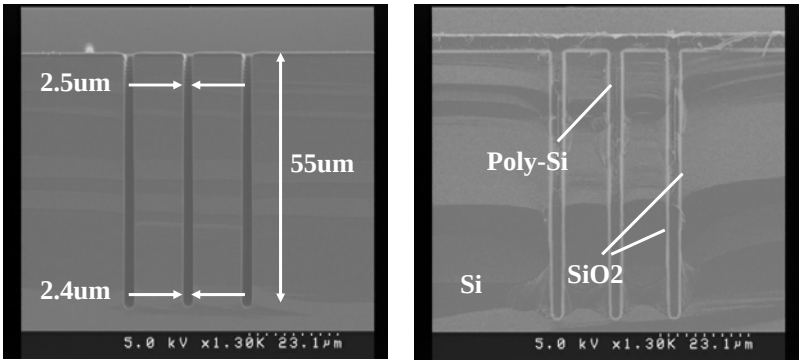
(c) Via after BEOL

W TSV

Cu TSV

SEM Cross Section of Poly-Si TSV

(Via first)

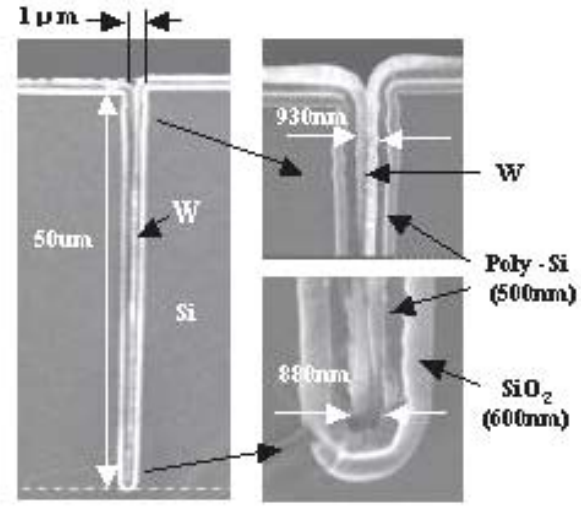


(a) Si deep trench etching **(b) Filling with Poly-Si**

T. Matsumoto and M. Koyanagi et al., SSDM, pp.1073- 1074, 1995.

SEM Cross Section of W/ Poly-Si TSV

(Via first or Via before BEOL)

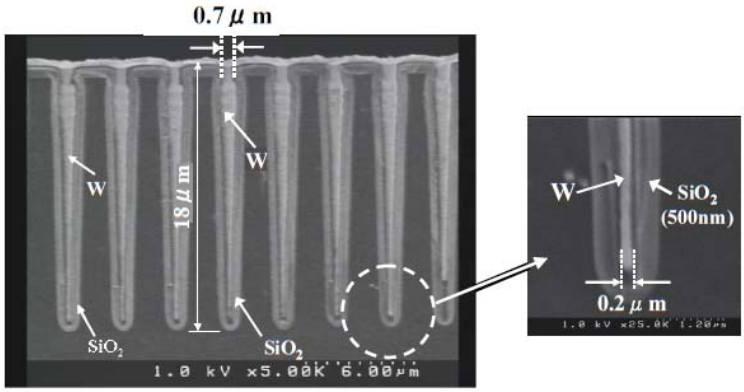


Adsorption time
tad = 1sec
Reduction time
tred = 15sec
Evacuation time
tevc1 =5sec
tevc2 = 5sec
Deposition temperature
350℃

Y. Igarashi and M. Koyanagi et al., SSDM, pp.34-35, 2001.

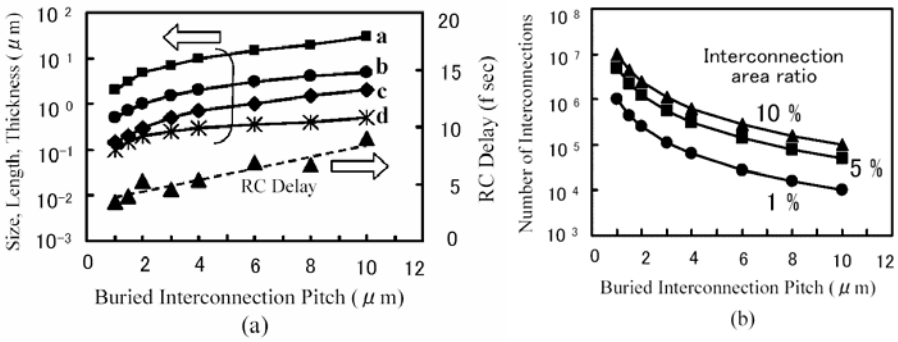
Tungsten Profiles in Trenches with Diameter of 0.7 μ m

(Via first or Via before BEOL)



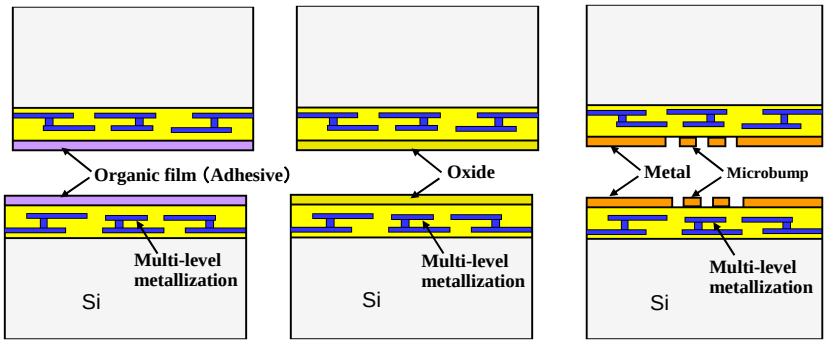
Adsorption time; tad = 1sec
Reduction time; tred = 15sec
Evacuationtime; tevc1 =5sec, tevc2 = 5sec
Deposition temperature; 350℃

Scaling Capability of Buried Interconnection (TSV)



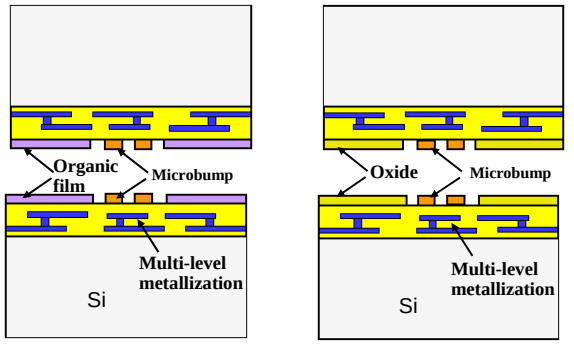
a: buried interconnection length, b: microbump size,
c: buried interconnection diameter, d: insulator thickness.

Various Kinds of Wafer Bonding Methods (1)



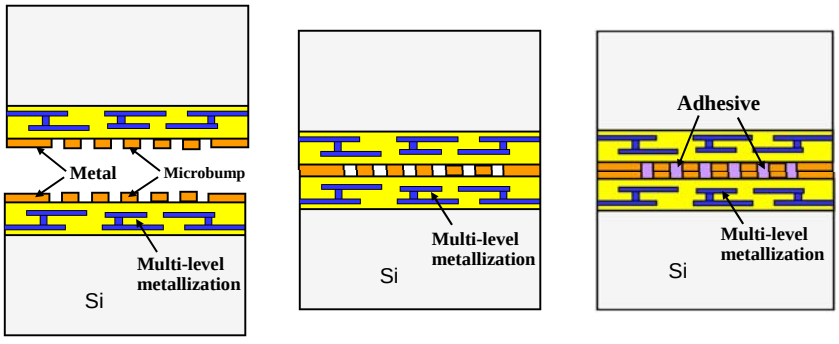
Adhesive Bonding | Direct Oxide Bonding | Direct Metal Bonding

Various Kinds of Wafer Bonding Methods (2)



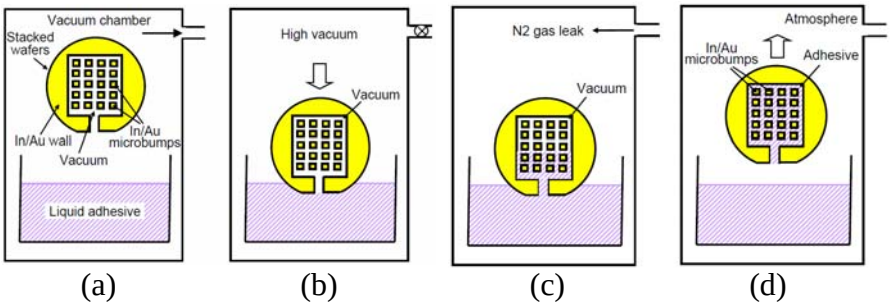
Adhesive/ Metal Bonding Oxide/ Metal Bonding

Various Kinds of Wafer Bonding Methods (3)
(Tohoku University)



Wafer Alignment Temporary Bonding (Metal Bonding) Adhesive Injection

Wafer Bonding Using Adhesive Injection Method



Adhesive Injection Process Flow

T. Matsumoto and M. Koyanagi et al, SSDM, pp.460-461, 1997.

3D LSI Test Chips Fabricated in Tohoku University

- 3-layer stacked image sensor chip (IEDM, 1999)
  Wafer bonding (Wafer non-transfer with TSV)
- 3-layer stacked memory chip (IEDM, 2000)
  Wafer bonding (Wafer non-transfer with TSV)
- 3-layer stacked artificial retina chip (ISSCC, 2001)
  Wafer bonding (Wafer non-transfer with TSV)
- 3-layer stacked microprocessor chip (Cool Chips, 2002)
  Wafer bonding (Wafer non-transfer with TSV)
- 10-layer stacked memory chip (IEDM, 2005)
  Chip-to-wafer bonding (Self assembly with TSV)
- 38-layer stacked test chip (IEDM, 2007)
  Reconfigured wafer-to-wafer bonding (Self assembly with TSV)

3D LSI Prototype Chips Fabricated in Tohoku Univ.

3D image sensor chip

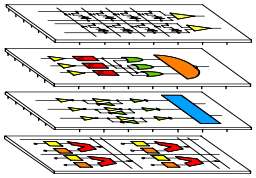
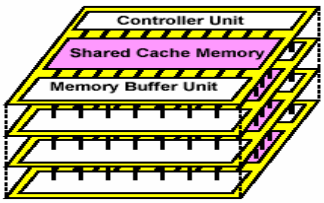


Image Sensor
AMP & ADC
Register
Processor

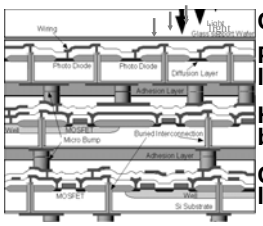
H. Kurino, M. Koyanagi *et al.*, IEDM (1999)

3D shared memory



K. W. Lee, M. Koyanagi *et al.*, IEDM (2000)

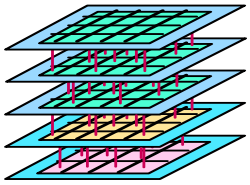
3D artificial retina chip



Quartz glass
Photoreceptor layer
Horizontal cell & bipolar cell layer
Ganglion cell layer

M. Koyanagi *et al.*, ISSCC (2001)

3D microprocessor chip



DRAM
DRAM
DRAM
SRAM
Processor

T. Ono, M. Koyanagi *et al.*, IEEE COOL Chips (2002)

Real-Time Image Processing System with 3D Stacked Structure

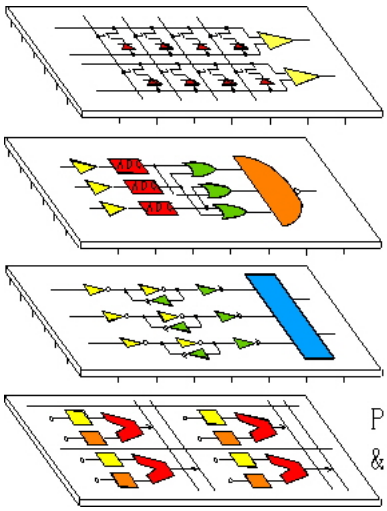


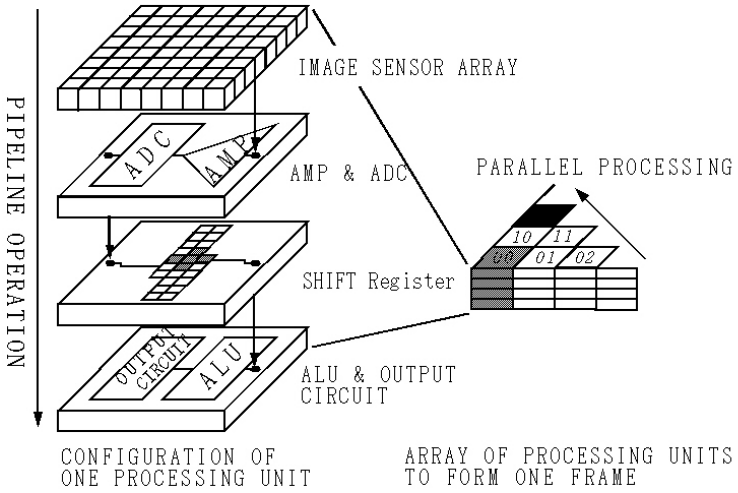
IMAGE SENSOR ARRAY

AMPLIFIER & ADC

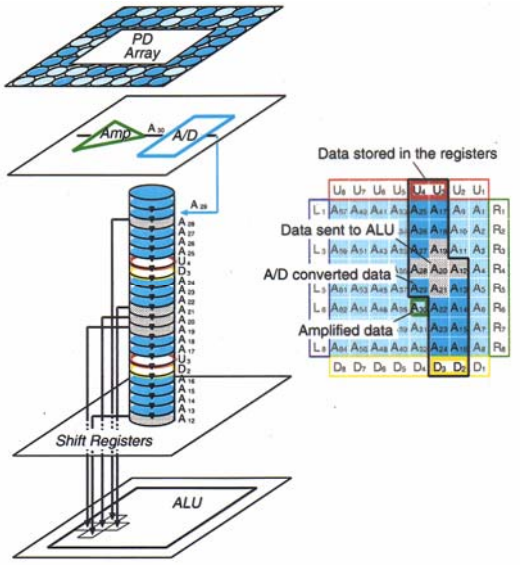
DATA LATCH & MASKING

PROCESSOR ARRAY & OUTPUT CIRCUIT

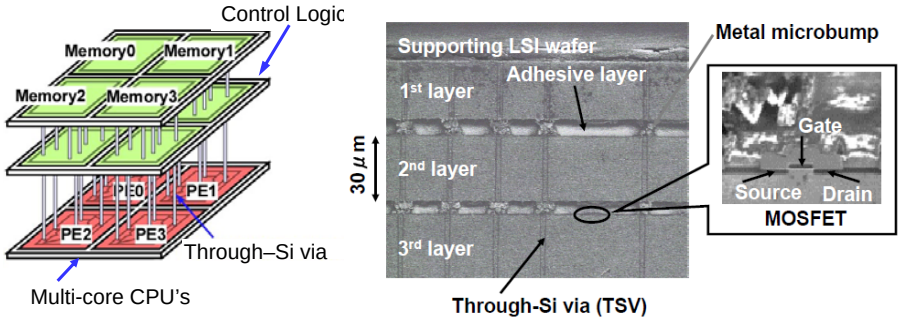
System Structure



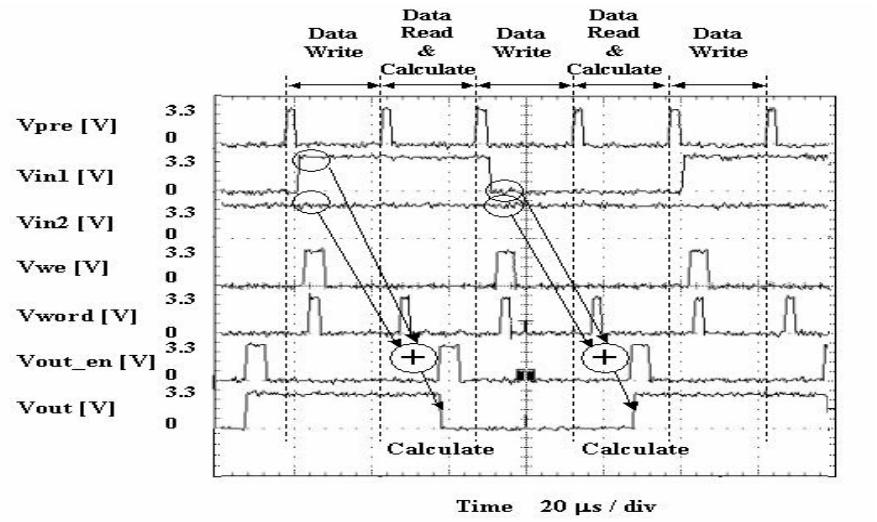
Data Flow in Processing Unit



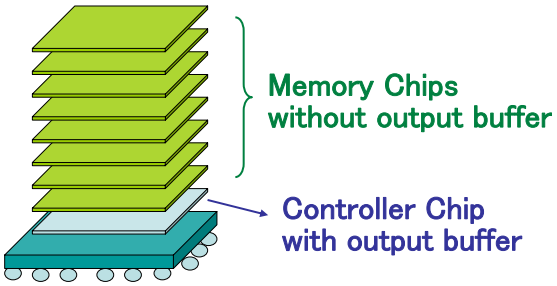
SEM Cross-Sectional View of 3-D Microprocessor Chip Fabricated by Wafer-to-Wafer Bonding



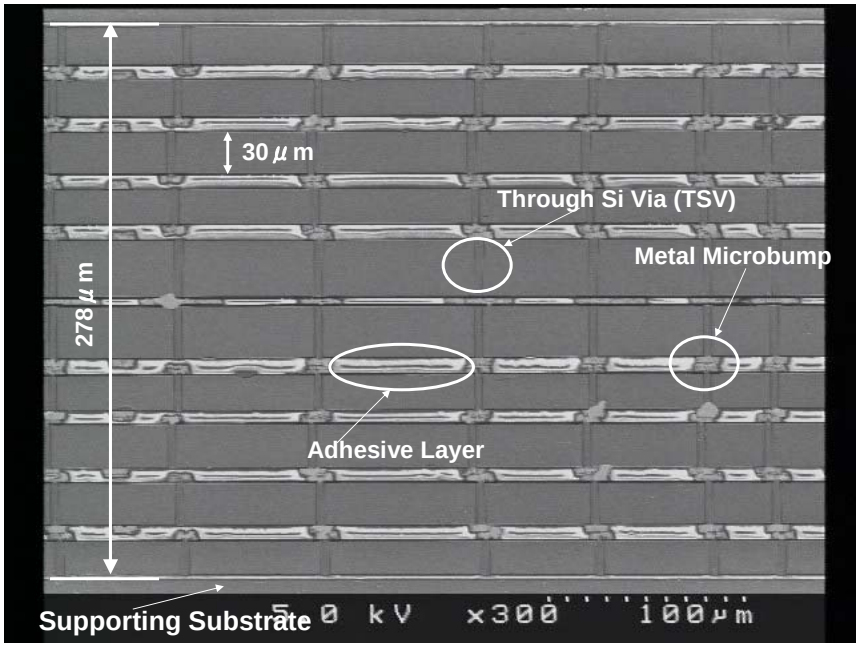
Measured Waveforms of 3-D Microprocessor Test Chip (SRAM layer: 3.3V, Processor layer: 2.5V)



3-D Memory with TSV



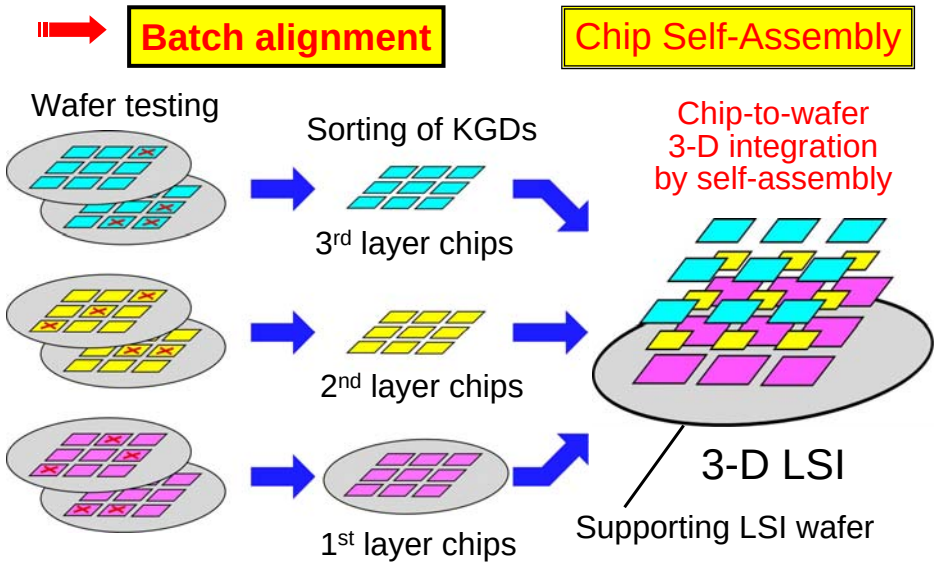
SEM Cross Section of 3-D LSI with 10 Stacked Layers



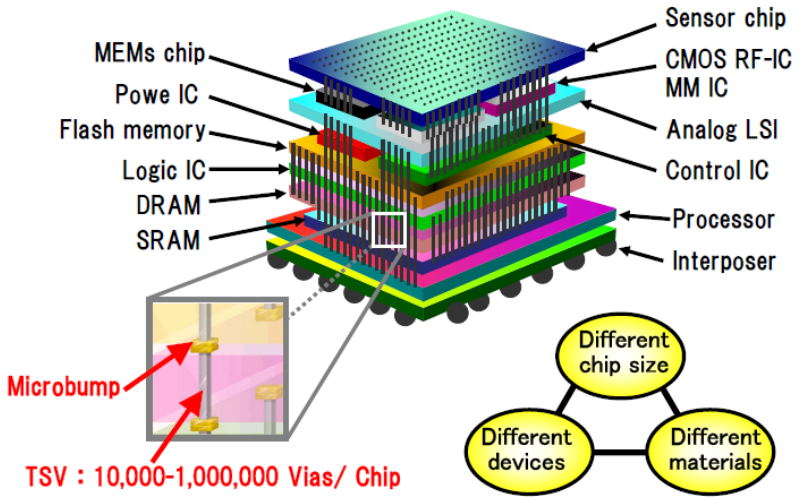
Comparison of 3D Integration Technologies

Stacking methods	Chip-on-chip	Chip-on-wafer	Wafer-on-wafer	Reconfigured wafer-on-wafer
Production throughput	Extremely Low	Low (pick & place)	High	High (self-assembly)
Production yield	High	High	Low	High
Flexibility in chip size	High	High	Low	High
Applications	Packaging	Processor, Memory, MEMS, etc.	DRAM	Processor, Memory, MEMS, etc.

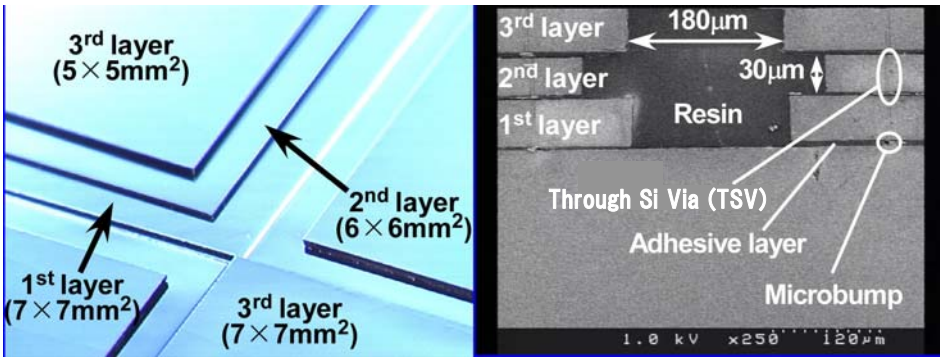
3-D Technology Based on New Chip-to-Wafer Bonding in Tohoku University : Super-Chip Integration



Configuration of Super-Chip



SEM Micrograph of 3-Layer Stacked Chips with Different Chip Size Fabricated Using Self-Assembly Method



Summary

1. **We developed a wafer-to-wafer 3D integration technology using metal microbump bonding and adhesive injection.**
2. **Various 3D LSI test chips were successfully fabricated and their basic operations were confirmed.**
3. **We developed a super-chip integration technology using a chip self-assembly method.**
4. **We succeeded in simultaneously self-assemble a number of known-good-dies (KGD's) with high alignment accuracy of 0.5 μ m.**
5. **We successfully stacked 38 test chips by a self-assembly method**