Addressing Thermal and Power Delivery Bottlenecks in 3D Circuits

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3D technologies

Wire-bonded 3D package Face-to-face Capacitive coupling
Inductive coupling Through-Silicon via - bulk Through-Silicon via - SOI

[R. Davis et al.]
Thermal and Power Supply Integrity in 3D

- Higher current density, faster current transients
  - Thermal management: heat sink limitations
  - Power delivery issues: via resistance, limited number of supply pins

- Chart showing current per power pin (2D) from ITRS
  - Current per power pin (2D) – ITRS
  - Year: 2005 to 2025
  - Current per Power Pin (mA): 0 to 300

Diagram comparing 2D and 3D power pin configurations.
Resolving processor-memory bottlenecks

[Loi et al., DAC06]
Thermal challenges

- Each layer generates heat
- Heat sink at the end(s)

- Simple analysis
  - Power(3D)/Power(2D) = \( m \)
    - \( m = \# \text{ layers} \)
  - Let \( R_{\text{sink}} \) = thermal resistance of heat sink
  - \( T = \text{Power} \times R_{\text{sink}} \)
    - \( m \) times worse for 3D!

- And this does not account for
  - Increased effective \( R_{\text{sink}} \)
  - Leakage power effects, T-leakage feedback

- Thermal bottleneck: a major problem for 3D
  - Impacts delays, power, reliability
Power delivery challenges

- Each layer draws current from the power grid
- Power pins at the extreme end tier(s)

- Simple analysis
  - \( \text{Current}(3D)/\text{Current}(2D) = m \)
    - \( m = \# \text{ layers} \)
  - Let \( R_{\text{grid}} = \text{resistance of power grid} \)
  - \( V_{\text{drop}} = \text{Current} \times R_{\text{grid}} \)
    - \( m \) times worse for 3D!

- And this does not account for
  - Increased effective \( R_{\text{grid}} \)
  - Leakage power effects, increased current due to T-leakage feedback

- Power bottleneck: a major problem for 3D
  - Impacts delays, reliability
Thermal analysis and optimization in 3D
Full-chip thermal analysis

- Macroscale thermal analysis for full-chip profiles
  - (as against nanoscale analysis, considering electron-phonon interactions)
- Heat generation
  - Switching gates/blocks act as heat sources
  - Time constants for heat of the order of ms or more
- Thermal equation:
  \[ k_i \nabla^2 T + g(x, y, z, t) = \rho c_p \frac{\partial T(x, y, z, t)}{\partial t} \]
- Boundary conditions corresponding to the ambient, heat sink, etc.
- Self-consistency: Power = f(Temperature), Temperature = g(Power)
Thermal analysis

- Thermal equation: partial differential equation

\[ k_t \nabla^2 T + g(x, y, z, t) = \rho c_p \frac{\partial T(x, y, z, t)}{\partial t} \]

- Boundary conditions corresponding to the ambient, heat sink, etc.
- Self-consistency
  - Power is a function of temperature, which is a function of power!
  - Often handled using iterations
The finite difference approach

• Finite difference method
  – Thermal-electrical analogy
    • Can find “thermal resistance” and “thermal capacitance” values between element nodes
  – Steady state:
    \[ G \mathbf{T} = \mathbf{P} \]
    • \( G \) is the thermal conductance matrix
    • \( \mathbf{T} \) and \( \mathbf{P} \) are the temperature and power density vectors

• Same structure as power grid optimization problem, which has been widely addressed in IC design. Can adapt solution techniques
  – Multigrid, etc.
  – New - fast random walk based solvers
The finite element approach

- Discretize into elements; use polynomial interpolation based on values at nodes
- Use “element stamps” and assemble these into a larger matrix
- Steady state: apply boundary conditions to get \( K \mathbf{T} = \mathbf{P} \)
- Rectangular symmetries for on-chip geometries
  - Stamp for a hexahedral element
    - Rows and columns correspond to nodes 1 - 8

\[
[k] = \begin{bmatrix}
+A & +B & +C & +D & +E & +F & +G & +H \\
+B & +A & +D & +C & +F & +E & +H & +G \\
+C & +D & +A & +B & +G & +H & +E & +F \\
+D & +C & +B & +A & +H & +G & +F & +E \\
+E & +F & +G & +H & +A & +B & +C & +D \\
+F & +E & +H & +G & +B & +A & +D & +C \\
+G & +H & +E & +F & +C & +D & +A & +B \\
+H & +G & +F & +E & +D & +C & +B & +A \\
\end{bmatrix}
\]
Performance optimization in 3D

- Minimize power usage
- Rearrange heat sources
- Thermal vias/conduits
- Improved heat sinking
3D placement: One approach

Objective Function: 
\[ \sum_{\text{each net } i} [WL_i + \alpha_{ILV} \cdot ILV_i] + \alpha_{TEMP} \sum_{\text{each cell } j} [R_{j}^{cell} P_{j}^{cell}] \]

- Global Placement
  - Partitioning Placement
  - Thermal Aware Net Weighting
  - Thermal Resistance Reduction Nets
- Coarse Legalization
  - Global Moves/Swaps
  - Local Moves/Swaps
  - Cell Shifting
- Detailed Legalization

[Goplen, DAC07]
Thermal resistance reduction nets

![Diagram of thermal resistance reduction nets with IOPad 1, Cell 3, Cell 4, IOPad 2, Cell 2, Cell 5, and Heat Sink]

Runtime vs. Circuit size

Run Time versus Number of Cells

- Thermal Placement
- Regular Placement

\[ y = 0.0002x^{1.1909} \]

\[ y = 0.0002x^{1.1749} \]

[Source: Goplen, DAC07]
Heat removal in 3D through thermal vias

- **Thermal vias**
  - Electrically isolated vias
  - Used for heat conduction

- **Thermal via regions**
  - Contains thermal vias
  - Predictable obstacle for routing
  - Variable density of thermal vias
Thermal via insertion

Temperature Profile: Before  Temperature Profile: After  Thermal Via Regions

[Goplen, ISPD05]
3D routing with integrated thermal via insertion

• Build good heat conduction path through dielectric:
  – Thermal vias: interlayers vias dedicated to thermal conduction.
  – Thermal wires: metal wires improves lateral heat conduction.
  – Thermal vias + thermal wires a thermal conduction network.
• Thermal wires compete with lateral signal wire routing.
• Thermal vias: large, can block lateral signal routing capacity.

[Zhang, ASPDAC06]
3D Power Delivery
Traditional power delivery

- **Requirements**
  - $V_{dd}$, GND signals should be at correct levels (low V drop)
  - Electromigration constraints
    - Current density must never exceed a specification
    - For each wire, $I_i/w_i < J_{\text{spec}}$
  - $dl/dt$ constraints
    - Need to manage $dl/dt$ to reduce inductive effects

- **Techniques for meeting constraints**
  - Widening wires
  - Using appropriate topologies
  - Adding decoupling capacitances

- **Already challenged for 2D technologies**
  - Reliable power delivery hard
  - Decaps get leaky

- **Circuit + CAD approaches necessary**
Multi-story power supply

Improved supply noise due to:
- Reduced current magnitude
- Cleaner middle supply voltage

Attractive for 3D chips:
- Isolated substrate for each tier
- Chip is naturally partitioned

<table>
<thead>
<tr>
<th></th>
<th>1-story</th>
<th>2-story</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Current</strong></td>
<td>2I</td>
<td>I</td>
</tr>
<tr>
<td><strong>Voltage</strong></td>
<td>Vdd</td>
<td>2Vdd</td>
</tr>
<tr>
<td><strong>Power</strong></td>
<td>2Vdd·I</td>
<td>2Vdd·I−Δ</td>
</tr>
<tr>
<td><strong>Noise</strong></td>
<td>15%Vdd</td>
<td>&lt; 8%Vdd</td>
</tr>
</tbody>
</table>
CAD solutions for multi-story circuits
Multi-story power supply: Test layout

- A test layout in MITLL’s SOI process shows a 5.3% area overhead
Overall Design Flow

- Netlist and block information
- Floorplanning involving regular modules and regulators
- Assigning modules using a graph partition-based algorithm
- Module assignment
Estimating the wasted power

\[ x_i = \begin{cases} 
0 & M_i \text{ works between } 2V_{dd} \text{ and } V_{dd} \\
1 & M_i \text{ works between } V_{dd} \text{ and } GND 
\end{cases} \]

\[ I_R(t) = \sum_{i=1}^{n} I_i(t) \times (1 - 2x_i) \]

\[ \min I_R^2(t) = \left( \sum_{i=1}^{n} I_i(t) \right)^2 - 4 \sum_{i<j} I_i(t)I_j(t) \times (x_i + x_j - 2x_ix_j) \]

\[ \max S = \sum_{i<j} I_i(t)I_j(t)(x_i + x_j - 2x_ix_j) \]

\[ = 0 \text{ if } x_i = x_j \quad \text{ and } \quad = 1 \text{ if } x_i \neq x_j \]

Graph partitioning problem!
Constructing the graph

\[ w(V_i, V_j) = \left( \sum_{k=1}^{K} \frac{S_{ik} S_{jk}}{S_i S_j} \right) I_i(t) I_j(t) \]
3D benchmarks

- Exercised on GSRC floorplanning benchmarks
- Largest floorplan has 300 modules
- Comparison with (slow)simulated annealing method

<table>
<thead>
<tr>
<th>Layer</th>
<th>Wasted Power/Useful Power (%)</th>
<th>Maximum IR Noise (mV)</th>
<th>Runtime (sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Partition-Based</td>
<td>Annealing</td>
<td>Partition-Based</td>
</tr>
<tr>
<td>n100Layer0</td>
<td>3.3</td>
<td>3.1</td>
<td>52.8</td>
</tr>
<tr>
<td>n100Layer1</td>
<td>3.1</td>
<td>3.8</td>
<td>28.9</td>
</tr>
<tr>
<td>n100Layer2</td>
<td>3.7</td>
<td>5.7</td>
<td>45.4</td>
</tr>
<tr>
<td>n200Layer0</td>
<td>8.7</td>
<td>6.4</td>
<td>55.2</td>
</tr>
<tr>
<td><strong>n200Layer1</strong></td>
<td><strong>5.6</strong></td>
<td><strong>6.4</strong></td>
<td><strong>62.1</strong></td>
</tr>
<tr>
<td>n200Layer2</td>
<td>5.6</td>
<td>7.1</td>
<td>77.4</td>
</tr>
<tr>
<td>n300Layer0</td>
<td>4.7</td>
<td>4.5</td>
<td>61.1</td>
</tr>
<tr>
<td>n300Layer1</td>
<td>6.3</td>
<td>6.3</td>
<td>33.4</td>
</tr>
<tr>
<td>n300Layer2</td>
<td>5.4</td>
<td>4.6</td>
<td>46.5</td>
</tr>
</tbody>
</table>

Runtime Comparison: \( > 10^3 \times \text{speedup over SA} \)
Switched decaps for active noise cancellation

- Charge provided by switched decap (=0.5C·Vdd+CΔVdd/2) much larger than that of a conv. decap (=2C·ΔVdd)
- For a supply noise (ΔVdd) of 5%, effective decap value is boosted by 7.5X
Supply noise cancellation: Results

- 200pF switched decap has lower noise than 1200pF conventional decap
- 5–11X boost over passive decaps depending on supply noise magnitude
Proof of concept: Switched decap test chip

- **Technology**: 0.13µm CMOS
- **Quiescent Current**: 0.54mA
- **Regulation Freq.**: 10MHz-300MHz
- **Regulator Area (w/o decap)**: 100µmx70µm
- **Regulator Area (w/ 300pF decap)**: 190µmx220µm
- **Total Die Area**: 0.9mmx1.8mm

- 2.2-9.8dB reduction of the 40MHz resonant noise using 100-300pF switched decaps
## Comparison with passive damping

<table>
<thead>
<tr>
<th>Swdecap Value</th>
<th>Resonant Suppression</th>
<th>Equivalent Passive Decap</th>
<th>Decap Boost</th>
</tr>
</thead>
<tbody>
<tr>
<td>100pF</td>
<td>2.2dB</td>
<td>500pF</td>
<td>5X</td>
</tr>
<tr>
<td>200pF</td>
<td>5.5dB</td>
<td>1500pF</td>
<td>7.5X</td>
</tr>
<tr>
<td>300pF</td>
<td>9.8dB</td>
<td>3500pF</td>
<td>11X</td>
</tr>
</tbody>
</table>
MIM decaps

• Capacitance density*
  – CMOS — 17.3 fF/µm² at 90nm
  – MIM — 8.0 fF/µm²

• Leakage density*
  – CMOS — 1.45e-4 A/ cm²
  – MIM — 3.2e-8 A/cm²

• Congestion
  – MIM — routing blockage

• Described in paper 2D-4, ASPDAC09

* Numbers deduced from Roberts et al., IEDM05 and PTM simulations
Conclusion

• Power, thermal issues are major bottlenecks for 3D integration
  – The root cause of both is closely related
• Solutions can come through low power design, physical design, and novel circuit techniques