Efficiently Finding the ‘Best’ Solution with Multi-Objectives from Multiple Topologies in Topology Library of Analog Circuit

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FUJITSU

Outline

- Introduction
- The ‘best’ solution of topology library of analog circuit
  - Abstract Pareto-front of topology library
  - Find the best solution for specification
- Experiment
- Summary

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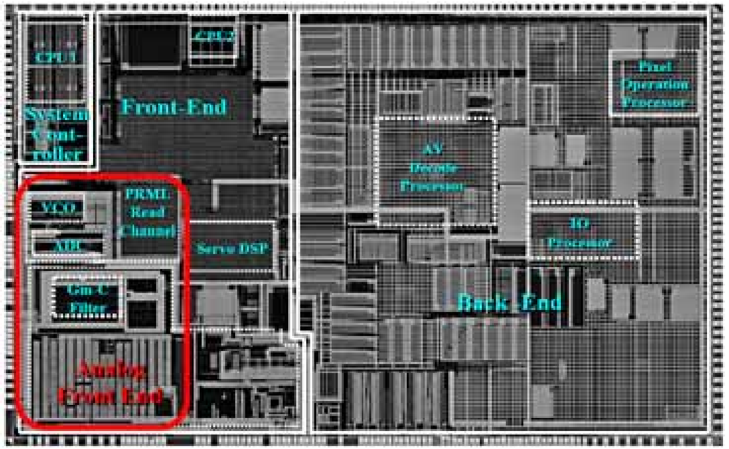
Background



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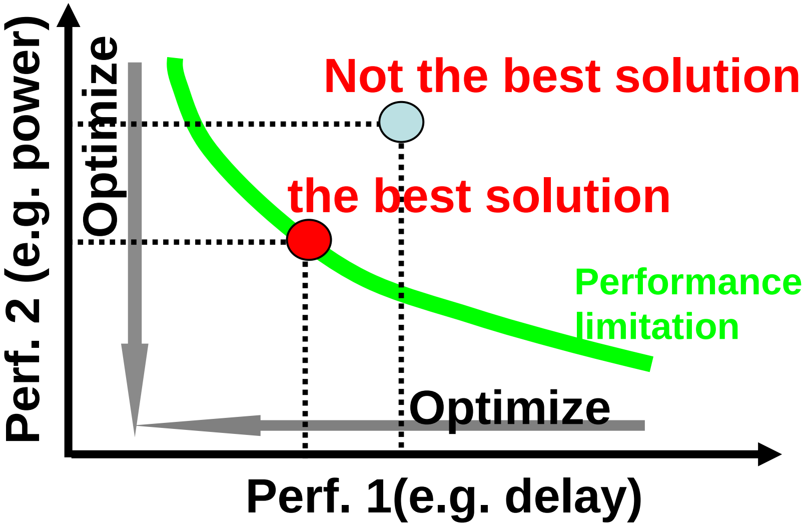
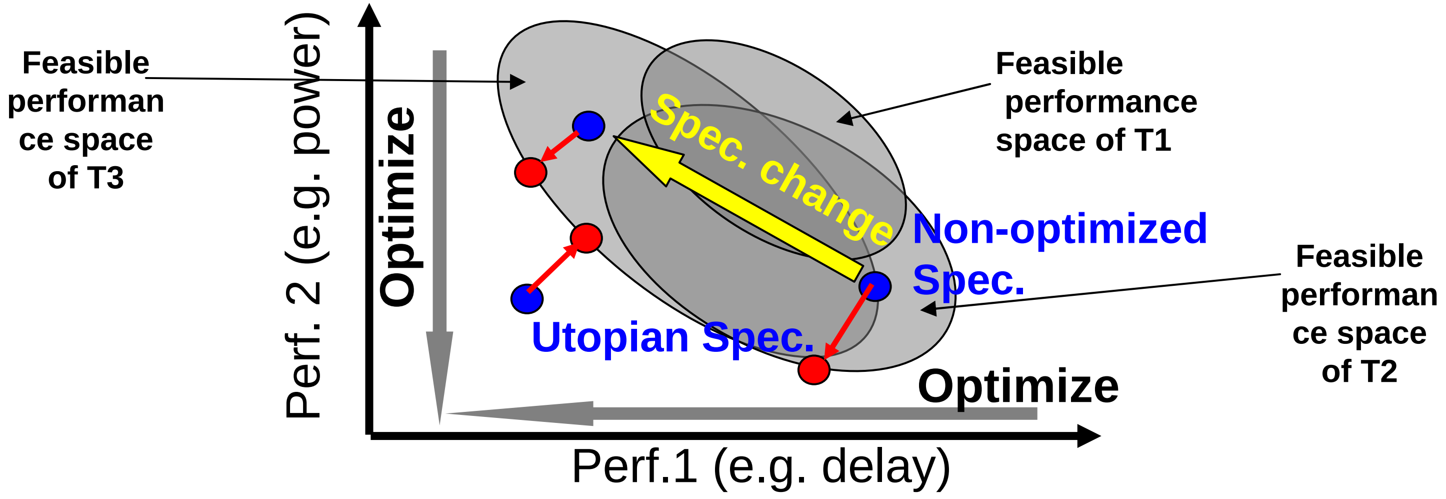


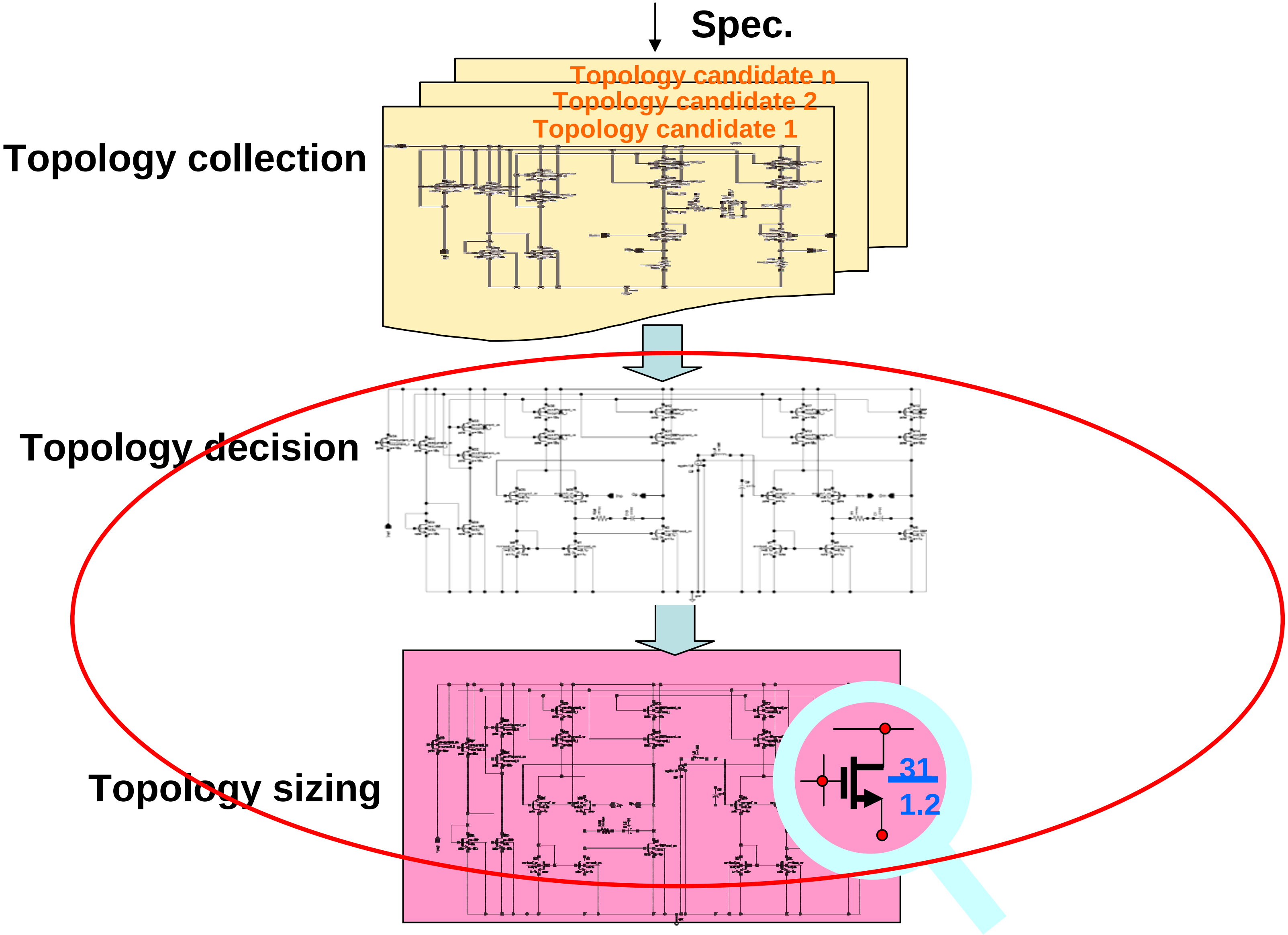
- Only the chips with higher performance, shorter developing-period can win the market
- Each block is needed to provide its best performances
- Best solution of a block
  - Contribute better performance to system
  - Relax the constraints of other blocks

Motivation



- Specification assignments in early design stage
- For analog block, the first assigned specification maybe non-optimized or Utopia
- The specification may also be changed
- We provide an *automatic* design method to efficiently find the *best* solution with *multi-objectives* from *multiple candidates* of analog topologies

Analog Circuit Design Flow



Spec.

Topology candidate n

Topology candidate 2

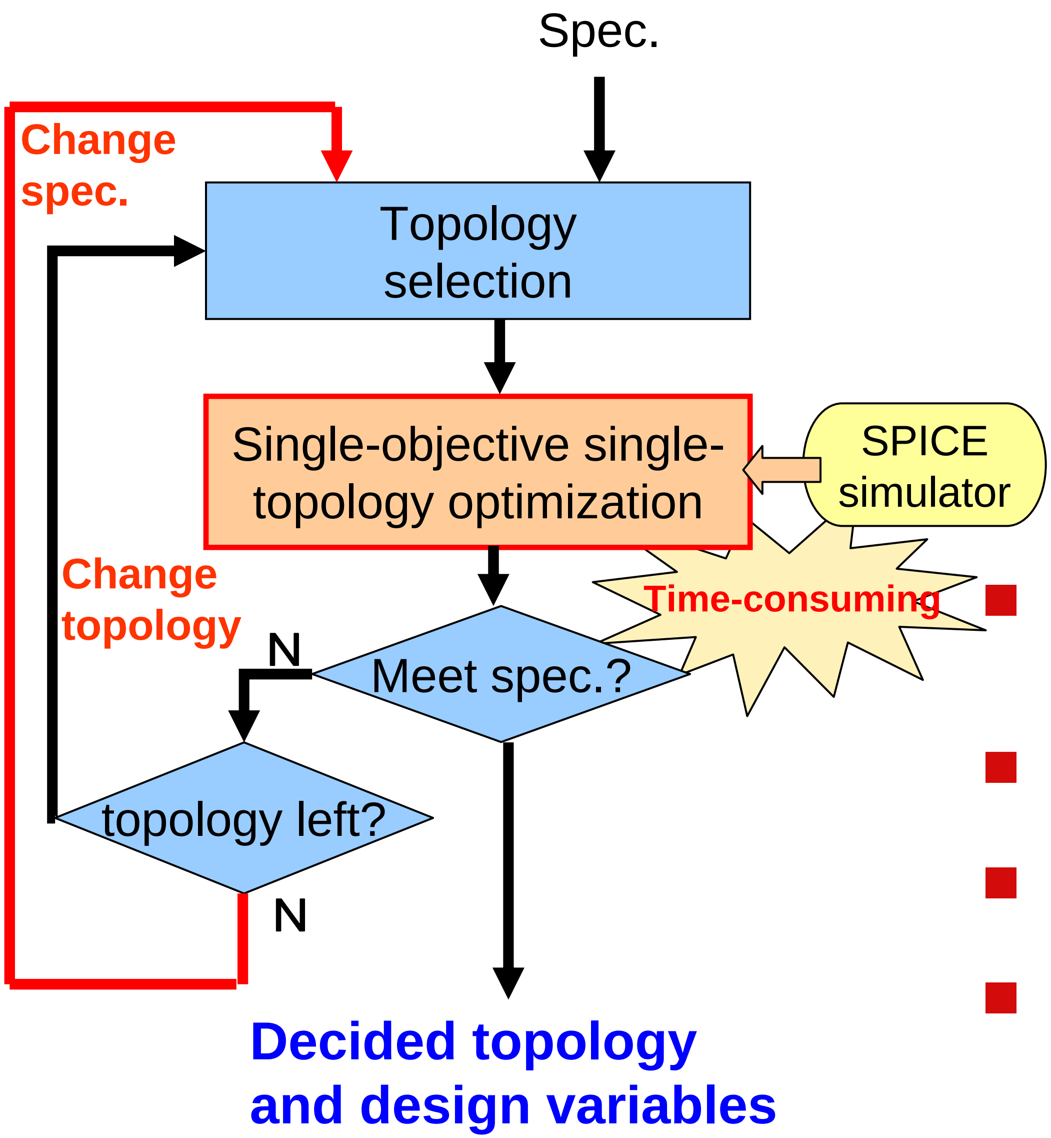
Topology candidate 1

Topology collection

Topology decision

Topology sizing

Traditional Flow for Automatic Design


Spec.

Change spec.

Topology selection

Single-objective single-topology optimization

SPICE simulator

Time-consuming

Change topology

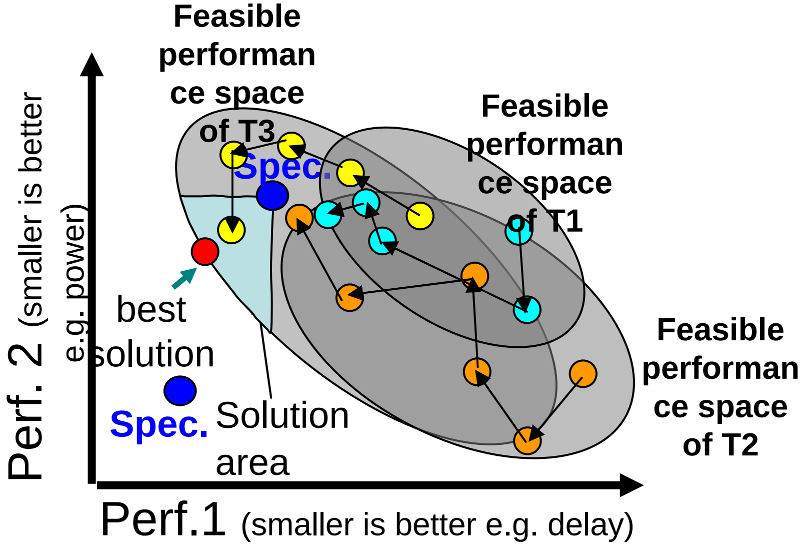
N

Meet spec.?

topology left?

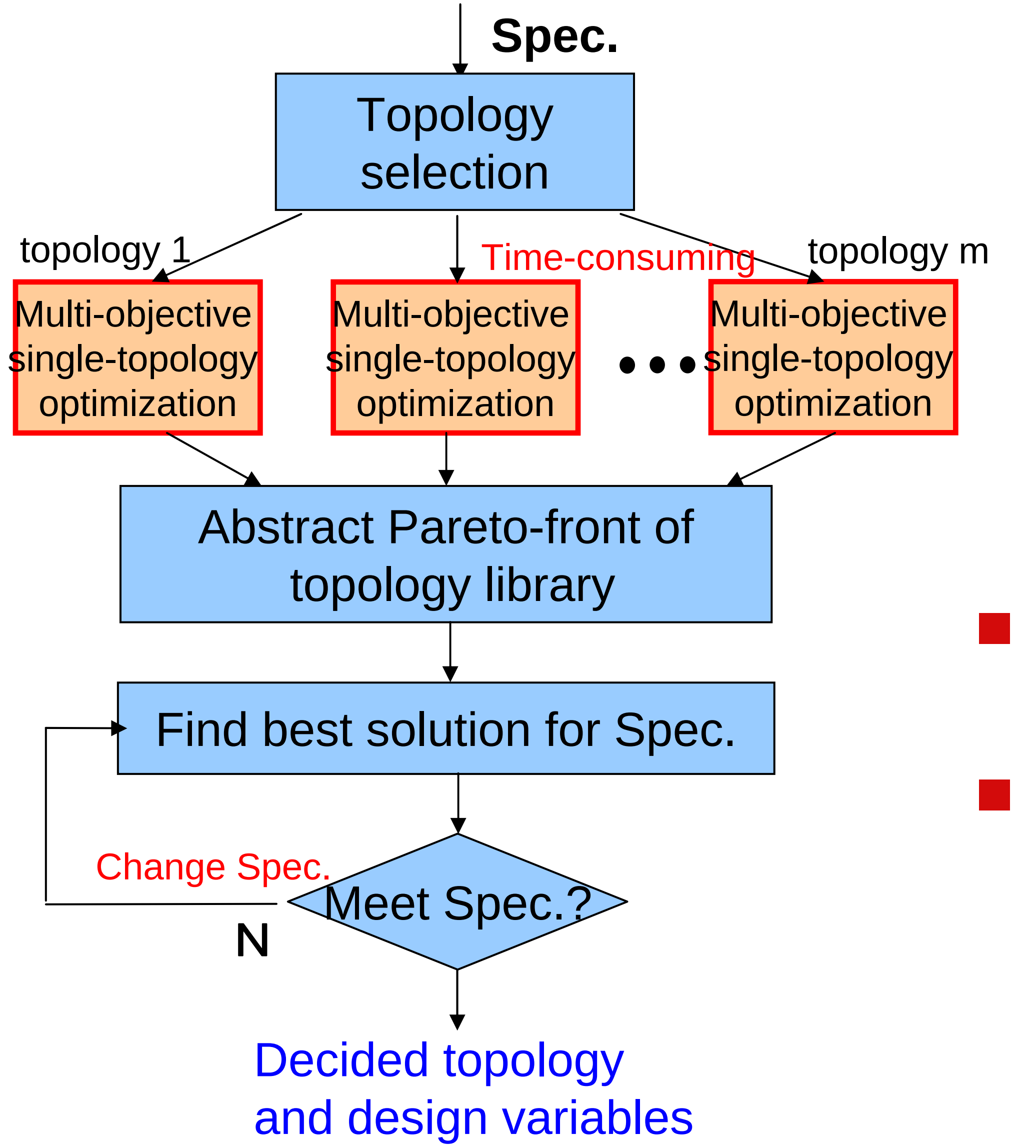
N

Decided topology and design variables

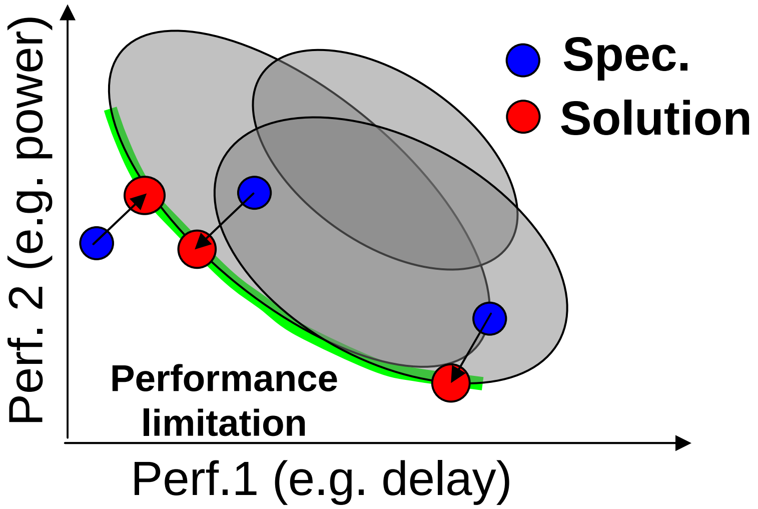

Feasible performance space of T3
Feasible performance space of T1
Feasible performance space of T2
Spec.
best solution
Spec.
Solution area
Perf. 2 (smaller is better e.g. power)
Perf.1 (smaller is better e.g. delay)

- This flow works well to find a solution when the specification is achievable
- Assignment of a ***good* achievable specification** is difficult
- Inefficient when specification is changed
- The output solution may not be the *best solution* that the topologies can provide

The Flow of This Work

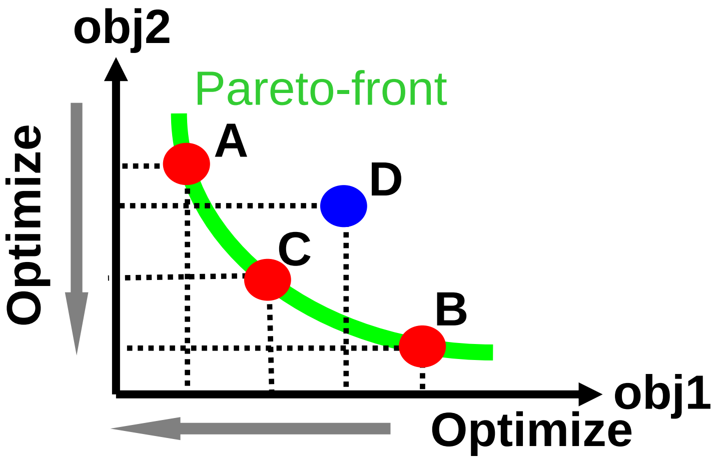


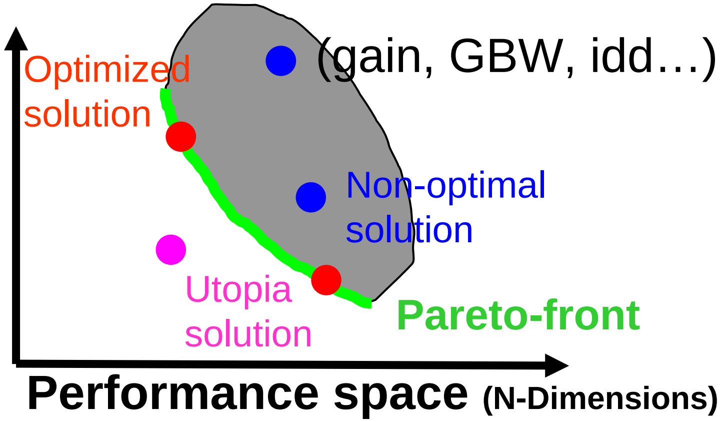
Spec.
Topology selection
topology 1
Time-consuming
topology m
Multi-objective single-topology optimization
Multi-objective single-topology optimization
• • •
Multi-objective single-topology optimization
Abstract Pareto-front of topology library
Find best solution for Spec.
Change Spec.
Meet Spec.?
N
Decided topology and design variables



- Perform the time-consuming optimization **not** depending on the detailed specification
- Efficient to find the best solution from multiple topologies especially in early design stage while the specification is not clear

Review: Pareto-Front





- The non-dominated solution set for multi-objective optimization problem regarding to all objective
  - A dominate B $\boldsymbol{a} \prec \boldsymbol{b} \Leftrightarrow \forall_{\boldsymbol{i}} a_i \le b_i \wedge \exists_i a_i < b_i$
- The optimized solution set in analog performance space
- In design, we naturally choose the optimized solution on the Pareto-front

Related Works

- On abstraction algorithm of Pareto-front
  - [Stehr 03], [Mueller 05], [Tiwary 06], [Yu 07]
- On high-level design using Pareto-front
  - [Tiwary 04], [Eeckelaert 07]
- On sizing analog circuit through multiple topologies using Pareto-front
  - [Mcconaghy 07]
  - The final decision is manually made depending on the 2D or 3D Pareto-front graph
- We need an efficient tool to automatically find the best solution of multi-dimensional specification from the multiple candidates of analog topologies.

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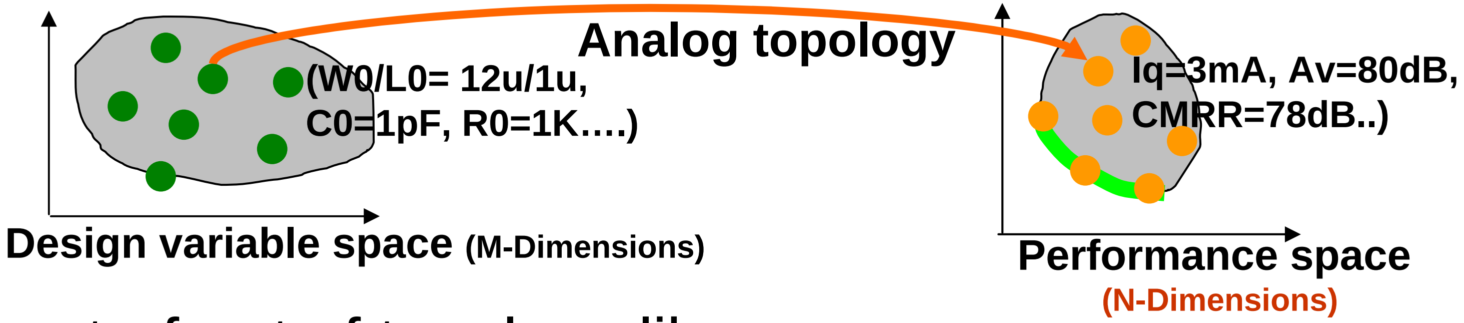
Pareto-Front of Topology Library

- Pareto-front of an analog topology



Analog topology

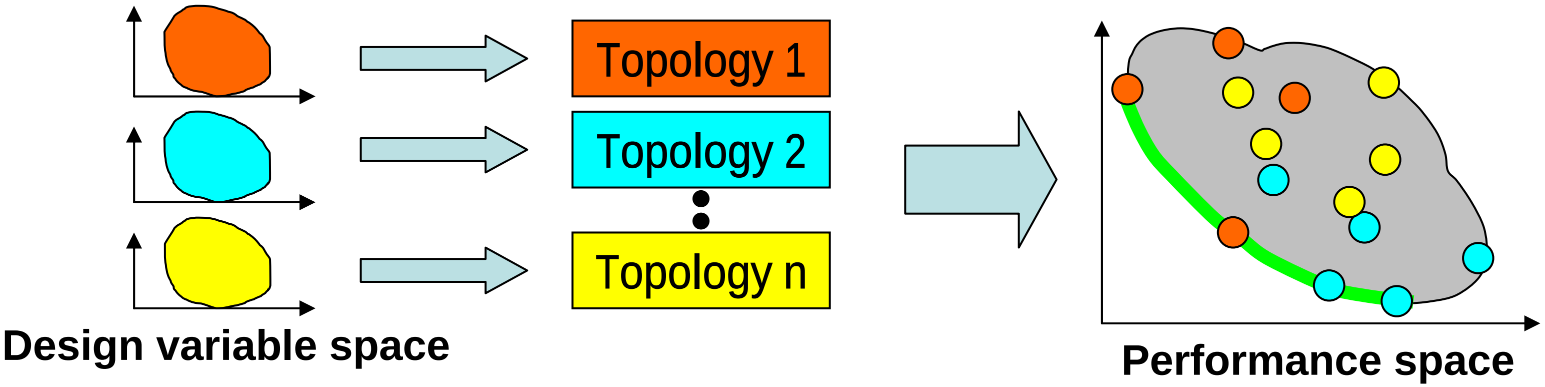
(W0/L0= 12u/1u, C0=1pF, R0=1K….)

Iq=3mA, Av=80dB, CMRR=78dB..)

Design variable space (M-Dimensions)

Performance space (N-Dimensions)

- Pareto-front of topology library
  - A set of optimized solutions
  - Non-dominated solutions of the achievable performances of all the topologies in the library



Topology 1

Topology 2

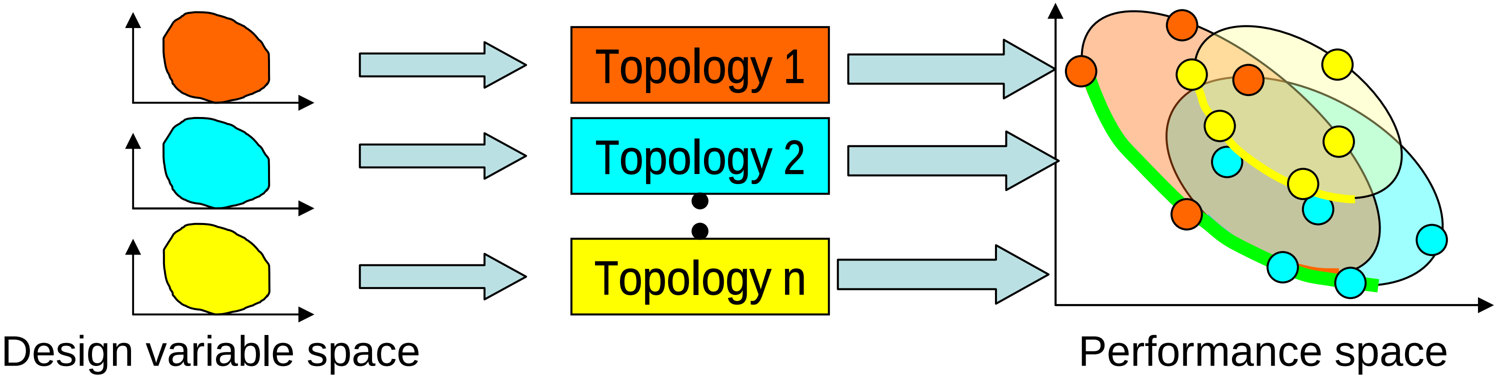
Topology n

Design variable space

Performance space

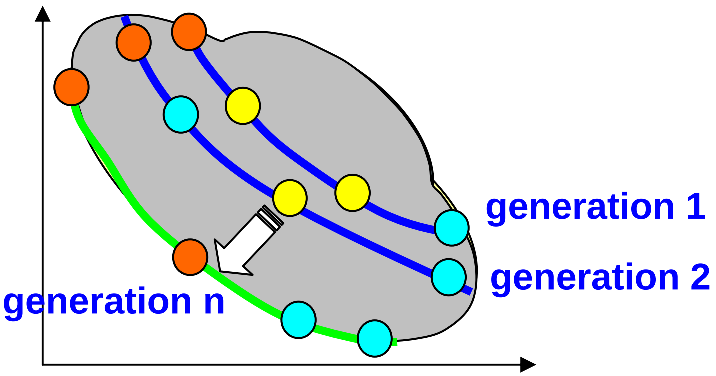
Theorem

- Theorem
  - The points on Pareto-front of topology library are also on one of the Pareto-fronts of individual topology in the library.
- Divide the abstraction of Pareto-front of topology library into two steps
  - Abstract Pareto-front of each topology
  - Abstract the Pareto-front of library

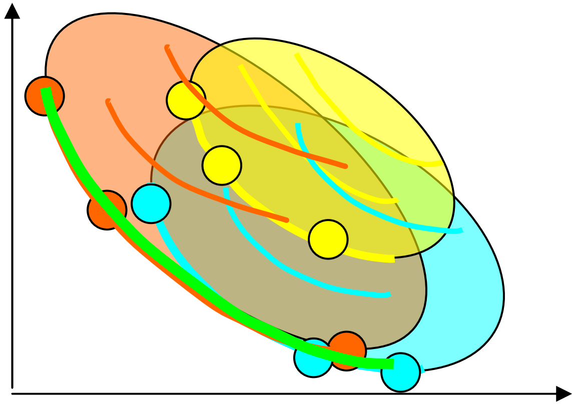


Abstract Pareto-Front Using Theorem

- NSGA (Non-dominated Sorting Genetic Algorithm)
  - Iteratively search the optimized solutions (generation) to find the sampling points on Pareto-front
- Abstracting the Pareto-front of topology library by definition
  - Once a topology in library is changed, the evaluations of all topologies have to be repeated



- Abstracting the Pareto-front by the theorem
  - Only need to evaluate the changed topology
  - Note that the number of evaluated data is proportional to the number of design variables, it is efficient when some of topologies in the library are changed



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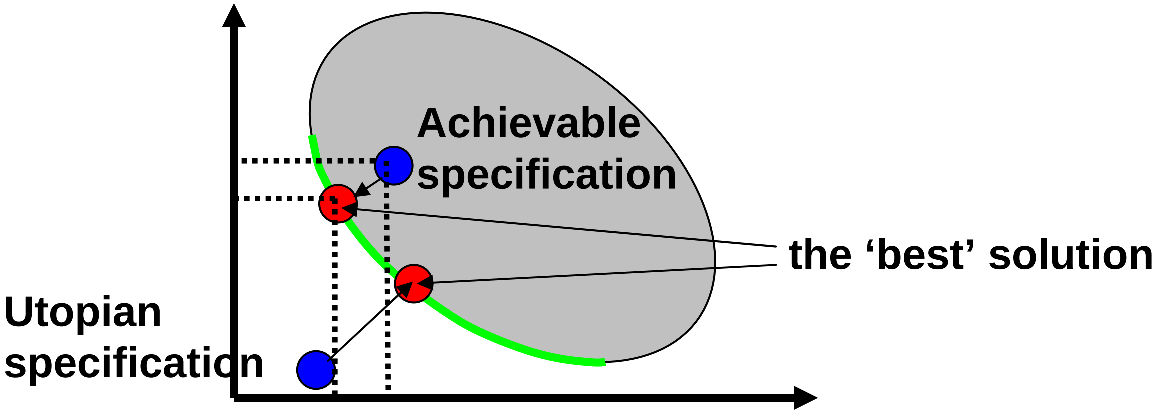
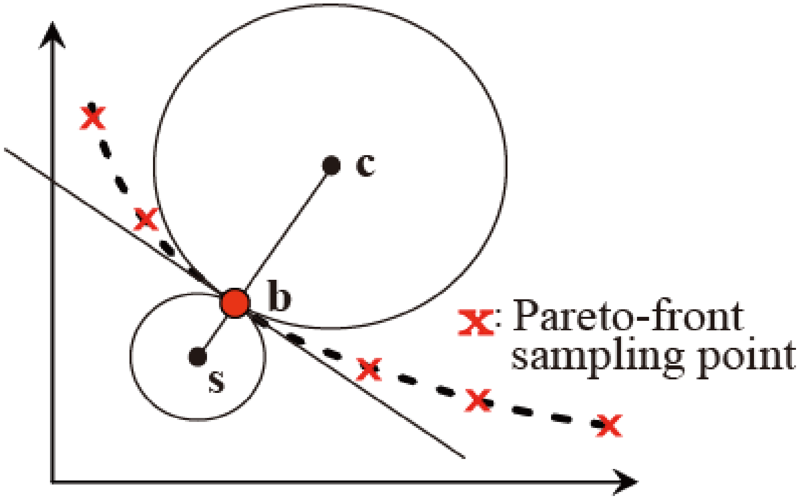
Definition of the ‘Best’ Solution

- The ‘best’ solution
  - The point on Pareto-front which is nearest to the specification in normalized distance
  - Superior or equal to the achievable specification in all the performances
  - Achievable solution which is nearest to the Utopian specification



Collinearity Theorem

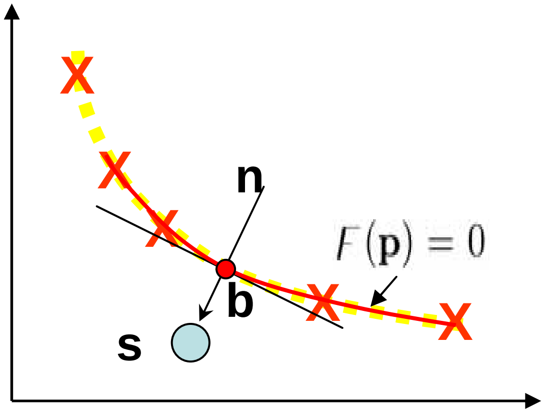
- Collinearity theorem [Kasprzak 01]
  - The internal point on Pareto-front b is the best solution if and only if the specification s, b and the instantaneous center c are collinear.

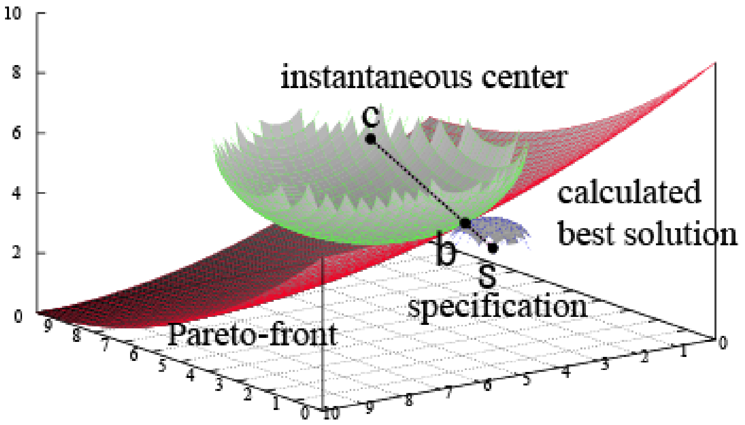


Calculate the Best Performance

- Calculate the best performance having N-dimensions
  - Model Pareto-front by the equation $F(\mathbf{p}) = 0$
  - Calculate the best performance by solving the equations extended from Collinearity theorem

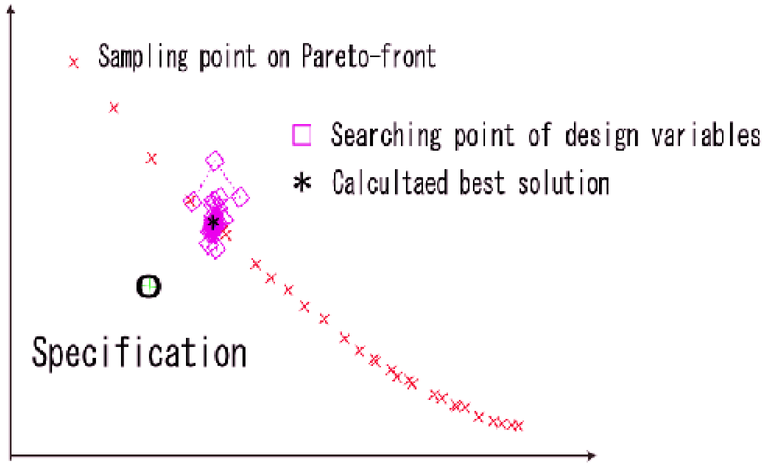
$$\begin{cases} F(\mathbf{b}) = 0 \\ \mathbf{b} = t\mathbf{n} + \mathbf{s} \\ \mathbf{n} = \nabla F(\mathbf{p}) = \left(\frac{\partial F}{\partial p_0}, \frac{\partial F}{\partial p_1}, \cdots, \frac{\partial F}{\partial p_{N-1}}\right)\Big|_{\mathbf{p}=\mathbf{b}} \end{cases}$$





Calculate the Best Solution

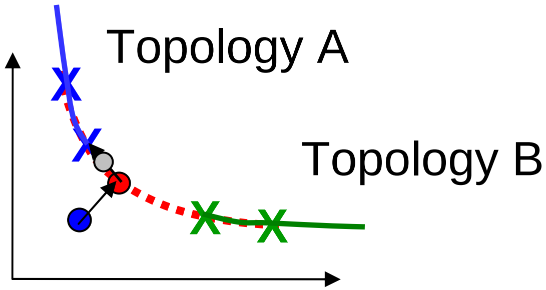
- Topology decision
  - Topology’s Pareto-front includes the best performance
- Search design variables
  - Locally model the performances pb with design variables
  - Search the design variables to minimize the normalized distance ||b-pb||
  - Example
    - Searching design variables by Nelder-Mead algorithm



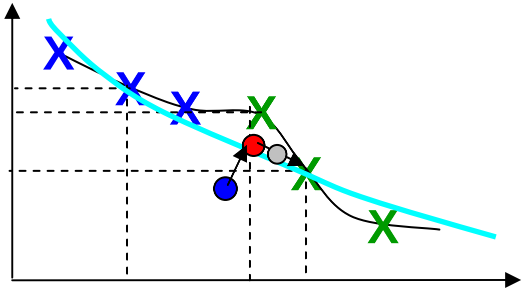
# of design variables: 5
# of specification item :2

The Best Solution

- Verify the calculated best solution via SPICE
- Interpolatively find the best solution between the calculated best solution and the best sampling point for special cases



Special case1



Special case2

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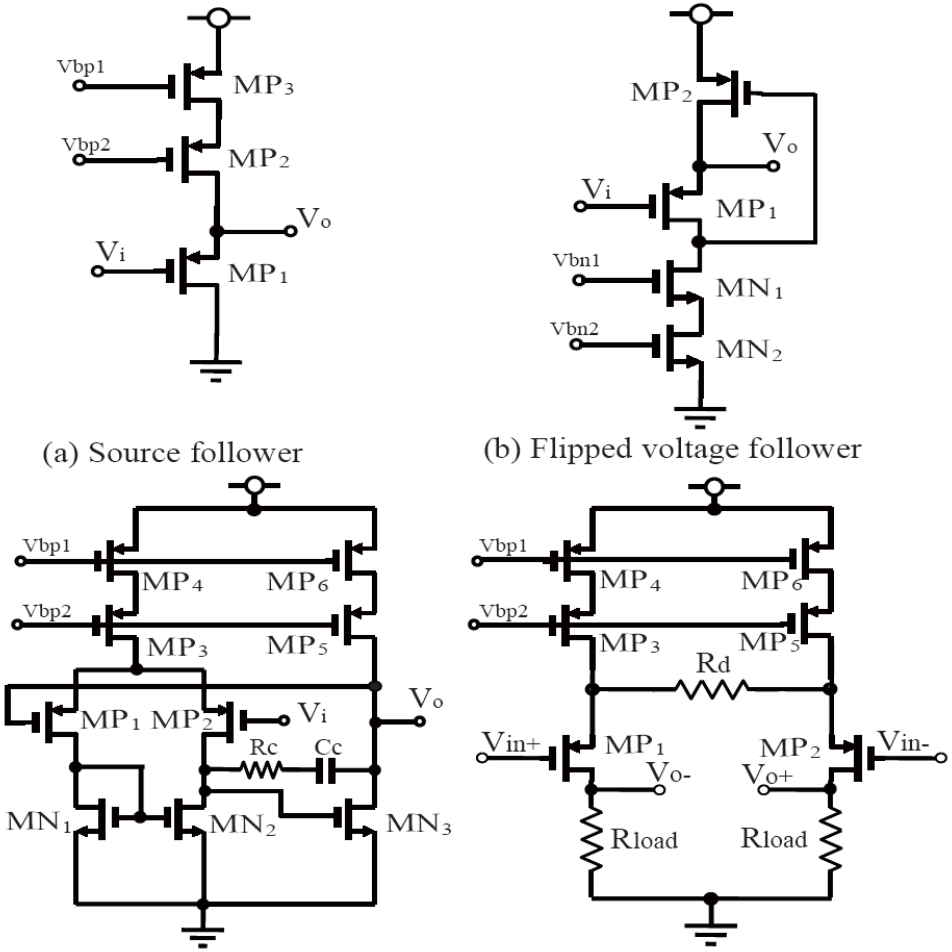
Case Study

- Analog buffer in actual ADC project for high-definition video application
- System requirements
  - Capacitance load up to 5pF
  - Power supply down to 1.05V
  - 65nm BSIM4 process parameters
- Four topologies in library
- Experiment environment
  - HSPICE simulator with high accuracy options
  - 1.1GHz Sparcv9 CPU
  - 16G memory



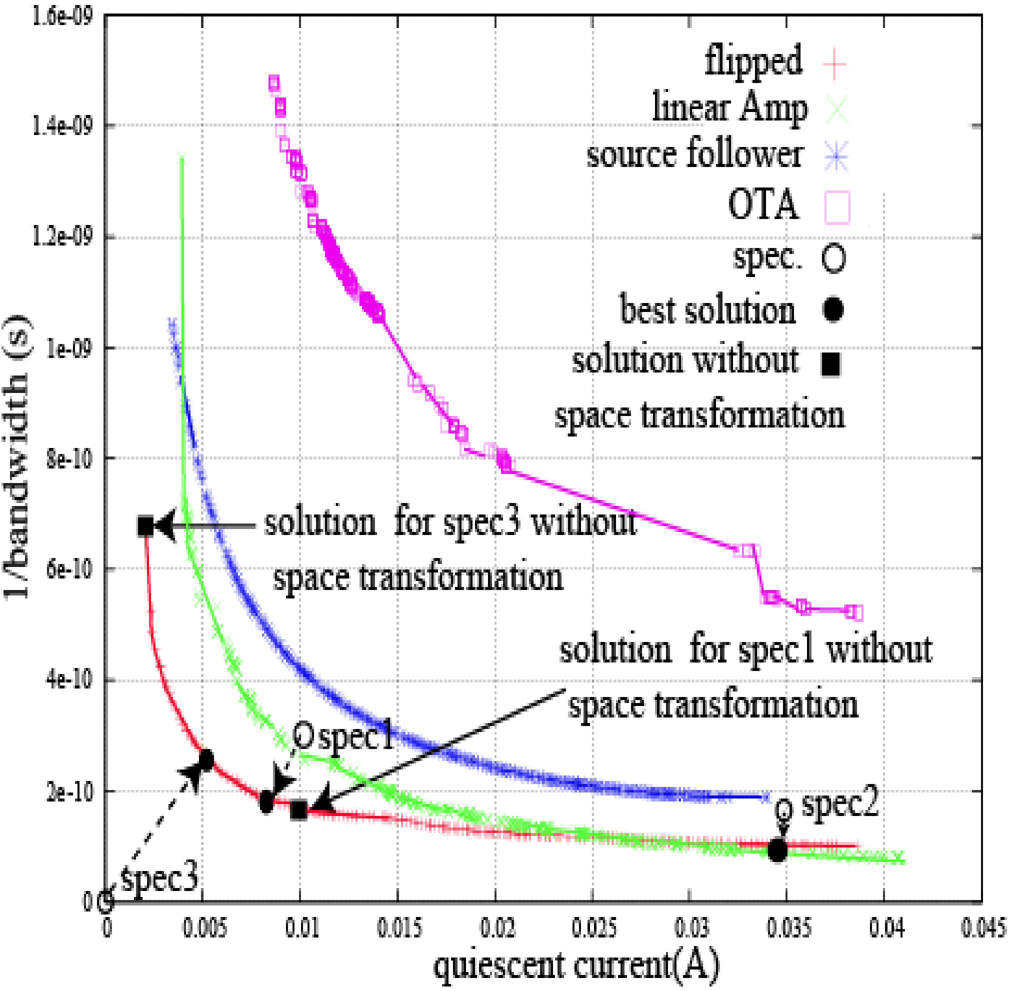
(a) Source follower

(b) Flipped voltage follower

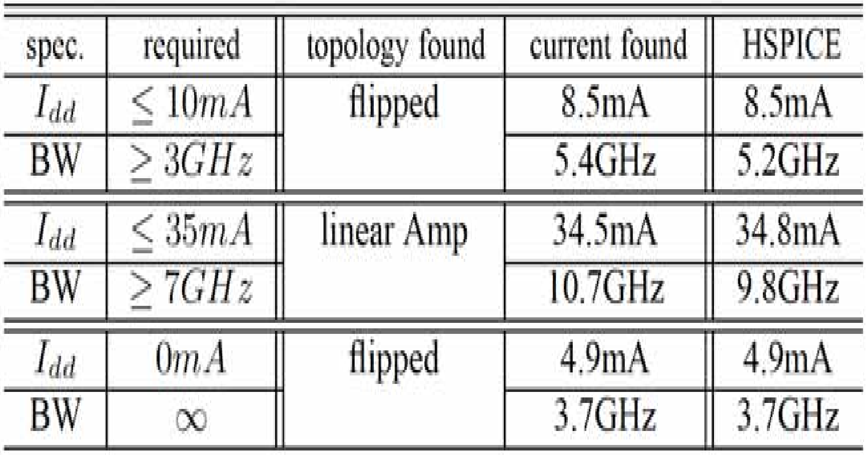
(c) Buffer using OTA

(d) Linear Amplifier

Best Solution for 2D Specification

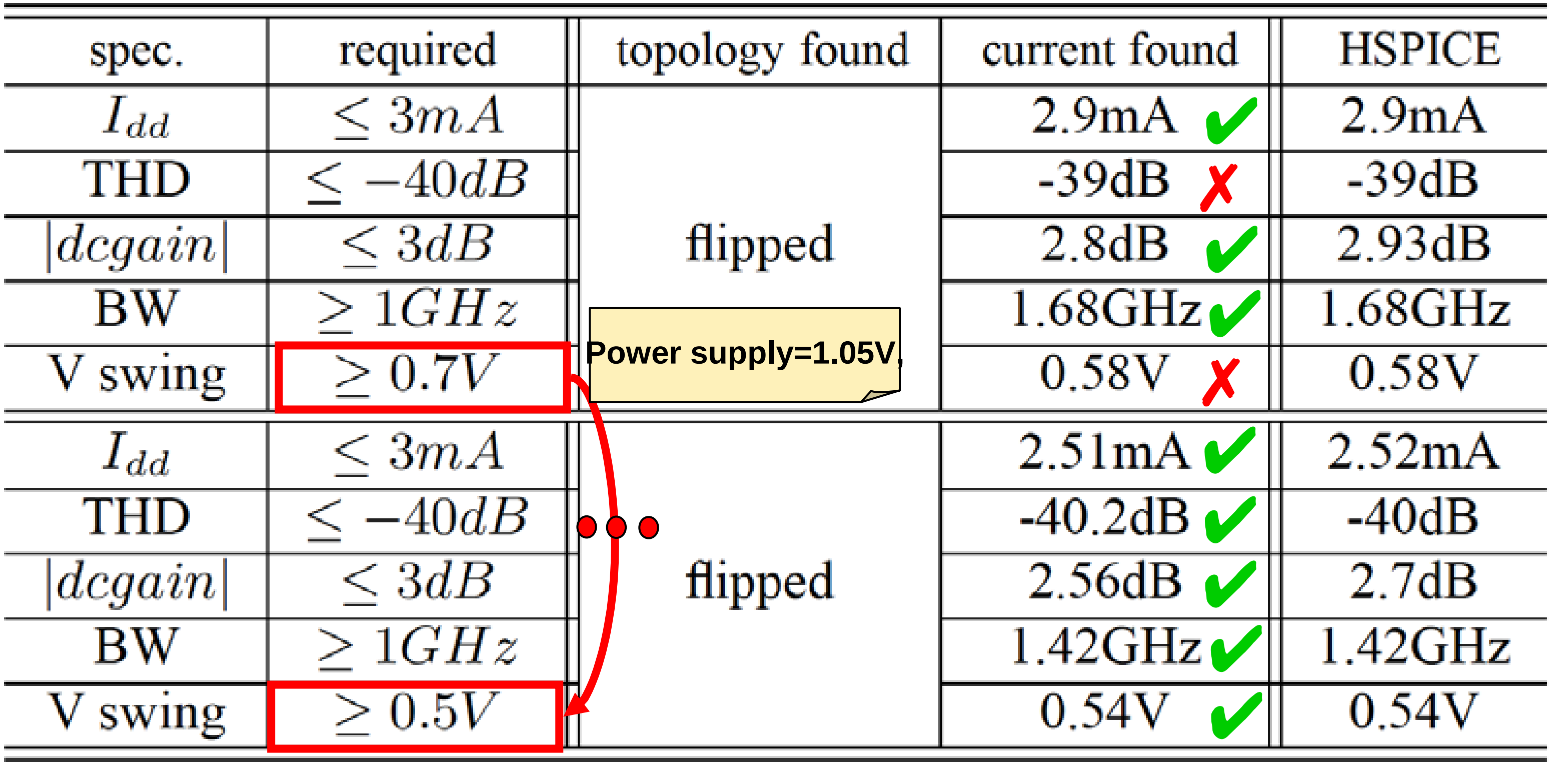


- Simulation type: transient & AC
- Pareto-front abstraction time: 32.4 hours
- Time for different specification: less than 1 minute



spec.	required	topology found	current found	HSPICE
I_{dd}	$\leq 10mA$	flipped	8.5mA	8.5mA
BW	$\geq 3GHz$		5.4GHz	5.2GHz
I_{dd}	$\leq 35mA$	linear Amp	34.5mA	34.8mA
BW	$\geq 7GHz$		10.7GHz	9.8GHz
I_{dd}	$0mA$	flipped	4.9mA	4.9mA
BW	∞		3.7GHz	3.7GHz

Best Solution for 5D Specification



spec.	required	topology found	current found	HSPICE
I_{dd}	$\leq 3mA$	flipped	2.9mA ✓	2.9mA
THD	$\leq -40dB$		-39dB ✗	-39dB
$\|dcgain\|$	$\leq 3dB$		2.8dB ✓	2.93dB
BW	$\geq 1GHz$		1.68GHz ✓	1.68GHz
V swing	$\geq 0.7V$		0.58V ✗	0.58V
I_{dd}	$\leq 3mA$	flipped	2.51mA ✓	2.52mA
THD	$\leq -40dB$		-40.2dB ✓	-40dB
$\|dcgain\|$	$\leq 3dB$		2.56dB ✓	2.7dB
BW	$\geq 1GHz$		1.42GHz ✓	1.42GHz
V swing	$\geq 0.5V$		0.54V ✓	0.54V

Power supply=1.05V,

Time for different specification: less than 1 minute

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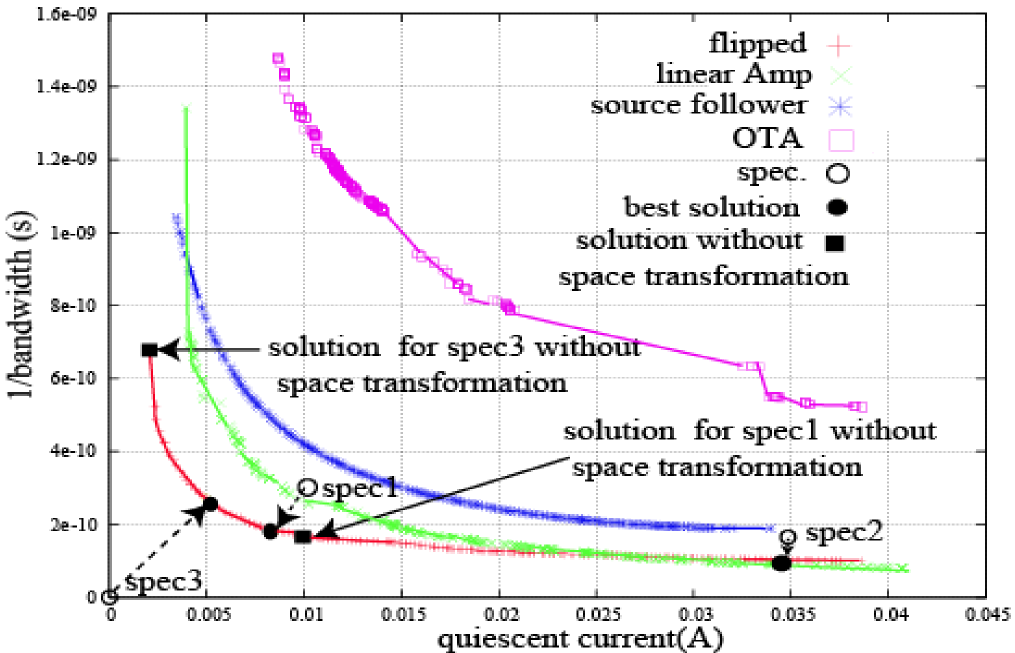
Summary

- Summaries
  - Introduce a method to automatically find the ‘best’ solution that the multiple topologies in topology library can produce
  - The efforts of time-consuming optimization stage are maximally preserved for specification and topology change
  - This method is efficient to find the non-dominated optimized solution from multiple topologies especially in early design stage
- Future works
  - Handle the variations of process and operation environment
  - Support the high-level design of mixed-signal SoC

Thank you!

Appendix: Normalization

- Space transformation
  - Affine transformation
    - **p**’ = S**p** + **a**
    - Move each point by a fixed distance in the same direction
    - Collinearity between points and the distance ratios along a line is preserved
    - Linear scaling & shift


flipped
linear Amp
source follower
OTA
spec.
best solution
solution without space transformation
solution for spec3 without space transformation
solution for spec1 without space transformation
spec1
spec2
spec3
1/bandwidth (s)
quiescent current(A)
1.6e-09
1.4e-09
1.2e-09
1e-09
8e-10
6e-10
4e-10
2e-10