Thermal-aware Post Compilation for VLIW Architectures

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Outline

- Introduction
- Motivation
- The Proposed Methods
  - Binding Method
  - Forwarding Method
- Experimental Results
- Conclusions

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Introduction (1/2)

- Transistor density and power consumption have grown rapidly.

  → Serious heat dissipation problem
- High temperature induces undesirable effects.
  - Low reliability
  - Low performance
  - High cooling costs

Introduction(2/2)

- A thermal management method needs to be developed.
  - To reduce hotspots
  - To balance the temperature distribution

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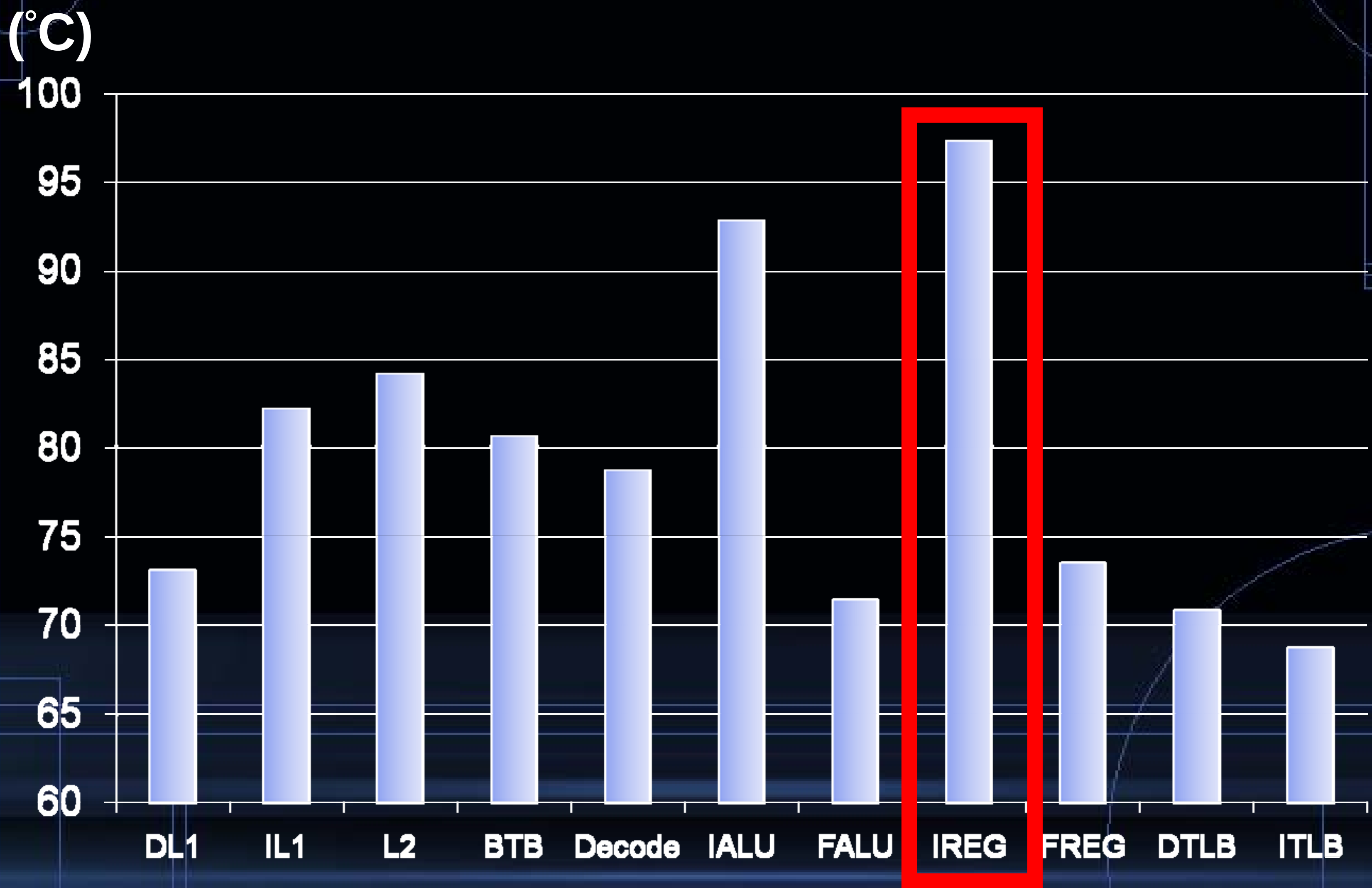
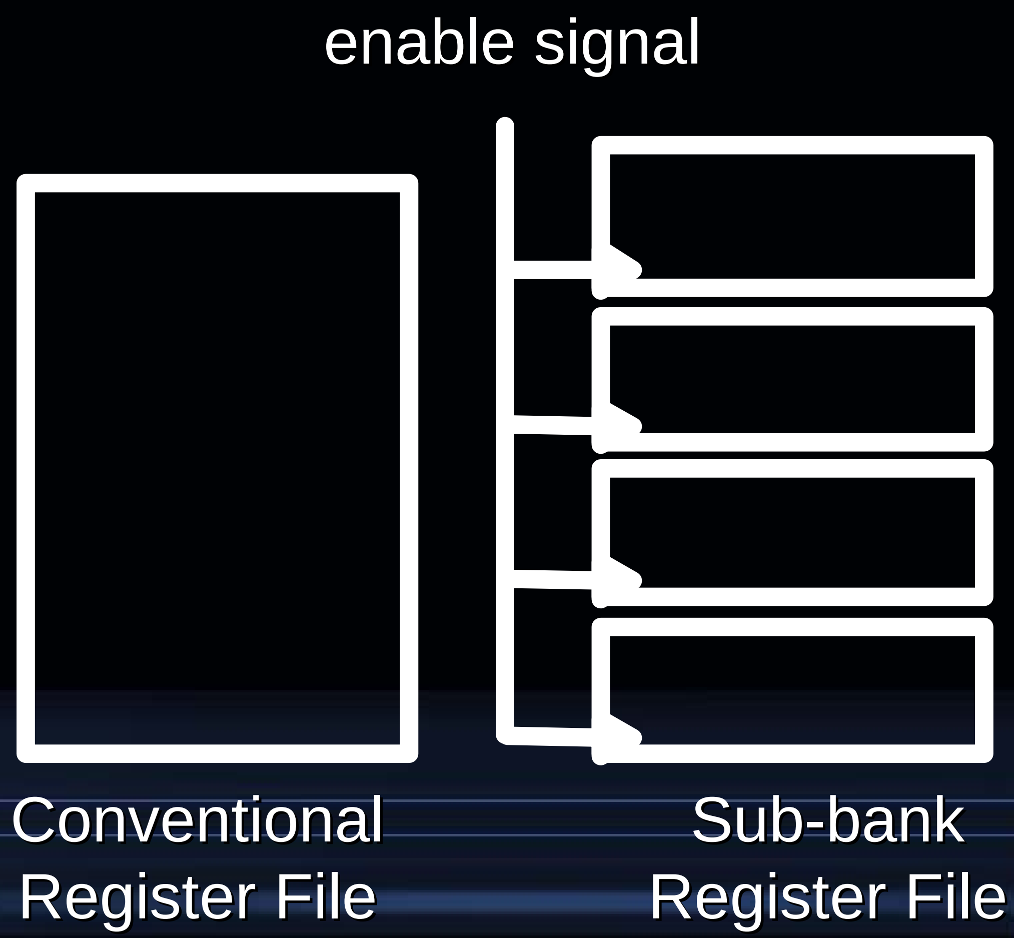
Temperature Distribution



Register File Architecture



Proposed in [Tseng 2003]

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The Proposed Method

- A static thermal management technique at compiler level.
- Target at VLIW architecture.

- We propose two techniques.
  - Register binding
    → balance the temperature of register file
  - Forwarding method
    → reduce the access count of register file

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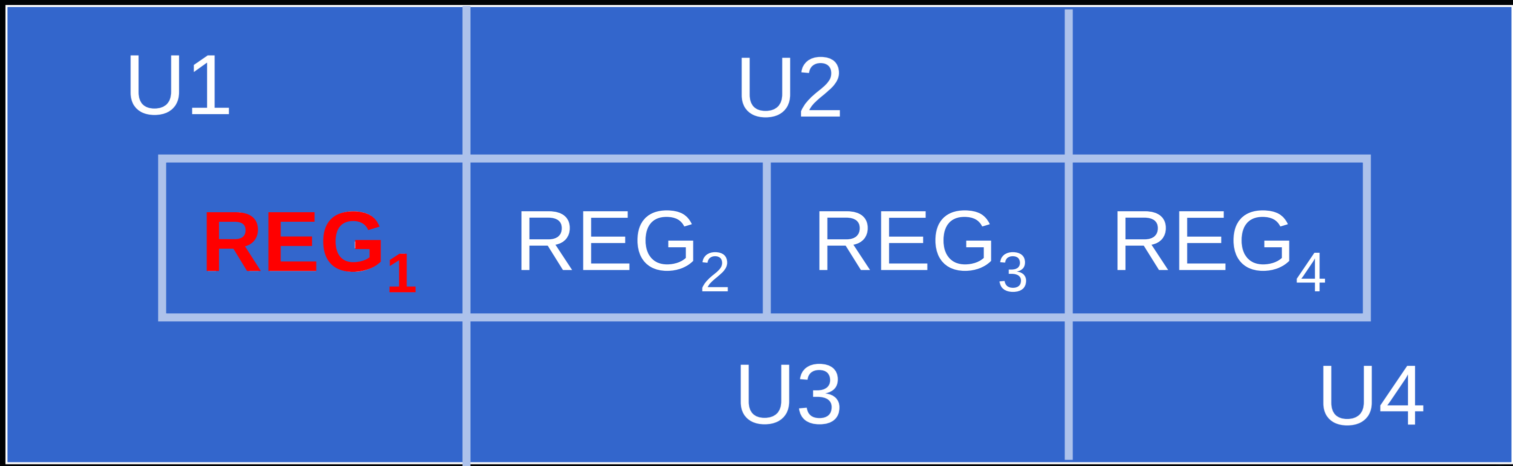
Register Binding – Simple Binding

$U1_{Temp} > U2_{Temp} = U3_{Temp} > U4_{Temp}$



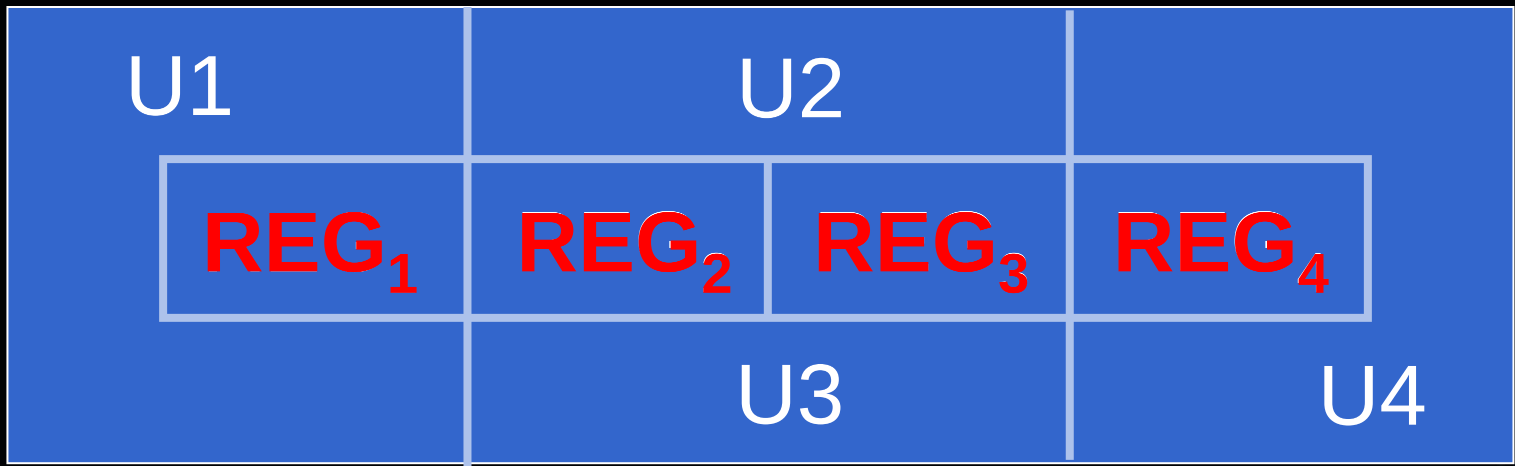
Binding order:

$REG_1 \rightarrow REG_1 \rightarrow REG_1 \rightarrow REG_1$

Hotspot : REG_1

Register Binding – Round-Robin-Like Binding

$$U1_{Temp} > U2_{Temp} = U3_{Temp} > U4_{Temp}$$



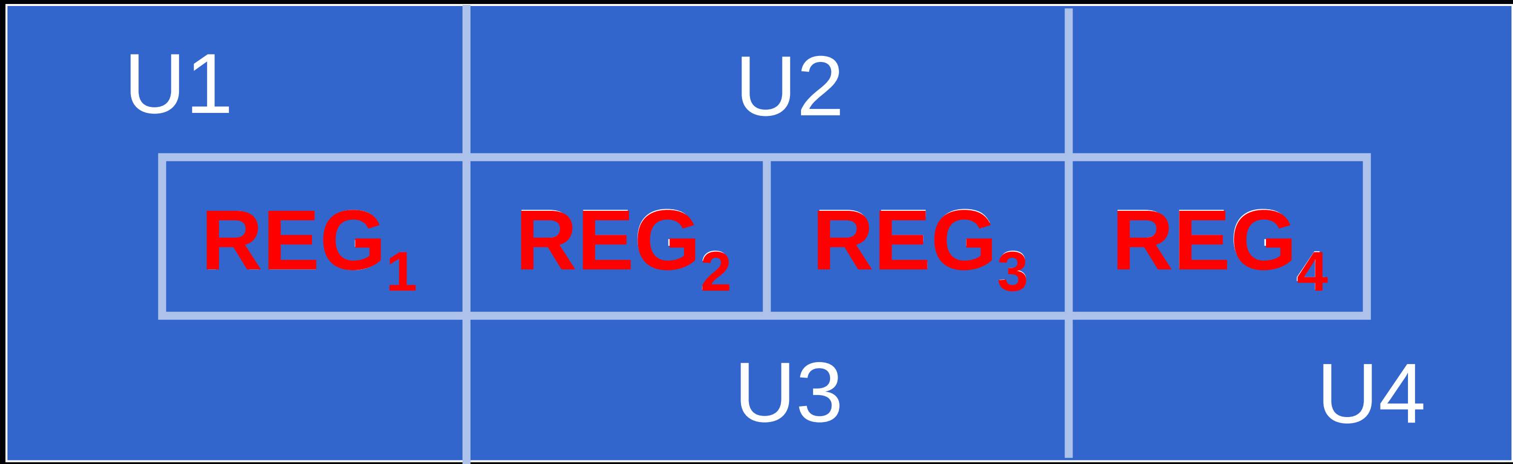
Binding order:

$REG_1 \rightarrow REG_2 \rightarrow REG_3 \rightarrow REG_4$

Hotspot : REG_1 & REG_2

Register Binding – Floorplan-Aware Binding

$U1_{Temp} > U2_{Temp} = U3_{Temp} > U4_{Temp}$



Binding order:

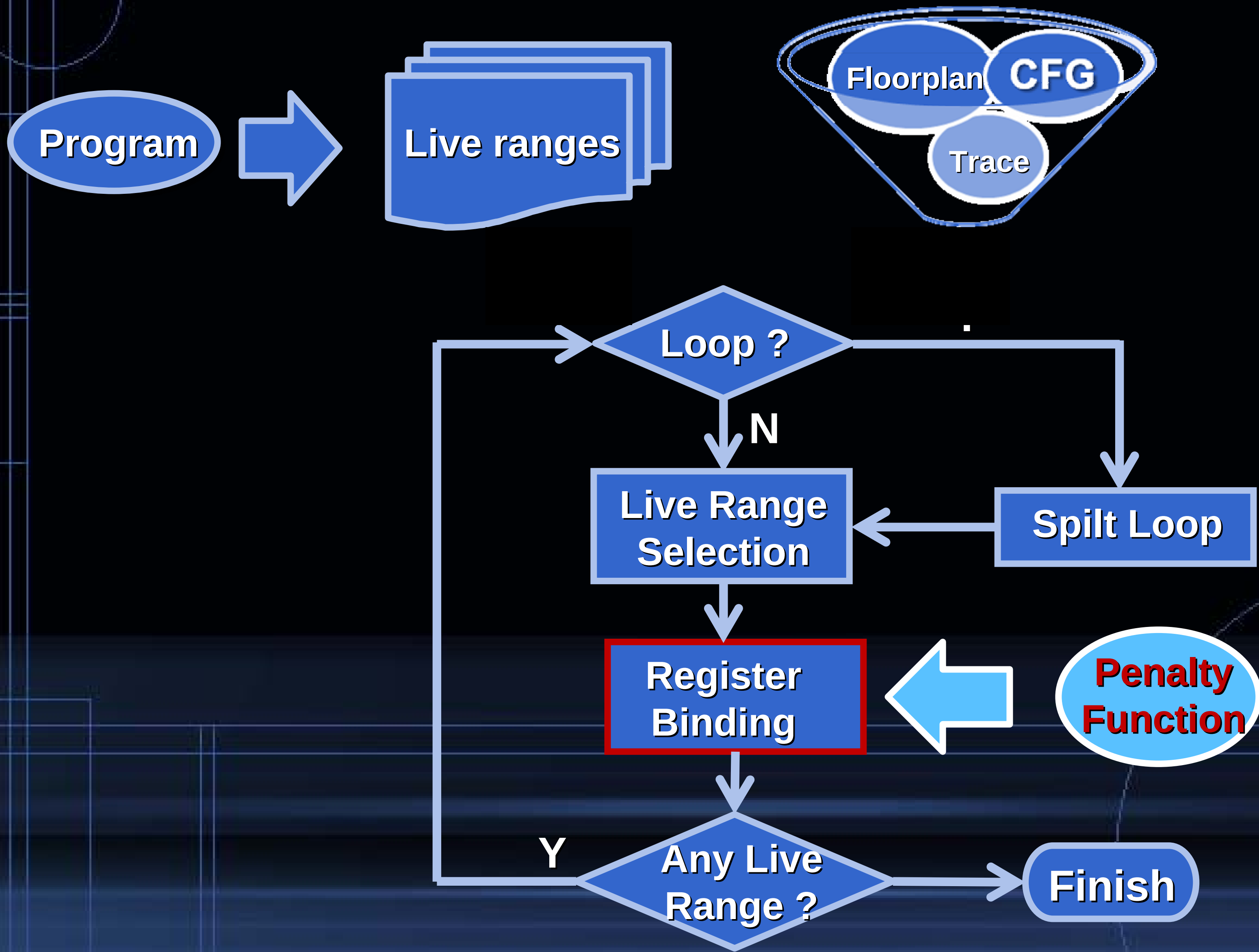
$REG_4 \rightarrow REG_2 \rightarrow REG_3 \rightarrow REG_1$

Temperature Balance !!

Register Binding

- Spatial information
  - Floorplan
    - → location of every unit
- Temporal information
  - Control flow graph (CFG)
    - → program flow
  - Temperature trace file
    - → temperature of every unit

Binding Algorithm Flow



Penalty Function

- Determine whether a sub-bank register file is selected for binding or not.
- Apply *Penalty* to every sub-bank register.
- Bind the target live range to the bank with lowest penalty.

$$Penalty(REG_i) = \alpha \times \underline{proifling\_penalty}(REG_i) + (1-\alpha) \times \underline{history\_penalty}(REGi)$$

$$0 < \alpha < 1$$

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Forwarding Method – Motivation

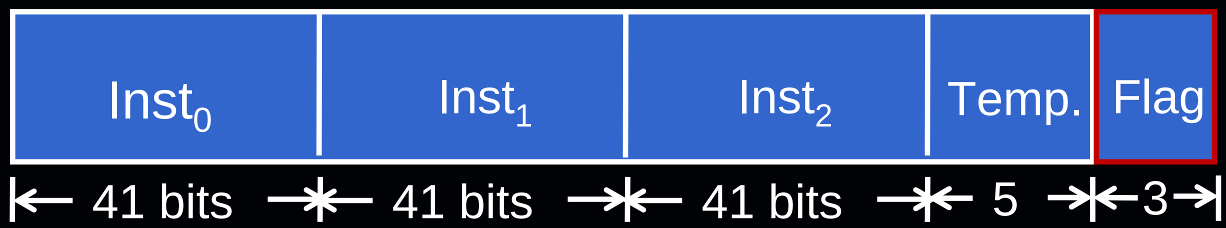
- The forwarding unit exists in a pipeline architecture.
- Useless data is still read from register file when forwarding occurs.

Forwarding Method – Main Idea

- Forwarding condition is detected at compile time and encoded into instructions.
- Sub-bank register file is determined to be turned off or not at run time.

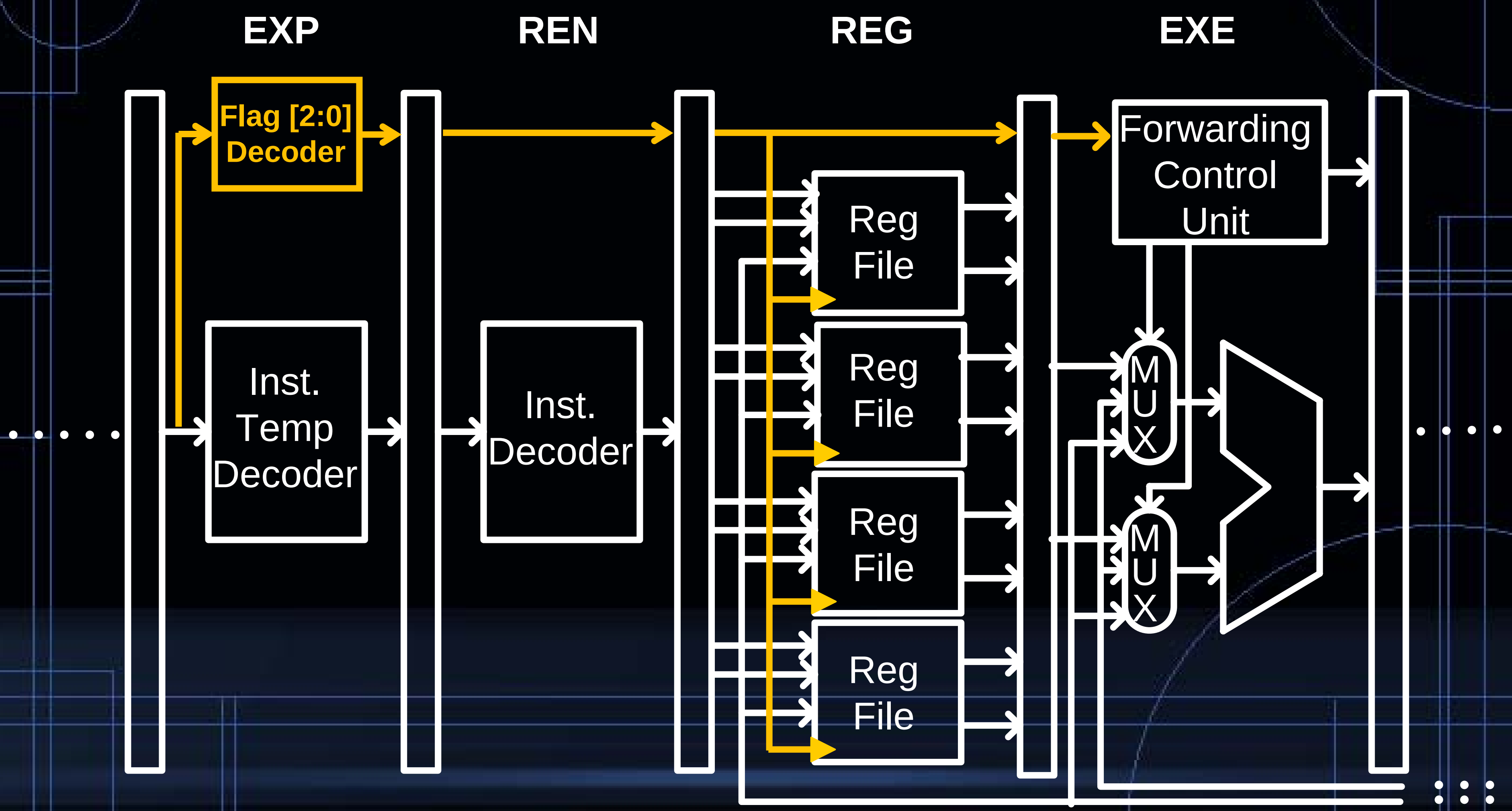
- A *Forwarding-aware Scheduling Algorithm* is proposed to allow more operand-forwarding.

The Modified Bundle Format



Flag encoding	Forwarding condition
000	no forwarding occurs
001	$Inst_0$, 1st source register
010	$Inst_1$, 1st source register
011	$Inst_2$, 1st source register
100	Conflict
101	$Inst_0$, 2nd source register
110	$Inst_1$, 2nd source register
111	$Inst_2$, 2nd source register

The Modified Datapath



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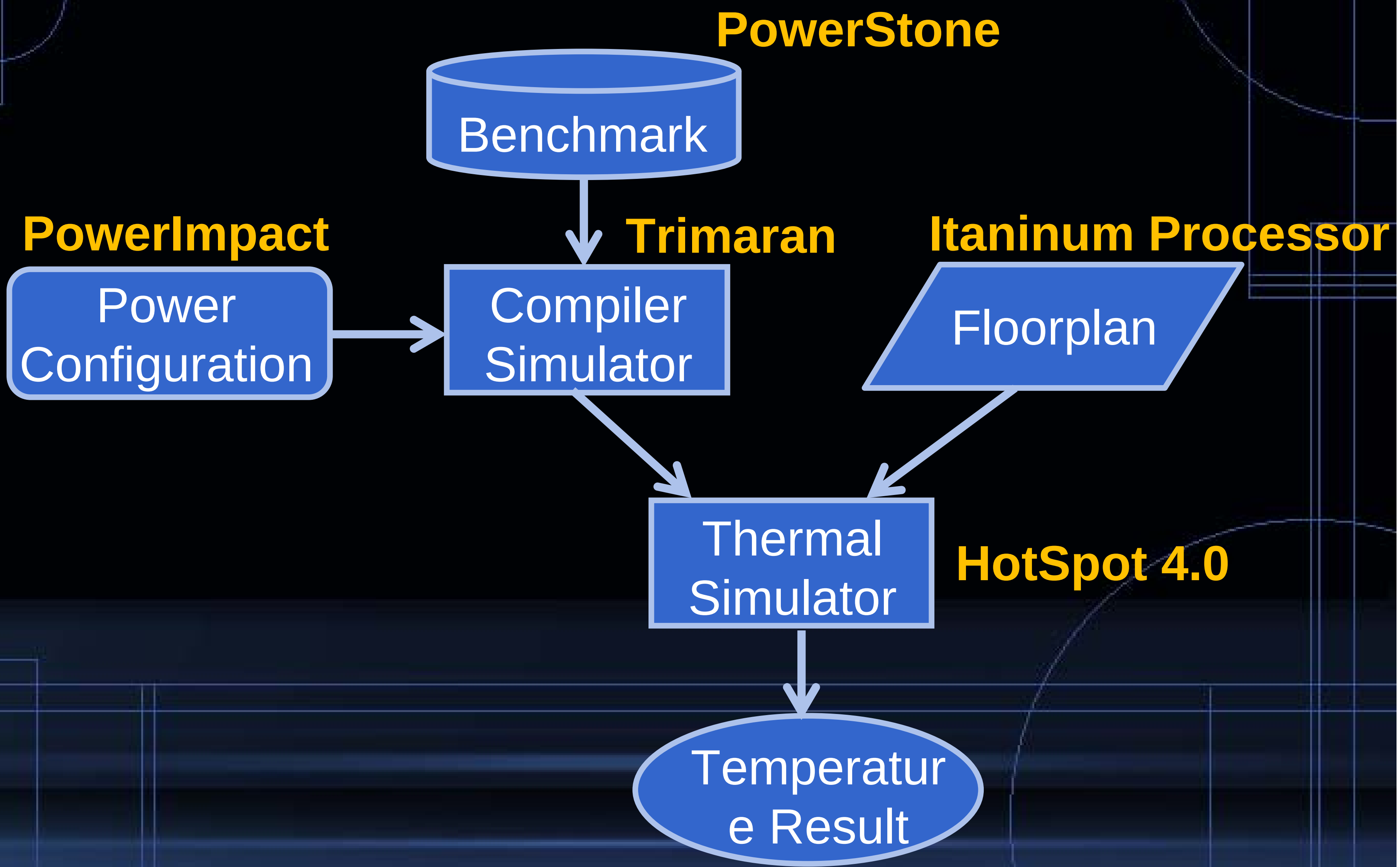
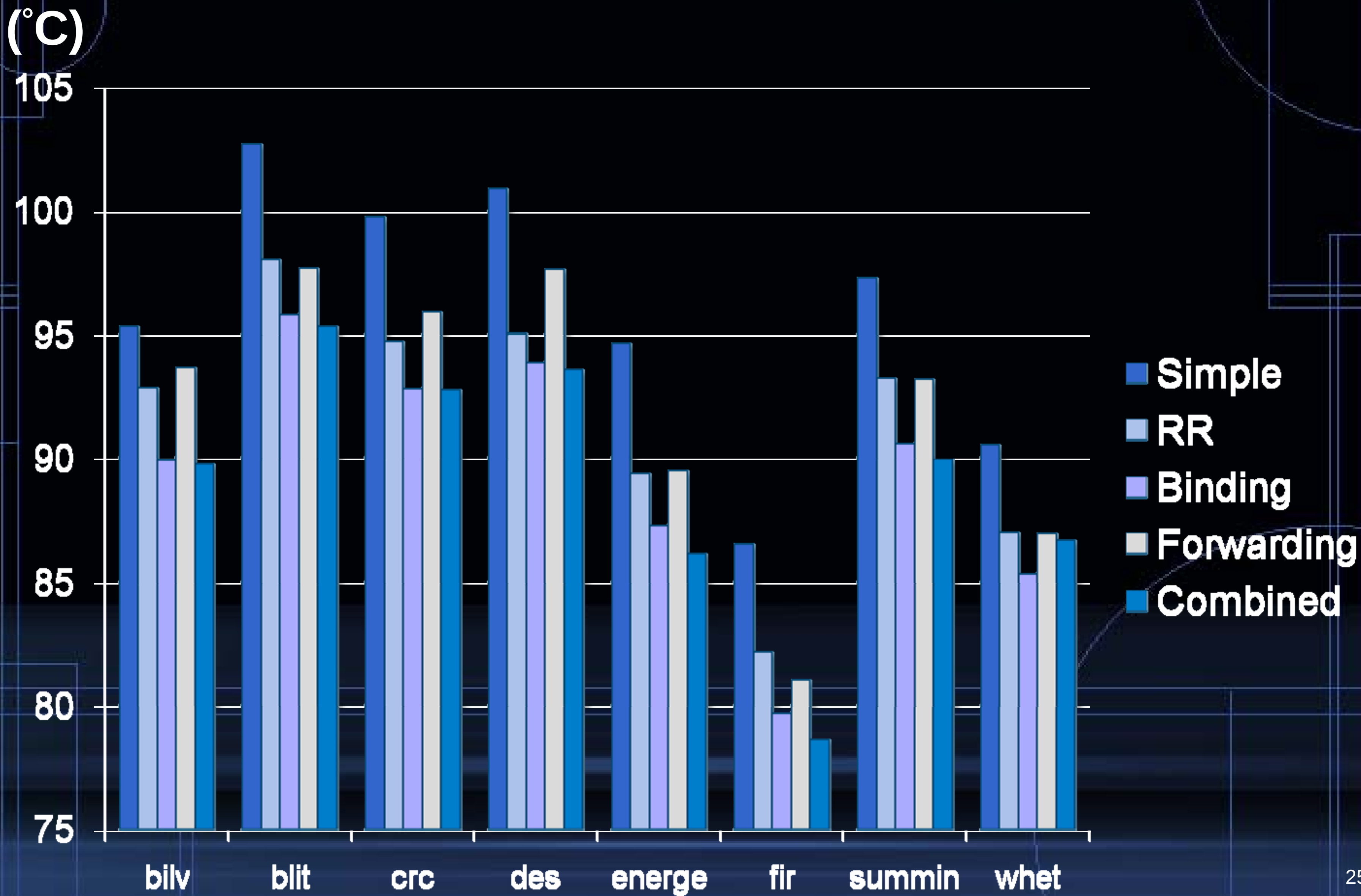
Experiment Flow



Temperature Reduction



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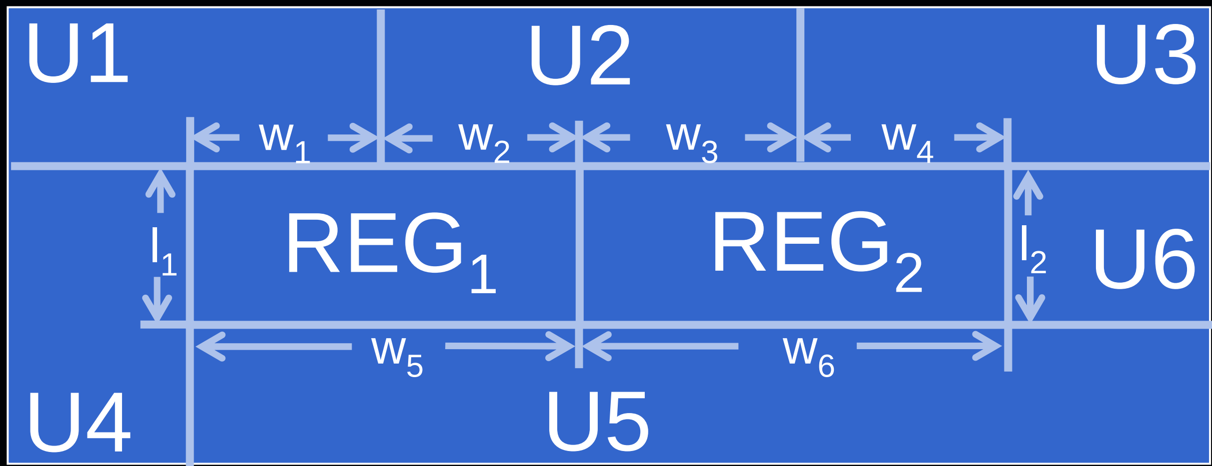
Conclusions

- Binding algorithm and forwarding method are proposed to reduce the hotspot of register file.
- The peak temperature reduction reach 7.89°C in the best case and 7.22°C in average.

THANK YOU !!

Profiling_penalty

- To represent the thermal relationship between register file and its adjacent units.

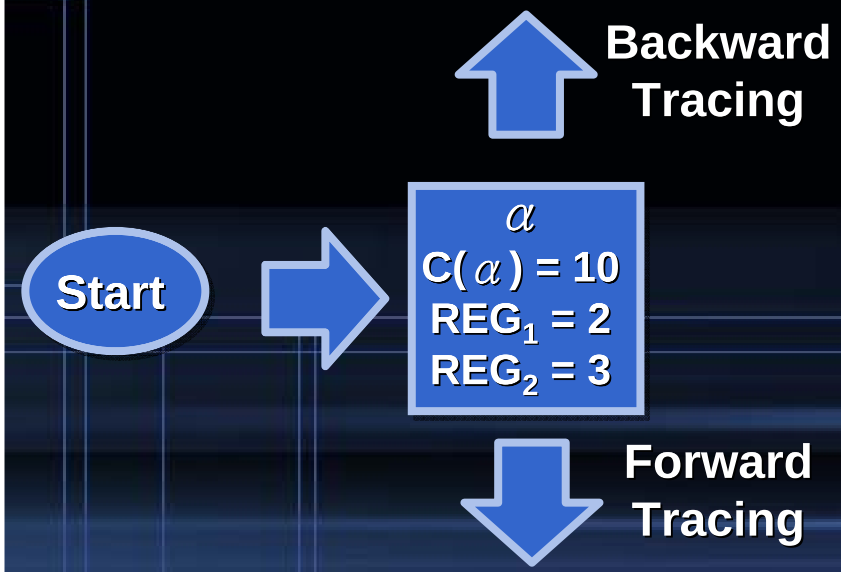


$$\mathit{profiling\_penalty}(REG_1) = \frac{(U1_{Temp} \times w_1) + (U2_{Temp} \times w_2) + (U4_{Temp} \times l_1) + (U5_{Temp} \times w_5)}{4}$$

BACK

History_penalty

- To represent the thermal relationship within sub-bank register files.
- The CFG (Control Flow Graph) is used to accumulate the access counts of register file.



Basic block α

C(α) = 10

→ α executes 10 cycles

$REG_1 = 2$

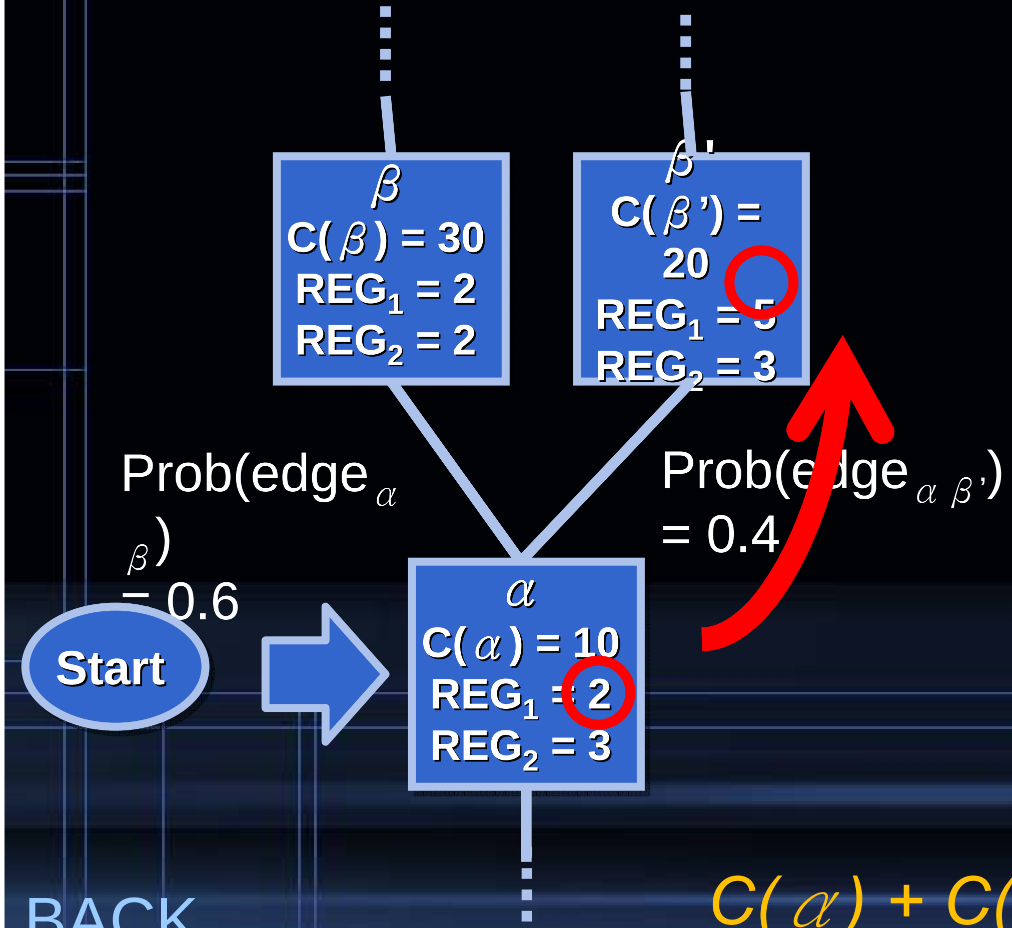
→ access counts of REG_1

$REG_2 = 3$

→ access counts of REG_2

History_penalty

- To represent the thermal relationship within sub-bank register files.



priority(β)

$= Prob(edge_{\alpha\beta}) \times (1 + REG_1)$

$= 0.6 \times (1+2) = 1.8$

priority(β')

$= Prob(edge_{\alpha\beta'}) \times (1 + REG_1)$

$= 0.4 \times (1+5) = 2.4$

$Count(REG_1) = 2 + 5 = 7$

C(α) + C(β') > threshold cycle?

BACK

Performance Penalty

Bench-mark	Orig. Cycle count	Binding Pen (%)	Forwarding Pen (%)	Combined Pen (%)
bilv	376064357	0.0	1.3	0.9
blit	50440416	0.0	1.7	1
crc	5660433	0.0	0.7	0.5
des	41964763	0.0	1.5	0.8
energe	711784	0.0	1.2	1.2
fir	45077873	0.0	1.6	1.1
summin	492696	0.0	0.8	0.8
whet	77202731	0.0	1.5	0.9
average		0.0	1.3	0.9