Defect-Aware Thresholder in the Sense Amplifier of Nanowire Crossbar Memories

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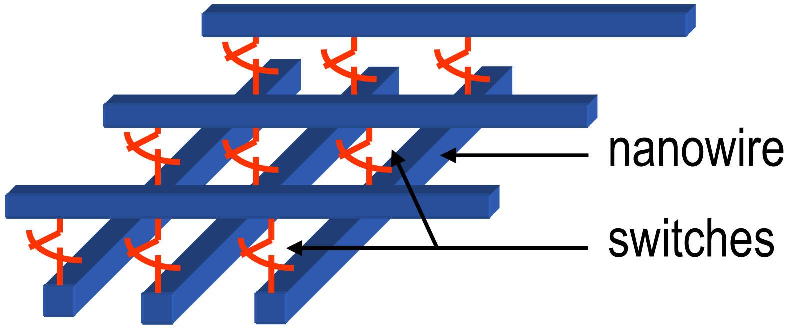
Motivation

- Silicon nanowire crossbar circuits are a promising post-CMOS candidate:
  - Higher density
  - Regular organization
  - Multiple functions



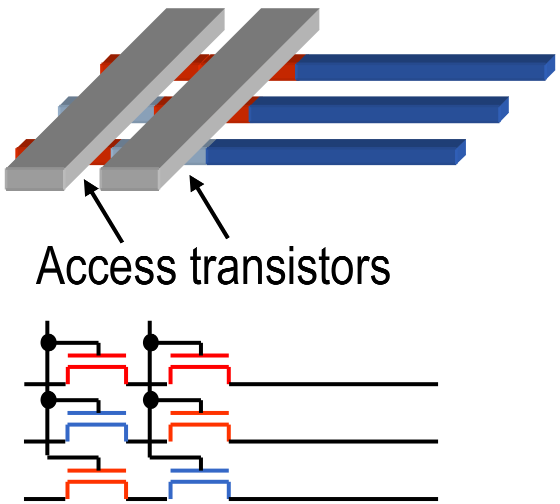
- Interfacing the nanowire crossbars and the rest of the CMOS chip is still challenging:
  - Bridging the scales is not reliable
- Crossbar circuits need special test procedures
  - Decoder test is required

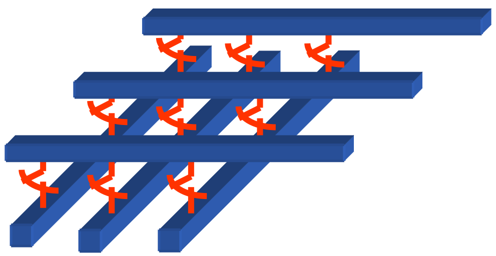
Outline

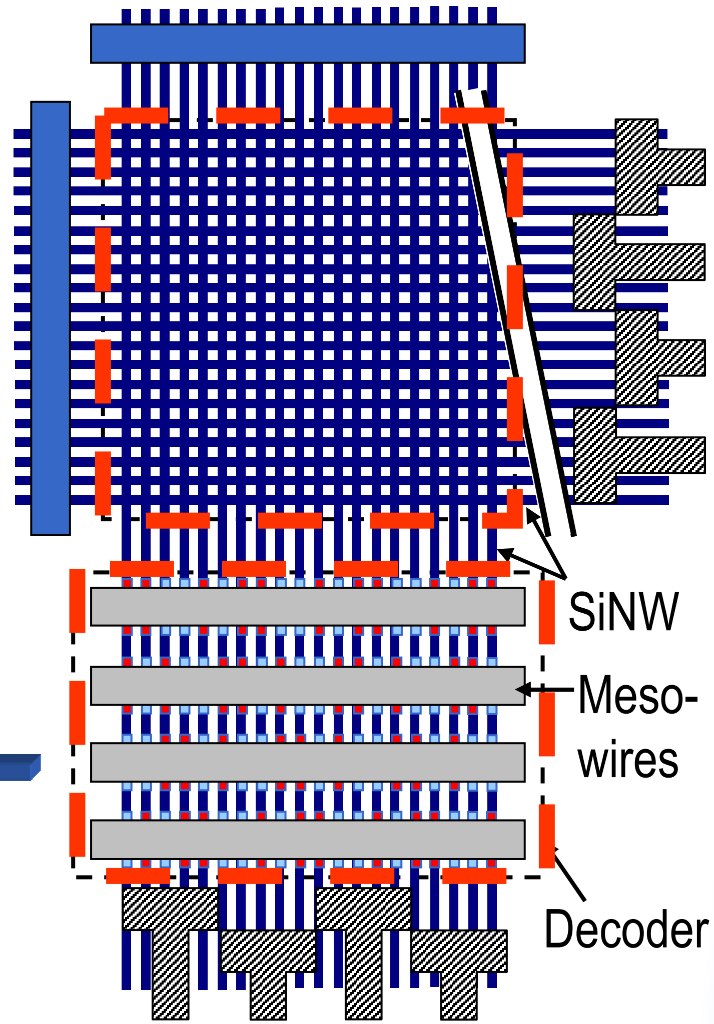
- Introduction
- Decoder Test
- Current Variability Model
- Simultation Results
- Conclusions

Organization of Nanowire Crossbars

- Two parts of the crossbar circuit [DeHon'03]:
  - Crosspoints: functional region
  - Decoder: interfacing CMOS⇔SiNW





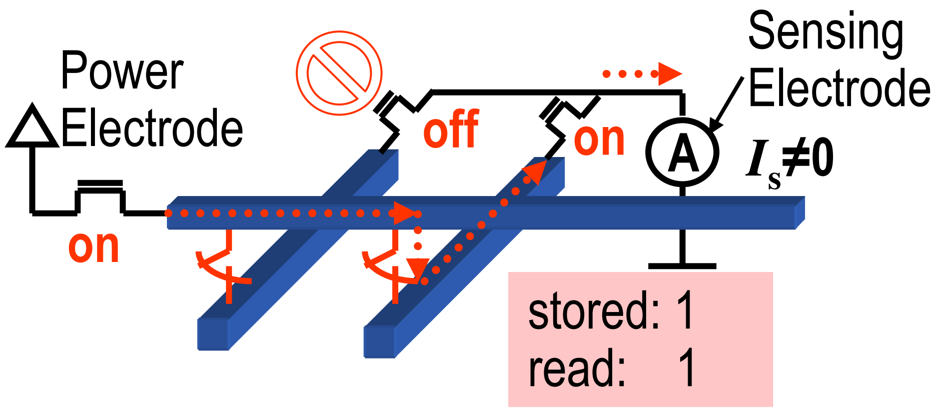


Nanowire Decoders

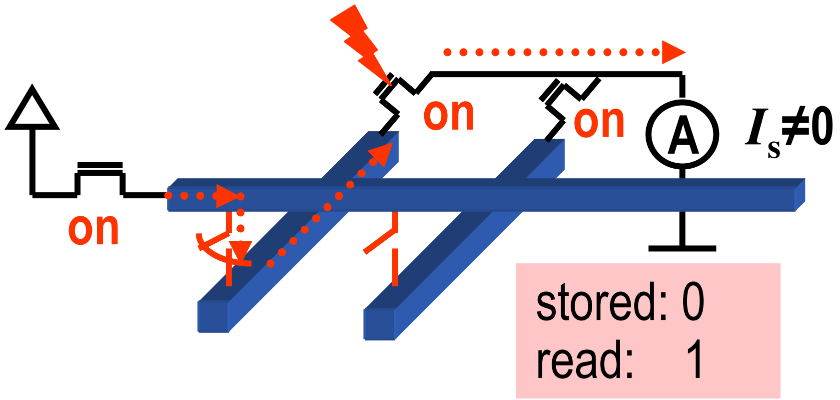
- Task of the decoder: unique addressing of every nanowire by the outer CMOS circuit.
- Matching the sub-lithographic to lithographic pitch is technologically expensive.
- Cost-efficient and CMOS-compatible decoders generally provide a stochastic addressing.
  - Unpredicted number of nanowires with a given address: axial [DeHon'03], radial [Savage'06], random contact decoder [Hogg'06]
  - Unpredictable threshold voltage (V_T) of access transistors: axial, mask-based [Beckman'05], gate-all-around decoders [Ben Jamaa'07]

Decoder Variability

- Current-based memory operations [Cerofolini'07]



- Variability of V_T ➔ errors in READ/WRITE:



Testing Nanowire Decoders

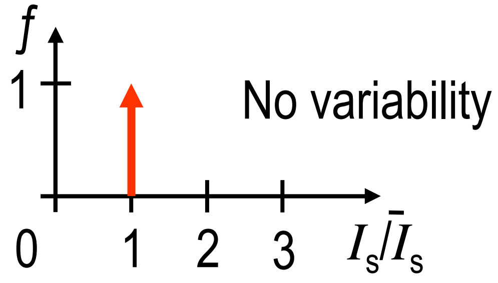
- Variability of V_T ➔ pattern sensitivity faults
  - Expensive functional testing [Abadir'83, Adams'03].
  - Efficient algorithms for crossbar memories?

- Reducing memory test complexity by first testing decoder

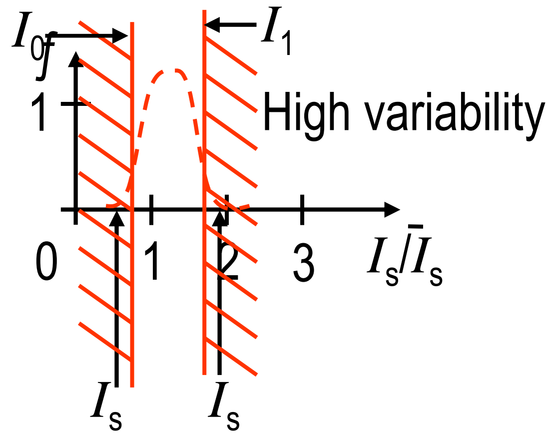
- Challenges:
  - How can we test nanowire array decoders?
  - What are the thresholder design constraints?
  - How do design and test mutually influence on each other?

Variability-Induced Decoder Errors

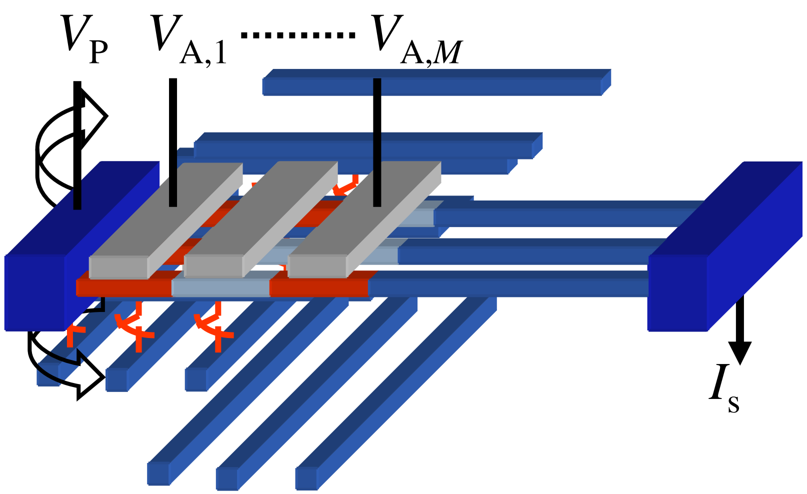
- In the absence of variability, sensed current I_s fixed value $\bar{I}_s$



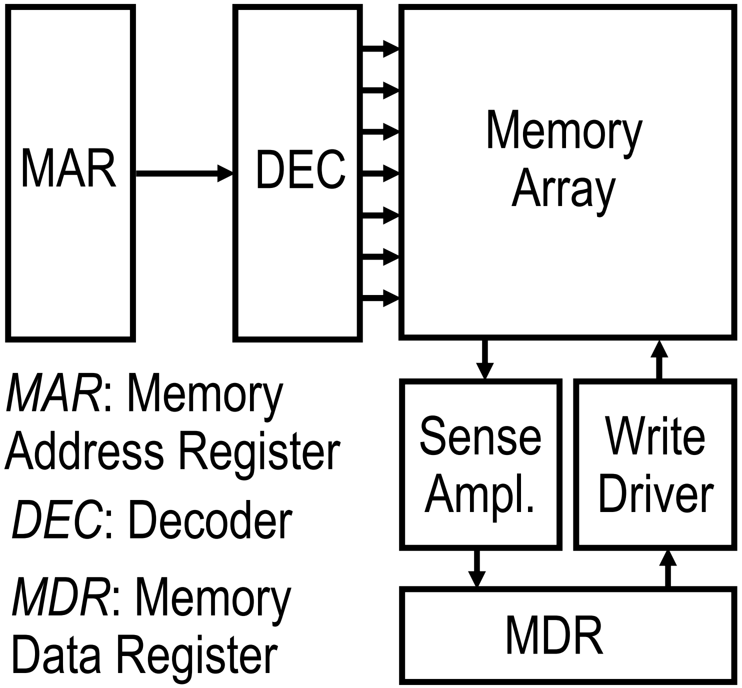
- With high variability, I_s follows a stochastic distribution f:
  - Single NW addressed, but current lower than noise level
  - Single NW addressed, but current higher than level of 2 NWs



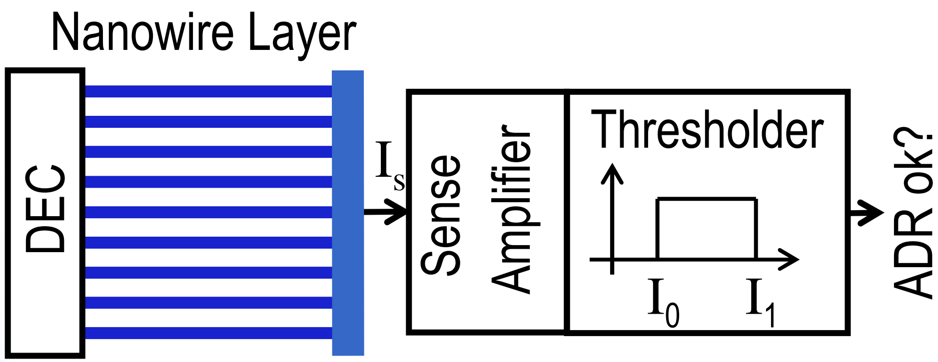
Bootstrap Decoder Test



- Advantages:
  - Linear complexity
  - No additional physical resources



MAR: Memory Address Register
DEC: Decoder
MDR: Memory Data Register



Test Quality

- Thresholder must identify absence of addressed NWs:
  - Maximize $Pr_1 = Pr\{I_s < I_0$, given that: I_s delivered by = 0 NW$\}$

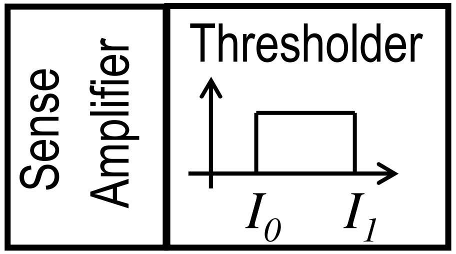
- Thresholder must identify uniquely addressed NWs:
  - Maximize $Pr_2 = Pr\{I_0 \leq I_s \leq I_1$, given that: I_s delivered by = 1 NW$\}$

- Thresholder must identify unintentionally addressed NWs:
  - Maximize $Pr_3 = Pr\{I_1 < I_s$, given that: I_s delivered by ≥ 2 NW$\}$

- The best test maximizes all 3 events ➔ test quality improves by minimizing test error defined as:

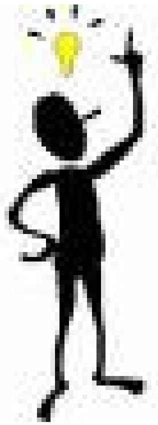
$$\varepsilon = 1 - Pr_1 \times Pr_2 \times Pr_3$$

Test-Aware Thresholder Design



How should I design the thresholder?

What are the best values for I_0 and I_1?



Define distribution of variable parameters $\mathbf{P}$

Calculate dependency of I_s on $\mathbf{P}$

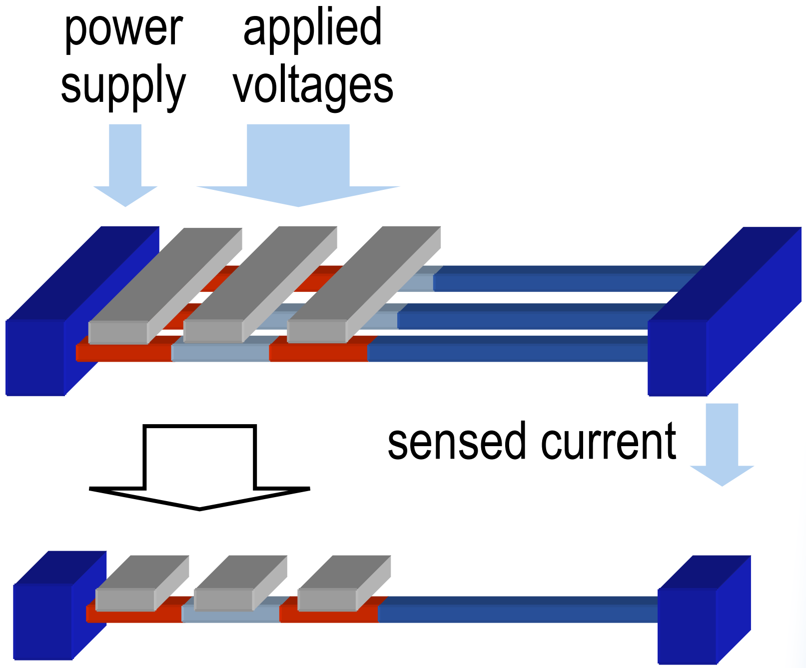
Calculate stochastic distribution of I_s

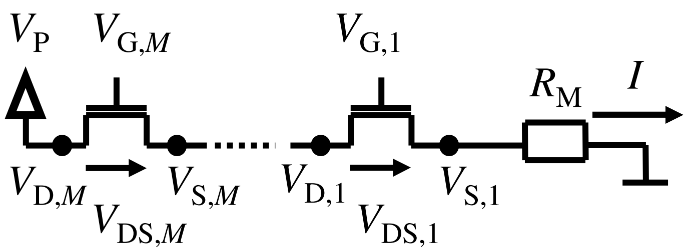
Derive ε as a function of I_s, *i.e.*, $\mathbf{P}$

$$\{I_0, I_1\} = \arg\min \varepsilon(\mathbf{P})$$

Variability of Circuit Under Test

- Circuit under test:
  - Full NW layer
  - Defect-free case: 1 NW
  - Circuit reduced to a series of M transistors and a resistor R_M
- Model parameters:
  - Gaussian parameters: $V_{T,i} \sim N(V_T^{OP}, \sigma_T^2)$
  - Model-fixed parameter: R_M
  - Extrinsic parameter: V_P
- Variability model:
  - Sensitivity analysis: $I = I^{OP} + \delta I$
  - Linearization: $\delta I = \mathbf{g}^T \cdot \delta V_T$
  - Small signal conductance vector $\mathbf{g}$





Current Components

- Array of N nanowires

- Current through the NW array:
  - I_u: Useful signal – caused by a single addressed NW
  - I_{in}: Intrinsic noise – caused by N_{in} non-addressed NWs
  - I_{dn}: Defect-induced noise – caused by N_{dn} badly addressed NWs

Distribution of Current Components

- Useful signal:
  - I_{on}: on-current

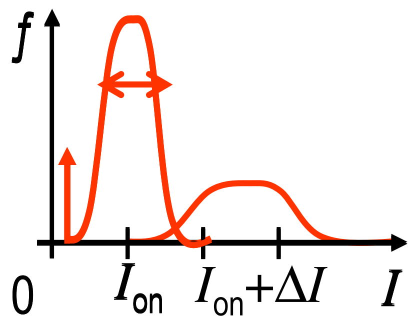
$$I_u \propto N(I_{on}, \|\mathbf{g}\|^2 \sigma_T^2)$$

- Intrinsic noise:
  - I_{off}: off-current

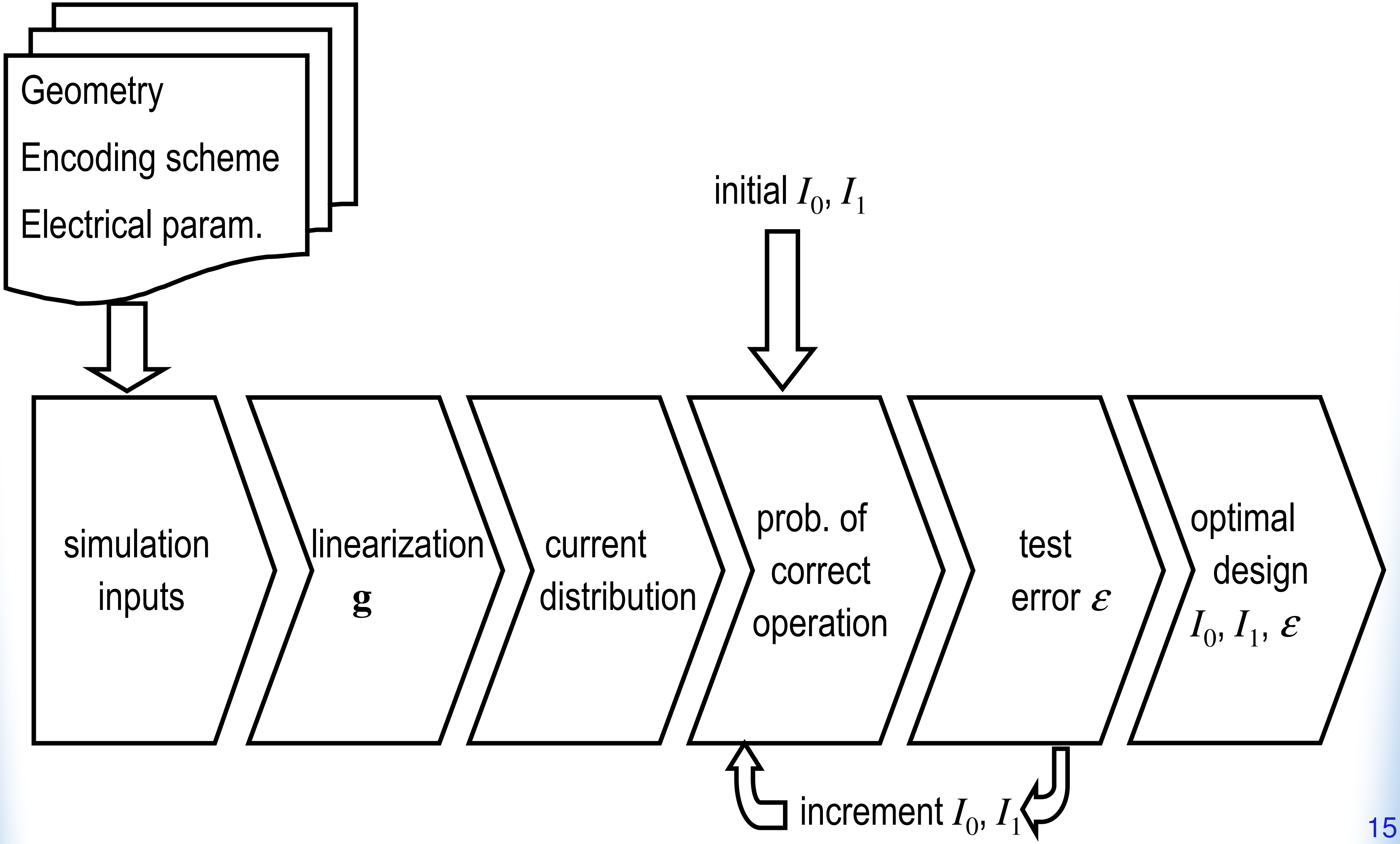
$$I_{in} = N_{in} \times I_{off}$$

- Defect-induced noise:
  - Defects in NW i described by $\mathbf{s}_i$
  - N_{di} defective NWs shift mean value, and increase std-deviation

$$I_{di,N_{di}} \propto N(I_{on} + \Delta V_T \cdot \mathbf{g}^T \cdot \sum_{i=1}^{N_{di}} \mathbf{s}_i, N_{di} \|\mathbf{g}\|^2 \sigma_T^2)$$



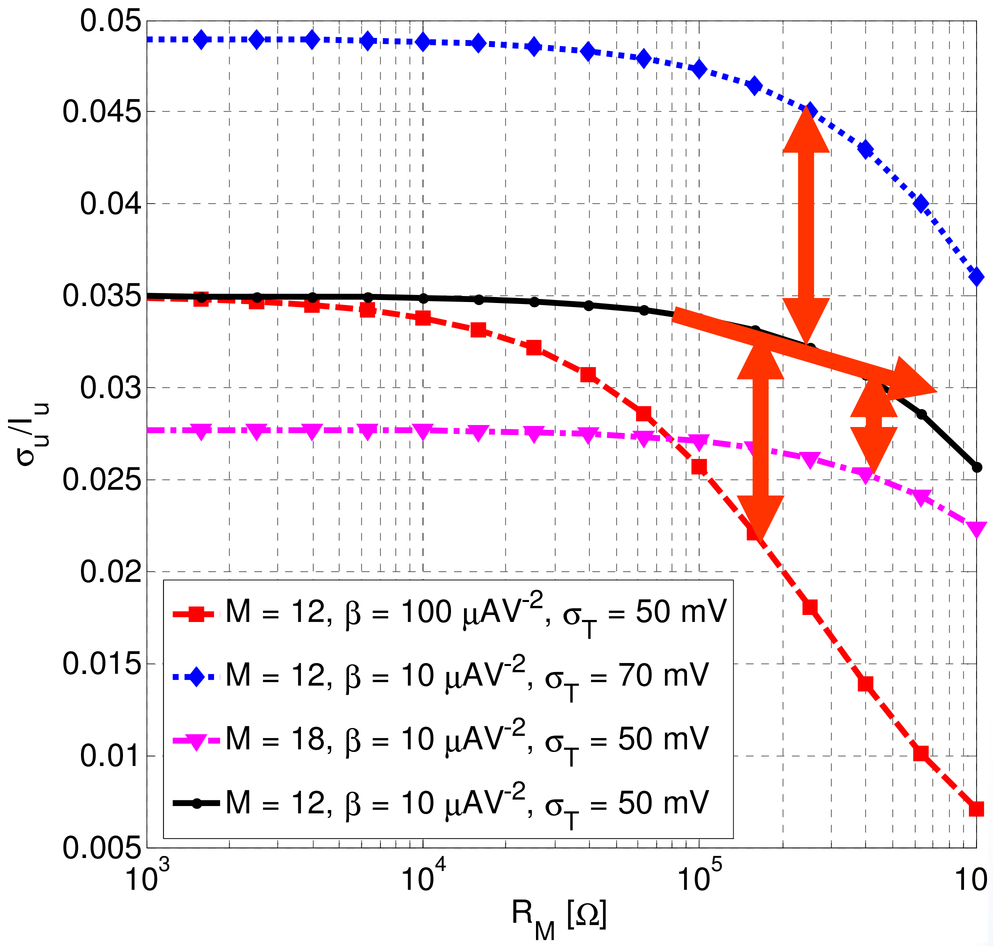
Simulation Flow



General Signal Variation

- Distribution of I_u and I_{di} with similar qualitative behaviours

- I_u distribution improves with:
  - $R_M \uparrow$: σ_u decreases faster than $\bar{I}_u$
  - $\beta \uparrow$: higher current injection
  - $\sigma_T \downarrow$: σ_u scales linearly with σ_T
  - $M \uparrow$: $\sigma_u \sim 1/\sqrt{M} \downarrow$ faster than $\bar{I}_u$



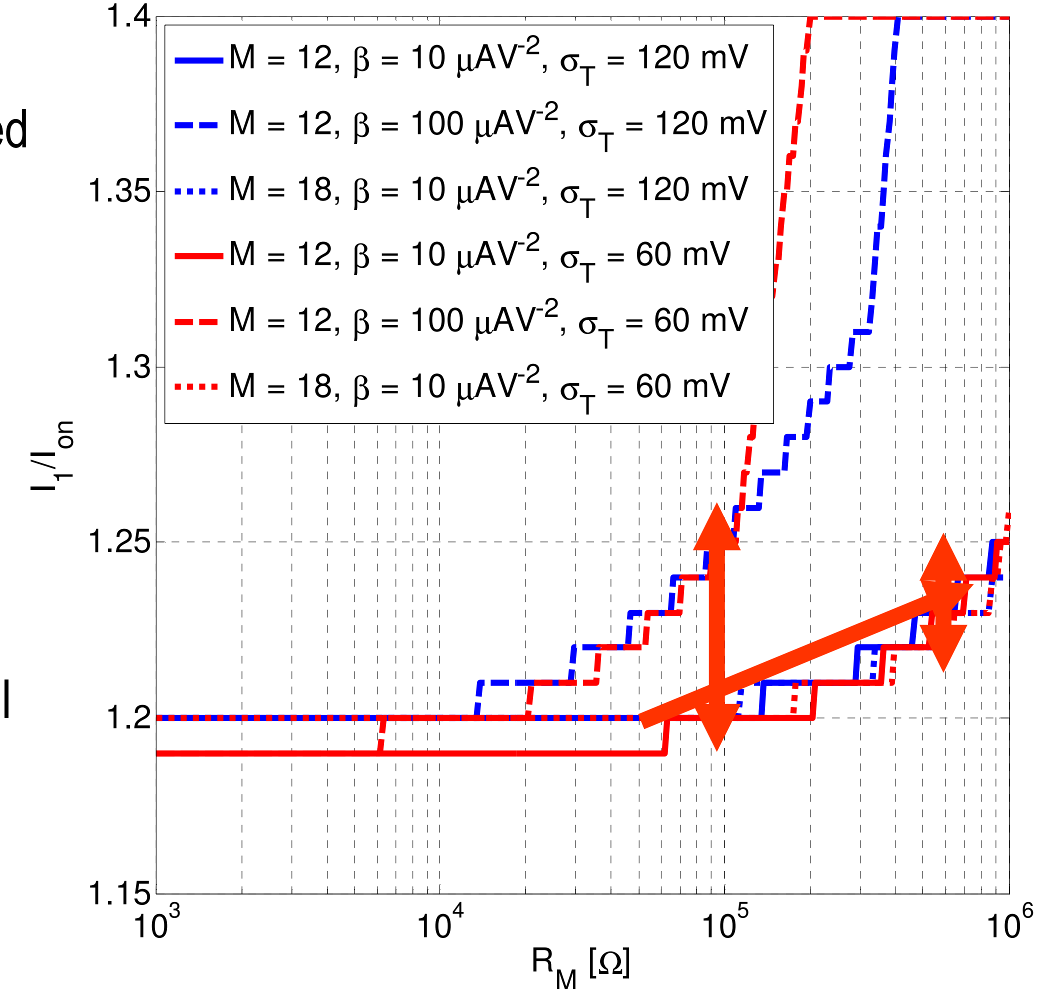
Thresholder Parameters

- Influence of parameters:
  - β: weak 10× ➔ 4%
  - R_M: stronger only if combined with β ➔ unlikely
  - M: weaker

$$I_1 \approx 1.2 \times I_{on}$$

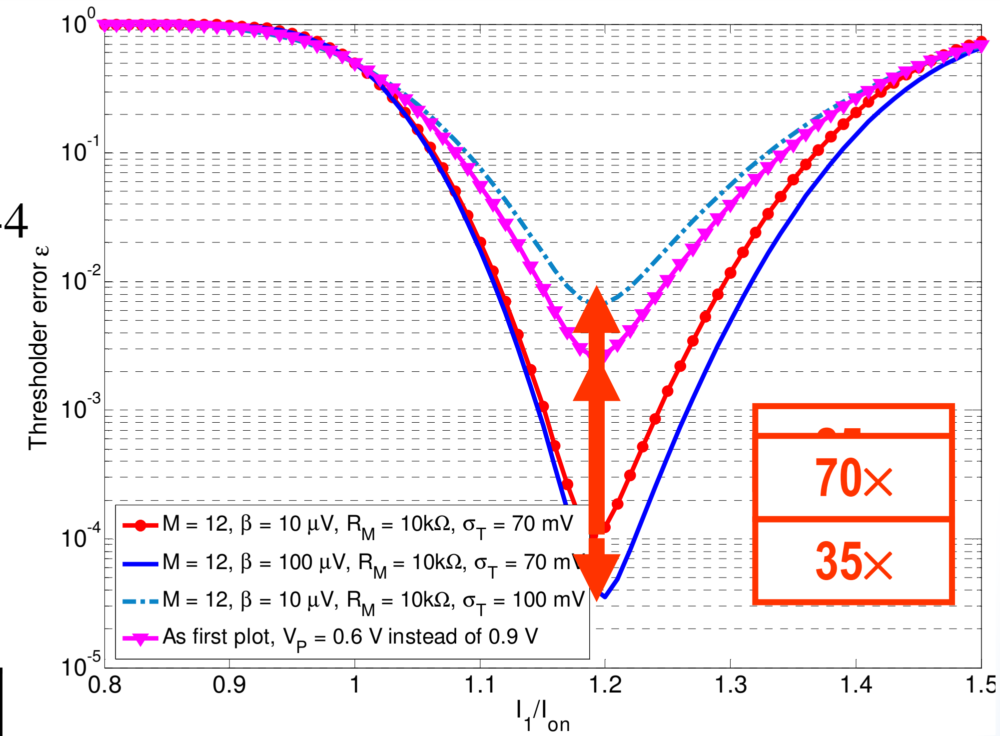
- Fixing range of I_0:
  - Not too small to filter noise
  - Not too large to detect useful signal

$$I_0 \approx 0.7 \times I_{on}$$



Test Error

- Typical parameters:: $\varepsilon \sim 10^{-4}$
- Impact of parameters on ε:



Parameter	I^{OP}	δI	Impact
$V_P \downarrow$	↓	–	☹
$\sigma_T \uparrow$	–	↑	☹
$\beta \uparrow$	↑	–	☺
$M \uparrow$	↓	↓↓	☺

	M	14	16	18
	Area	12%	24%	36%
ε	σ_T=80mV	4x	15x	59x
	σ_T=100mV	3x	7x	15x

Conclusions

- Decoder test necessary to reduce crossbar memory test complexity caused by decoder variability
- Stochastic and perturbative current model used to quantify test error
- Robust thresholder against technology and parameter variation
- Typical test error ~10^{-4}, better test with higher supply voltage, stronger access devices and redundant decoder design

Thank you...