Call for Papers
ASP-DAC 2009

Asia and South Pacific Design Automation Conference 2009

http://www.aspdac.com/aspdac2009/

January 19~22, 2009

Yokohama, Japan

Aims of the Conference:

ASP-DAC 2009 is the fourteenth annual international conference on VLSI design automation in Asia and South Pacific region, one of the most active regions of design and fabrication of silicon chips in the world. The conference aims at providing the Asian and South Pacific CAD/DA and Design community with opportunities of presenting recent advances and with forums for future directions in technologies related to Electronic Design Automation (EDA). The format of the meeting intends to cultivate and promote an instructive and productive interchange of ideas among EDA researchers/developers and system/circuit/device designers. All scientists, engineers, and students who are interested in theoretical and practical aspects of VLSI design and design automation are welcome to ASP-DAC.

Areas of Interest:

Original papers on, but not limited to, the following areas are invited.

Strict Paper Submission Deadline:
July 14, 2008, 6:00 AM TST (GMT +08:00)

[1] System-Level Design Methodology:
System modeling, specification, language, design methodology, performance analysis, hardware-software co-design/co-simulation/co-verification, HW-SW interface synthesis, IP/platform-based design, etc.

[2] System Architecture and Optimization:
System-on-Chip and multi-processor SoC (MPSoC) architecture design, low power system design, network on chip, system communication architecture, memory architecture, application-specific instruction-set processor (ASIP) synthesis, virtual platforms, etc.

[3] Embedded and Real-Time Systems:
Embedded system design, real-time system design, OS, middleware, compilation techniques, memory/cache optimization, interfacing and software issues

[4] High-Level/Behavioral/Logic Synthesis and Optimization:
High-Level/behavioral/RTL synthesis, technology-independent optimization, technology mapping, interaction between logic design and layout, sequential and asynchronous logic synthesis, resource scheduling, allocation, and synthesis

[5] Validation and Verification for Behavioral/Logic Design:
Logic simulation, symbolic simulation, formal verification, equivalence checking, transaction-level/RTL and gate-level modeling and validation, assertion-based verification, coverage-analysis, constrained-random testbench generation

[6] Physical Design (Routing):
Routing, repeater issues, interconnect optimization, interconnect planning, module generation, layout verification, post-placement layout and optimization, clock network design.

[7] Physical Design (Placement):
Placement, floorplanning, partitioning, hierarchical design, interaction between physical design and logic synthesis.

[8] Timing, Power, Thermal Analysis and Optimization:
Deterministic and statistical static timing analysis, statistical performance analysis and optimization, low power design, power and leakage analysis, power/ground and package analysis and optimization, thermal analysis, etc.

[9] Signal/power Integrity, Interconnect/Device/Circuit Modeling and Simulation:
Signal/power integrity, clock and bus analysis, interconnect and substrate modeling/extraction, package modeling, device modeling/simulation, circuit simulation, high-frequency and electromagnetic simulation of circuits, etc.

[10] Design for Manufacturability/Yield and Statistical Design:
DFM, DFY, CAD support for OPC and RET, variability analysis, yield analysis and optimization, reliability analysis, design for resilience and robustness, cell library design, design fabrics, etc..

[11] Test and Design for Testability:
Testable design, fault modeling, ATPG, BIST and DFT, memory test and repair, core and system test, delay test, analog and mixed signal test.

[12] Analog, RF and Mixed Signal Design and CAD:
Analog/RF synthesis, analog layout, verification and simulation techniques, noise analysis, mixed-signal design considerations

[13] Emerging technologies and applications

(i) System-level design case studies for emerging applications: multimedia, consumer electronics, communication, networking, ubiquitous computing, biomedical applications, etc.

(ii) Post CMOS technologies: nanotechnology, quantum, optical interconnect, 3D integration, probabilistic architecture, microfluidics, molecular, bioelectronics, etc., with emphasis on modeling, analysis, novel circuit/architecture, CAD tools, and design methodologies.

ASP-DAC 2009 University VLSI Design Contest encourages submitting original papers on VLSI design and implementation at universities and other educational organizations.

Submission of Papers:

Deadline for submission:	**6 am TST,**	**July**	**14 (Mon),**	**2008**
Notification of acceptance:		**September**	**26 (Fri),**	**2008**
Deadline for final version:	**6 am TST,**	**November**	**17 (Mon),**	**2008**

Specification of the paper submission format will be available at the WEB site:
`http://www.aspdac.com/aspdac2009/`

Panels, Special Sessions and Tutorials:

Suggestions and proposals are welcome and have to be addressed to the Conference Secretariat (e-mail: aspdac2009@aspdac.com) no later than June 9 (Mon), 2008.

Prospective Sponsors:

ACM SIGDA, IEEE CAS, IEICE ESS, IPSJ SIG-SLDM

ASP-DAC2009 Chairs:

General Chair: Kazutoshi Wakabayashi (NEC)
Technical Program Chair: Ren-Song Tsay (National Tsing Hua Univ.)
Technical Program Vice Chair: Shinji Kimura, (Waseda Univ.)

Conference Secretariat:

Please contact Conference Secretariat (e-mail: aspdac2009@aspdac.com), if you have questions or comments.