Program of the 6th IEEE International Workshop on Compact Modeling

date: Monday, January 19
place: Pasifico Yokohama

			Title	Authors	Affiliation
8:30-8:35			Opening Remarks		
		Session 1	**Plenary Session**		
8:35-9:15	1		Low-Power 60GHz CMOS Pulse Communication	M. Fujishima	University of Tokyo
9:15-9:55	2		Variation and Manufacturability Aware Design Methodology for the Advanced System LSI	N. Nishiguchi	STARC, Japan
9:55-10:35	3		Fully Depleted SOI Technology for Ultra Low Power Application and Needs for Next SOI Circuit Model	J. Ida	OKI Semiconductor
10:35-10:45		break			
		Session 2	**SOI and Multi-Gate MOSFET**		
10:45-11:10	4		HiSIM-SOI: A Dynamic Depletion Model Valid for Device/ Circuit Optimization	S. Kusu et al.	Hiroshima University
11:10-11:35	5		Quantum Mechanical Compact Modeling of Inversion Charge in Double-Gate MOSFETs Unifying Symmetric and Asymmetric Operation Modes	Z. Yuan et al.	Tsinghua University
11:35-12:00	6		Multiple-Gate MOSFETs: Structures, Operation Modes, and Generic Compact Model Development	X. Zhou et al.	Peking University
12:00-13:00		lunch break			
		Session 3	**Bulk-MOSFET**		
13:00-13:25	7		An Explicit Surface Potential Model of the Bulk-MOS with Inclusion of Poly-Gate Accumulation, Depletion, and Inversion	Y. Song et al.	Peking University
13:25-13:50	8		A Surface Potential Model for Bulk MOSFET which Accurately Reflects Channel Doping Profile Expelling Fitting Parameters	H. Sakamoto et al.	Selete, Japan
13:50-14:00		break			
		Session 4	**Parameter Extraction and Quality Assurance**		
14:00-14:25	9		A Practical Statistical Modeling Approach for CMOS Transistors	P. B. Y. Tan et al.	Silterra Malaysia
14:25-14:50	10		Proposal of Automated Rule-Based Spice Parameter QA Methodology	H. Koike et al.	STARC, Japan
14:50-15:15	11		MOSFET Model Extraction from BSIM3v3 to BSIM4 and PSP	P. B. Y. Tan et al.	Silterra Malaysia
15:15-15:40	12		Parameter Extraction Examples for HiSIM2 and HiSIM_HV	Y. Iino	Silvaco Japan
15:40-15:50		break			
		Session 5	**High-Voltage MOSFET, Nanowire and Photodiode**		
15:50-16:15	13		Modeling of Silicon Nanowire Schottky Barrier MOSFET	Y. Che et al.	Peking University
16:15-16:40	14		LDMOS Transistor Macro-modeling to Accurately Predict Bias Dependence of Gate-overlap Capacitance	T. Saito et al.	Renesas Technology
16:40-17:05	15		Electro-thermal Simulation for Automotive Power Application using Novel LDMOS Model	T. Kojima et al.	Toyota, Central R&D
17:05-17:30	16		Analysis and Modeling of p-i-n Photodiode Noise	T. Miyoshi et al.	Hiroshima University