ASP-DAC 2009

Contents

Highlights

Opening and Keynote I

Tuesday, January 20, 8:30-10:00, Small Auditorium, 5F

"Challenges to EDA System from the View Point of Processor Design and Technology Drivers"
Mitsuo Saito - Chief Fellow and VP of Engineering, Toshiba Corporation Semiconductor Company, Japan

Keynote II

Wednesday, January 21, 9:00-10:00, Small Auditorium, 5F

"Automated Synthesis and Verification of Embedded Systems: Wishful Thinking or Reality?"
Wolfgang Rosenstiel - Professor, Chair for Computer Engineering and Director, Wilhelm-Schickard-Institute for Informatics, University of Tuebingen, Germany

Keynote III

Thursday, January 22, 9:00-10:00, Small Auditorium, 5F

"From Restrictive to Prescriptive Design"
Leon Stok - Director, Electronic Design Automation, IBM Systems and Technology Group, United States

Special Sessions

1D: Tuesday, January 20, 10:15-12:20, Room 416+417
Presentation + Poster Discussion: "University LSI Design Contest" **(See page 23 for more details.)**

2D: Tuesday, January 20, 13:30-15:35, Room 416+417
Invited Talks: "EDA Acceleration Using New Architectures"

2D-1: Aspects of GPU for General Purpose High Performance Computing
Reiji Suda (Univ. of Tokyo/JST CREST, Japan), Takayuki Aoki (Tokyo Inst. of Tech./JST, CREST, Japan) Shoichi Hirasawa (Univ. of Electro-Comm./JST CREST, Japan) Akira Nukada (Tokyo Inst. of Tech./JST CREST, Japan) Hiroki Honda (Univ. of Electro-Comm./JST CREST, Japan) Satoshi Matsuoka (Tokyo Inst. of Tech./JST CREST/NII, Japan)

2D-2: Designing and Optimizing Compute Kernels on Nvidia GPUs
Damir A. Jamsek (IBM Research, United States)

2D-3: Parallelizing Fundamental Algorithms such as Sorting on Multi-core Processors for EDA Acceleration
Masato Edahiro (NEC Corp./Univ. of Tokyo., Japan)

3D: Tuesday, January 20, 15:55-18:00, Room 416+417
Invited Talks: "Hardware Dependent Software for Multi- and Many-Core Embedded Systems"

3D-1: Introduction to Hardware-dependent Software Design
Rainer Dömer (Univ. of California, Irvine, United States), Andreas Gerstlauer (Univ. of Texas, Austin, United States), Wolfgang Müller (Univ. of Paderborn, Germany)

3D-2: Using a Dataflow abstracted Virtual Prototype for HdS Design
Wolfgang Ecker, Stefan Heinen (Infineon Technologies AG, Germany)

3D-3: Needs and Trends in Embedded Software Development for Consumer Electronics
Yasutaka Tsunakawa (Sony Corp., Japan)

3D-4: Hardware-dependent Software Synthesis for Many-Core Embedded Systems
Samar Abdi, Gunar Schirner, Ines Viskic, Hansu Cho, Yonghyun Hwang, Lochi Yu, Daniel Gajski (Univ. of California, Irvine, United States)

4D: Wednesday, January 21, 10:15-12:20, Room 416+417
Invited Talks: "Challenges in 3D Integrated Circuit Design"

4D-1: Three-Dimensional Integration Technology and Integrated Systems
Mitsumasa Koyanagi, Takafumi Fukushima, Tetsu Tanaka (Tohoku Univ., Japan)

4D-2: A 3D Prototyping Chip based on a Wafer-level Stacking Technology
Nobuaki Miyakawa (Honda Research Institute, Japan)

4D-3: Design and CAD Challenges for 3D ICs
David Kung, Ruchir Puri (IBM Corp., United States)

4D-4: Addressing Thermal and Power Delivery Bottlenecks in 3D Circuits
Sachin S. Sapatnekar (Univ. of Minnesota, United States)

4D-5: The Road to 3D EDA Tool Readiness
Charles Chiang, Subarna Sinha (Synopsys, United States)

9D: Thursday, January 22, 15:55-18:00, Room 416+417
Invited Talks + Panel Discussion: "Dependable VLSI: Device, Design and Architecture – How should they cooperate ? –"

Organizer: Shuichi Sakai (Univ. of Tokyo, Japan)
Panelists: Hidetoshi Onodera (Kyoto Univ., Japan)
Hiroto Yasuura (Kyushu Univ., Japan)
James C. Hoe (Carnegie Mellon Univ., United States)

Designers' Forum

5D: Wednesday, January 21, 13:30-15:35, Room 416+417
Invited Talks: "Consumer SoCs"

5D-1: Development of Full-HD Multi-standard Video CODEC IP Based on Heterogeneous Multiprocessor Architecture
Hiroaki Nakata, Koji Hosogi, Masakazu Ehama, Takafumi Yuasa, Toru Fujihira (Hitachi, Ltd., Japan), Kenichi Iwata, Motoki Kimura, Fumitaka Izuhara, Seiji Mochizuki, Masaki Nobori (Renesas Technology Corp., Japan)

5D-2: A 65nm Dual-Mode Baseband and Multimedia Application Processor SoC with Advanced Power and Memory Management
Tatsuya Kamei, Tetsuhiro Yamada, Takao Koike, Masayuki Ito, Takahiro Irita, Kenichi Nitta, Toshihiro Hattori, Shinichi Yoshioka (Renesas Technology Corp., Japan)

5D-3: UniPhier: Series Development and SoC Management
Yoshito Nishimichi, Nobuo Higaki, Masataka Osaka, Seiji Horii, Hisato Yoshida (Panasonic Corp., Japan)

7D: Thursday, January 22, 10:15-12:20, Room 416+417
Invited Talks: "Analog/RF Circuit Designs"

7D-1: Design Methods for Pipeline & Delta-Sigma A-to-D Converters with Convex Optimization
Kazuo Matsukawa, Takashi Morie, Yusuke Tokunaga, Shiro Sakiyama, Yosuke Mitani, Masao Takayama, Takuji Miki, Akinori Matsumoto, Koji Obata, Shiro Dosho (Panasonic Corp., Japan)

7D-2: A Low-Jitter 1.5-GHz and Large-EMI reduction 10-dBm Spread-Spectrum Clock Generator for Serial-ATA
Takashi Kawamoto, Masaru Kokubo (Hitachi, Ltd., Japan)

7D-3: RF-Analog Circuit Design in Scaled SoC
Nobuyuki Itoh, Mototsugu Hamada (Toshiba Corp., Japan)

7D-4: An Approach to the RF-LSI Design for Ubiquitous Communication Appliances
Yuichi Kado, Mitsuru Harada (NTT, Japan)

6D: Wednesday, January 21, 15:55-18:00, Room 416+417
Panel Discussion: "ESL Design Methods"

Moderator: Takashi Hasegawa (Fujitsu Microelectronics Ltd., Japan)
Panelists: Simon Bloch (Mentor Graphics Corporation, United States)
Ahmed Jerraya (CEA-LETI, France)
Gabriela Nicolescu (Ecole Polytechnique de Montreal, Canada)
Shigeru Oho (Hitachi, Ltd., Japan)
Koichiro Yamashita (Fujitsu Labs. Ltd., Japan)

8D: Thursday, January 22, 13:30-15:35, Room 416+417
Panel Discussion: "Near-Future SoC Architectures – Can Dynamically Reconfigurable Processors be a Key Technology?"
Moderator: Hideharu Amano (Keio Univ., Japan)
Panelists: Toru Awashima (NEC Corp., Japan)
Hisanori Fujisawa (Fujitsu Labs. Ltd., Japan)
Naohiko Irie (Hitachi, Ltd., Japan)
Takashi Miyamori (Toshiba Corp., Japan)
Tony Stansfield (Panasonic Europe Ltd., Great Britain)

One Full-Day and Six Half-Day Tutorials

FULL-DAY Tutorial:
Monday, January 19, 2009, 9:30-17:00

1 **Software Development and Programming of Multi-core LSI**
Organizer: ***Ahmed Amine Jerraya*** - TIMA, France
Speakers: ***Wayne Wolf*** - Georgia Institute of Technology, United States ***Damir Jamsek*** - IBM, United States ***Hiroyuki Tomiyama*** - Nagoya Univ., Japan ***Fabien Clermidy*** - CEA-LETI, France

HALF-DAY Tutorials:
Monday, January 19, 2009, 9:30-12:30

2 **Formal Methods for C-Based Embedded System Design Verification — Technical Trends and Practical Aspects —**
Organizer: ***Masahiro Fujita*** - Univ. of Tokyo, Japan
Speakers: ***Masahiro Fujita*** - Univ. of Tokyo, Japan ***Alan J. Hu*** - Univ. of British Columbia, Canada ***Andy Chou*** - Coverity Inc., United States

3 **Statistical Design on the Verge of Maturity: Revisiting the Foundation**
Organizer: ***Michael Orshansky*** - Univ. of Texas, Austin, United States
Speakers: ***Sani Nassif*** - IBM, United States ***Michael Orshansky*** - Univ. of Texas, Austin, United States

Monday, January 19, 2009, 9:30-12:30 and 14:00-17:00

4, 5 **Circuit Reliability: Modeling, Simulation, and Resilient Design Solutions**
Section I (morning): Reliability Mechanisms and the Impact on IC Design
Section II (afternoon): Circuit Aging Prediction and Resilient Design
Organizer: ***Yu (Kevin) Cao*** - Arizona State Univ., United States
Speakers (Section I): ***Yu (Kevin) Cao*** - Arizona State Univ., United States ***Kaushik Roy*** - Purdue Univ., United States
Speakers (Section II): ***Marek Patyra*** - Intel, United States ***Subhasish Mitra*** - Stanford Univ., United States

Monday, January 19, 2009, 14:00-17:00

6 **Recent Advances in Low-Leakage VLSI Design**
Organizer: ***Youngsoo Shin*** - KAIST, Korea
Speaker: ***Youngsoo Shin*** - KAIST, Korea ***Kaushik Roy*** - Purdue Univ., United States

7 **Memory Architectures and Software Transformations for System Level Design**
Organizer: ***Nikil Dutt*** - Univ. of California, Irvine, United States
Speaker: ***Stylianos Mamagkakis*** - IMEC, Belgium ***Preeti Panda*** - Indian Institute of Technology, Delhi, India

Welcome to ASP-DAC 2009

On behalf of the Organizing Committee, I would like to invite you to attend the Asia and South Pacific Design Automation Conference 2009 (ASP-DAC 2009), being held here at Pacifico Yokohama, Japan, from January 19 through 22, 2009, jointly with the Electronic Design and Solution Fair 2009. ASP-DAC 2009 offers an ideal place for all these people to meet and exchange ideas about the challenges and solutions for the future. I hope you visit the conference to learn about all the latest advances in electronic design technology and automation.

The heart of conference is the technical program. ASP-DAC 2009 received 355 submissions from 33 countries/regions. Based on the result of a rigorous and thorough review followed by a full day face-to-face discussion, 116 papers were selected and compiled into an exciting program.

Each day, the technical program starts with a keynote address. This year, ASP-DAC is proud to present three keynote presentations from leading-edge company's leaders and academia. On Tuesday, Mr. Mitsuo Saito, Chief Fellow and VP of Engineering, Toshiba Corporation Semiconductor Company, will present some examples of the relationship between the design methodology revolution and the microprocessor evolution and the special requirements to the EDA industry for the next generation of SoCs and multi core processors. On Wednesday, Professor Wolfgang Rosenstiel, University of Tuebingen, will discuss possibilities and limitations of system level automated synthesis and verification of embedded systems. On Thursday, Dr. Leon Stok, Director, Electronic Design Automation, IBM Systems and Technology Group, will discuss if design rules can still be described in terms of restrictions for the coming technologies or if new approaches are needed.

The Designers' Forum is our unique program that will share design experience and solutions of actual product designs of the industries. This year's program will include invited talks of up-to-date consumer SoCs and analog technologies, panels of upstream design methods and dynamic reconfigurable processors.

The University Design Contest is also an important annual event of ASP-DAC where 23 designs were selected for presentation.

On Monday, one full-day and six half-day tutorials are scheduled to provide introductions to hot topics such as design for variability, reliable circuit design, low leakage design, multi-core software development, embedded system design, and functional verification.

An event like ASP-DAC doesn't just happen. I wish to express my appreciation to all authors, speakers, reviewers, session organizers, session chairs, panelists, keynote speakers and tutors. Also, I sincerely thank the members of the Organizing Committee, the Technical Program Committee, the University Design Contest Committee, the Technical Liaison and the Steering Committee.

Finally, special thanks to the all ASP-DAC attendees — we are sure you will have a productive and exciting experience at ASP-DAC 2009.

Kazutoshi Wakabayashi
General Chair
ASP-DAC 2009

Message from Technical Program Committee

On behalf of the Technical Program Committee of the Asia and South Pacific Design Automation Conference (ASP-DAC) 2009, we would like to welcome all of you to the conference held from January 19 through 22, 2009 at Pacifico Yokohama Conference Center in Yokohama, Japan.

This year, ASPDAC received 355 paper submissions, which is about the same as last year. The submissions span close to 30 countries/regions in Asia, North America, South America, Europe, Oceania, Australia and Africa. The Technical Program Committee was composed of 95 professionals who are experts on EDA, IC design, and system design, and was organized into 13 subcommittees. All committee members contributed to in-depth, rigorous and thorough reviews and most of them attended the paper selection meeting. Through a full day face-to-face discussion, 116 quality papers have been selected and compiled into 24 technical sessions in a three-day, three parallel tracks program. The program is further enriched by three keynote addresses, an additional track of special sessions and panels, and excellent tutorial sessions. We sincerely hope you will enjoy and benefit from the program.

Each day, technical session starts with a keynote address which is organized under the leadership of Dr. Kazutoshi Wakabayashi, General Chair. We have 9 special sessions on Track D (1D - 9D). On Tuesday, we have University LSI Design Contest session (1D), and sessions (2D and 3D) for recent advances on EDA area using novel hightly parallel architectures. On Wednesday, we have a session 3D for three dimensional integrated circuit design isuues and two designers' forum sessions (5D and 6D) for consumer SoCs and a panel discussion on ESL design methods. On Thursday, we have two designers' forum session on analog/RF circuits and on near-future SoC architectures, and an attracting special panel on Dependable VLSI device, design and architecture. These special sessions covers novel and exciting topics and we hope that you can find some hint to the futher research and development on LSI.

Finally, we would like to thank all people contributed to the 2009 event. At first, we should thank to all the authors who submitted excellent quality papers, since their contributions form the basis of our technical excellence. We also would like to thank to members of Organizing and Technical Program Commiiteees, the members of Industry Liaison, organizers of special sessions and the conference secretariat (JESA).

Looking forward to meeting with you at ASP-DAC 2009.

Ren-Song Tsay
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ASP-DAC 2009
Shinji Kimura
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[3] Embedded and Real-Time Systems

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[4] High-Level/Behavioral/Logic Synthesis and Optimization

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[5] Validation and Verification for Behavioral/Logic Design

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[6] Physical Design (Routing)

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[7] Physical Design (Placement)

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[8] Timing, Power, Thermal Analysis and Optimization

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[9] Signal/power Integrity, Interconnect/Device/Circuit Modeling and Simulation

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[10] Design for Manufacturability/Yield and Statistical Design

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[11] Test and Design for Testability

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[12] Analog, RF and Mixed Signal Design and CAD

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[13] Emerging Technologies and Applications

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University LSI Design Contest

The University LSI Design Contest was conceived as a unique program of ASP-DAC Conference. The purpose of the Contest is to encourage education and research in LSI design, and its realization on chips at universities, and other educational organizations by providing opportunities to present and discuss innovative and stateof-the-art designs at the conference. Application areas and types of circuits include (1) Analog, RF and Mixed-Signal Circuits, (2) Digital Signal processing, (3) Microprocessors, and (4) Custom Application Specific Circuits and Memories. Methods or technology used for implementation include (a) Full Custom and Cell-Based LSIs, (b) Gate Arrays, and (c) Field Programmable Devices, including FPGA/PLDs. This year, 23 selected designs from five countries/areas will be disclosed in Session 1D with a short presentations followed by live discussions in front of posters with light meals. Submitted designs were reviewed by the members of the University Design Contest Committee. As a result, the 23 designs were selected. Also, we have instituted one outstanding design award and one special feature award.

It is with great pleasure that we acknowledge the contributions to the Design Contest, and it is our earnest belief that it will promote and enhance research and education in LSI design in academic organizations. It is also our hope that many people not only in academia but in industry will attend the contest and enjoy the stimulating discussions.

Date, Time and Locations:

Oral Presentation 10:15-12:20, January 20, 2009, Room 416+417

Poster Presentation 12:20-13:30, January 20, 2009, Room 418 (Food will be served.)

University LSI Design Contest Committee
Co-Chairs

Kazutoshi Kobayashi
Kyoto University

Kenichi Okada
Tokyo Institute of Technology

Designers' Forum

Designers' Forum is conceived as a unique program that shares the design experience and solutions of real product developments among LSI designers and EDA academia/developers. It consists of these four special sessions:

Oral Sessions:	5D Consumer SoCs
	7D Analog/RF Circuit Designs
Panel Discussions:	6D ESL Design Methods
	8D Near-Future SoC Architectures

Designs will be presented focusing mainly on the design styles, problems and ways to tackle these. Panel discussions will also be held concerning the latest design problems. The following gives detailed information of each session:

Session 5D (13:30-15:35, Jan 21st) [Consumer SoCs] — This session deals with real SoC design for consumer electronics devices. Three presentations will be given from Hitachi, Renesas and Panasonic. Hitachi will introduce a video codec design on heterogeneous multi-processor architecture. Renesas will show a dual-mode baseband processor on a 65nm process and Panasonic will present their SoC development strategy using the common SoC platform Uniphier.

Session 7D (10:15-12:20, Jan 22nd) [Analog/RF Circuit Designs] — Four presentations on practical design of analog circuits will be given by Hitachi, Toshiba, Panasonic and NTT. Hitachi will introduce a spread spectrum clock generator for the serial ATA interface. Toshiba will show an RF circuit design in scaled SoC. Panasonic will introduce a strategic optimization method for pipeline and delta-sigma ADC. NTT will show a body area network.

Session 6D (15:55-18:00, Jan 21st) [ESL Design Methods] — Panelists from LSI design companies, tool venders and academic institute will discuss about the latest ESL (Electronic System Level) design methodologies/tools and their use in practical SoC designs. Panelists will introduce tool flow and LSI design experiences using UML, MATLAB, SystemC and other high abstraction level modeling languages and tools.

Session 8D (13:30-15:35, Jan 22nd) [Near-Future SoC Architectures — Can Dynamically Reconfigurable Processors be a Key Technology?] — Panelists from Hitachi, Toshiba, Panasonic Europe, Fujitsu and NEC will discuss the latest dynamic reconfigurable processor technologies, their practical use in consumer electronics devices, and their future expansion.

Designers' Forum Chair
Kunihiro Asada
University of Tokyo
Designers' Forum Chair
Kunio Uchiyama
Hitachi, Ltd.
Designers' Forum Vice Chair
Makoto Ikeda
University of Tokyo
Designers' Forum Vice Chair
Sumio Morioka
NEC Corporation

Student Forum at ASP-DAC 2009

A poster session for graduate students to present their research work is held during ASP-DAC 2009. This is a great opportunity for students to get feedback and have discussion with people from academia and industry.

Date and Time: 12:20-13:30, January 21, 2009

Location: Room 418 (Food will be served.)

We would like to thank the following poster selection committee members that evaluated the submissions,

- Koji Hashimoto (Fukuoka University, Japan)
- Tohru Ishihara (Kyushu University, Japan)
- Kazuhito Ito (Saitama University, Japan)
- Yih-Lang Li (National Chiao Tung University, Taiwan)
- Chien-Nan Jimmy Liu (National Central University, Taiwan)
- Yung-Hsiang Lu (Perdue University, United States)
- Nozomu Togawa (Waseda University, Japan)
- Chun-Yao Wang (National Tsing Hua University, Taiwan)
- David Wu (Chinese University of Hong Kong, Hong Kong)
- Chia-Lin Yang (National Taiwan University, Taiwan)

The sponser of this forum is Technical Group on VLSI Design Technologies (TGVLD) of the Institute of Electronics, Information and Communication Engineers (IEICE). We would also like to thank ASP-DAC 2009 for sponsoring the event. Special thanks to Dr. Farzan Fallah and Professor Atsushi Takahashi for supporting and contributing to the Student Forum.

Co-Chairs

Yasuhiro Takashima
University of Kitakyushu
Ting-Chi Wang
National Tsing Hua University

ASP-DAC 2009 Best Papers

Best Paper Candidates

1A-1 **Adaptive Inter-router Links for Low-Power, Area-Efficient and Reliable Network-on-Chip (NoC) Architectures**
Avinash Karanth Kodi (Ohio Univ., United States), Ashwini Sarathy, Ahmed Louri, Janet Wang (Univ. of Arizona, United States)

1C-1 **FastYield: Variation-Aware, Layout-Driven Simultaneous Binding and Module Selection for Performance Yield Optimization**
Gregory Lucas, Scott Cromar, Deming Chen (Univ. of Illinois, Urbana-Champaign, United States)

3A-1 **System-Level Cost Analysis and Design Exploration for Three-Dimensional Integrated Circuits (3D ICs)**
Xiangyu Dong, Yuan Xie (Pennsylvania State Univ., United States)

4B-3 **Analog Placement with Common Centroid and 1-D Symmetry Constraints**
Linfu Xiao, Evangeline Young (Chinese Univ. of Hong Kong, Hong Kong)

4C-1 **Stochastic Current Prediction Enabled Frequency Actuator for Runtime Resonance Noise Reduction**
Yiyu Shi (Univ. of California, Los Angeles, United States), Jinjun Xiong, Howard Chen (IBM, United States), Lei He (Univ. of California, Los Angeles, United States)

5B-1 **Efficient Analytical Determination of the SEU-induced Pulse Shape**
Rajesh Garg, Sunil P Khatri (Texas A&M Univ., United States)

5C-1 **Efficiently Finding the 'Best' Solution with Multi-Objectives from Multiple Topologies in Topology Library of Analog Circuit**
Yu Liu, Masato Yoshioka, Katsumi Homma, Toshiyuki Shibuya (Fujitsu Laboratories Ltd., Japan)

6B-1 **Efficient Simulated Evolution Based Rerouting and Congestion-Relaxed Layer Assignment on 3-D Global Routing**
Ke-Ren Dai, Wen-Hao Liu, Yih-Lang Li (National Chiao Tung Univ., Taiwan)

7B-1 **Dependent Latch Identification in the Reachable State Space**
Chen-Hsuan Lin, Chun-Yao Wang (National Tsing Hua Univ., Taiwan)

8A-1 **Improving Scalability of Model-Checking for Minimizing Buffer Requirements of Synchronous Dataflow Graphs**
Nan Guan (Northeastern Univ., China), Zonghua Gu (HKUST, China), Wang Yi (Uppsala Univ., Sweden), Ge Yu (Northeastern Univ., China)

8B-1 **A Novel Toffoli Network Synthesis Algorithm for Reversible Logic**
Yexin Zheng, Chao Huang (Virginia Tech, United States)

8C-4 **Design for Burn-In Test: A Technique for Burn-In Thermal Stability under Die-to-Die Parameter Variations**
Mesut Meterelliyoz, Kaushik Roy (Purdue Univ., United States)

Best Paper Award

1C-1 **FastYield: Variation-Aware, Layout-Driven Simultaneous Binding and Module Selection for Performance Yield Optimization**
Gregory Lucas, Scott Cromar, Deming Chen (Univ. of Illinois, Urbana-Champaign, United States)

5C-1 **Efficiently Finding the 'Best' Solution with Multi-Objectives from Multiple Topologies in Topology Library of Analog Circuit**
Yu Liu, Masato Yoshioka, Katsumi Homma, Toshiyuki Shibuya (Fujitsu Laboratories Ltd., Japan)

ASP-DAC 2009 Design Contest Award

Best Design Award

1D-1 **A Wireless Real-Time On-Chip Bus Trace System**
Shusuke Kawai, Takayuki Ikari (Keio Univ., Japan), Yutaka Takikawa (Renesas Design Corp, Japan), Hiroki Ishikuro, Tadahiro Kuroda (Keio Univ., Japan)

Special Feature Award

1D-13 **Ultra Low-Power ANSI S1.11 Filter Bank for Digital Hearing Aids**
Yu-Ting Kuo, Tay-Jyi Lin, Yueh-Tai Li (National Chiao Tung Univ., Taiwan), Chou-Kun Lin (ITRI, STC, Taiwan), Chih-Wei Liu (National Chiao Tung Univ., Taiwan)

Invitation to ASP-DAC 2010

On behalf of the Organizing Committee, I would like to invite you to the 2010 Asia and South-Pacific Design Automation Conference (ASP-DAC 2010) to be held on January 18-21, 2010 in Taipei, Taiwan. This is the first time that ASP-DAC comes to Taiwan. Taiwan is the place where many electronics systems and semiconductor devices are designed and manufactured. We have a very large community of academic researchers and industrial practitioners who are eager to interact with the world EDA community. In other words, Taiwan is a very good market for EDA ideas.

Taipei is the capital city of Taiwan. It is easily accessible by direct flight from major cities around the world. You will find many interesting places to visit. In addition to regular conference activity, the Organizing Committee will organize several social activities to enrich your trip.

Since 2006, in order to maintain quality and consistency of its technical program, ASP-DAC has established a rotation rule that includes the separation of the Technical Program Committee from the Organizing Committee. The 2010 Technical Program Committee will be under the leadership of Professor Shinji Kimura of Waseda University, Japan. I solicit your support to the conference by submitting your research work to the ASP-DAC 2010.

I hope you will have a successful ASP-DAC 2009 in Yokohama and look forward to seeing you all in Taipei in 2010.

Youn-Long Lin
General Chair
ASP-DAC 2010

About ASP-DAC

The ASP-DAC, is a premier Design Automation and Design conference, especially for Asian and South Pacific Electronic Design Automation and Design community, providing a forum to present and exchange ideas in order to promote the research, and accelerating cooperation between the IC Design and Design methodologies. The conference attendees are primarily developers of the EDA/CAD Tools and designers of VLSI circuits & systems (IP & SoC).

Keynote Addresses

Opening & Keynote I
Tuesday, January 20, 8:30-10:00,
Small Auditorium, 5F
"Challenges to EDA System from the View Point of Processor Design and Technology Drivers"
Mitsuo Saito
Chief Fellow and VP of Engineering
Toshiba Corporation Semiconductor Company, Japan

Historically, many microprocessors have been developed, since it was invented in early 1970's. Microprocessor design was always under the hardest competition, so they had been the technology driver for the semiconductor technology and the design methodology until recently.

By discussing the relationship between the design methodology (EDA) revolution and the technology driver products transition, based upon famous Makimoto's wave hypothesis, what happened to the microprocessor world is highlighted by showing typical examples.

As a recent example, the positioning of the Cell Broadband Engine as a high performance computing processor and as a flexible HW, is discussed mainly, also the performance result, and the future trend of the microprocessors towards multi-core are discussed. Then it is explained, why SpursEngine derived from Cell Broadband Engine had to be developed.

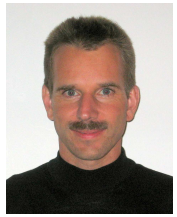
SoC (combination of microprocessor and HW functional unit) for custom applications should be the technology driver, for the next decade, which is the first experience after microprocessor was born. The special requirements to the EDA system to realize next wave, are predicted.

Finally, when the next wave comes, maybe after 2017, software centric era, what happens to the world, is briefly mentioned.

Keynote II
Wednesday, January 21, 9:00-10:00,
Small Auditorium, 5F
"Automated Synthesis and Verification of Embedded Systems: Wishful Thinking or Reality?"
Wolfgang Rosenstiel
Professor, Chair for Computer Engineering and Director
Wilhelm-Schickard-Institute for Informatics, University of Tuebingen, Germany

More complex embedded hardware/software systems have to be developed with shorter design time and reduced cost. One solution for this problem is increasing design automation starting from higher levels of abstraction. Automatic synthesis and verification has been around in research for a quite a while. This talk will show examples for state-of-the art tools for system-level synthesis and verification of embedded systems and demonstrate their possibilities and limitations by some automotive applications.

Keynote III
Thursday, January 22, 9:00-10:00,
Small Auditorium, 5F
"From Restrictive to Prescriptive Design"



Leon Stok
Director, Electronic Design Automation
IBM Systems and Technology Group,
United States

For many generations the hand-off between design and manufacturing has been done by a set of design rules. However, design rule manuals have grown in size from several tens of pages a few generations back to hundreds of pages now. Many more design rules have been added since the end of traditional scaling. Even with all these additional rules, corner cases are found late in the process that can become significant yield or functionality detractors. Restricted Design Rules (RDRs) have been created to simplify the design rules and come up with more manufacturable designs. IBM has practiced RDRs in the last few process generations but is this enough? For the next technology nodes no new exposure tools will be available for mass production and optical scaling is coming to a halt. Computational scaling will be required to extend Moore's law. In this new era, can we keep on describing design rules in terms of restrictions or do we need another approach?

Technical Program

Tuesday, January 20, 8:30 - 10:00

Tuesday, January 20, 8:30 - 10:00 Small Auditorium, 5F
Session 1K: Opening and Keynote Session I

Chair: ***Kazutoshi Wakabayashi*** – NEC Corp., Japan

Challenges to EDA System from the View Point of Processor Design and Technology Drivers
Mitsuo Saito (Toshiba Corp. Semiconductor Company, Japan)

Tuesday, January 20, 10:15 - 12:20

Tuesday, January 20, 10:15 - 12:20 Room 411+412
Session 1A: On-Chip Communication Architectures

Chair: ***Sri Parameswaran*** – Univ. of New South Wales, Australia

1A-1 Adaptive Inter-router Links for Low-Power, Area-Efficient and Reliable Network-on-Chip (NoC) Architectures
Avinash Karanth Kodi (Ohio Univ., United States), Ashwini Sarathy, Ahmed Louri, Janet Wang (Univ. of Arizona, United States)

1A-2 Analysis of Communication Delay Bounds for Network on Chips
Yue Qian (National Univ. of Defense Tech., China), Zhonghai Lu (Royal Inst. of Tech., Sweden), Wenhua Dou (National Univ. of Defense Tech., China)

1A-3 Frequent Value Compression in Packet-based NoC Architectures
Ping Zhou, Bo Zhao, Yu Du, Yi Xu, Youtao Zhang, Jun Yang (Univ. of Pittsburgh, United States), Li Zhao (Intel, United States)

1A-4 Simultaneous Data Transfer Routing and Scheduling for Interconnect Minimization in Multicycle Communication Architecture
Yu-Ju Hong (Purdue Univ., United States), Ya-Shih Huang, Juinn-Dar Huang (National Chiao Tung Univ., Taiwan)

1A-5 Dynamically Reconfigurable On-Chip Communication Architectures for Multi Use-Case Chip Multiprocessor Applications
Sudeep Pasricha, Nikil Dutt, Fadi Kurdahi (Univ. of California, Irvine, United States)

Tuesday, January 20, 10:15 - 12:20 Room 413
Session 1B: Dealing with Thermal Issues

Chairs: ***Youngsoo Shin*** – KAIST, Republic of Korea
Li Shang – Univ. of Colorado, Boulder, United States

1B-1 Stochastic Thermal Simulation Considering Spatial Correlated Within-Die Process Variations
Pei-Yu Huang, Jia-Hong Wu, Yu-Min Lee (National Chiao Tung Univ., Taiwan)

1B-2 A Control Theory Approach for Thermal Balancing of MPSoC
Francesco Zanini, David Atienza, Giovanni De Micheli (EPFL, Switzerland)

1B-3 Thermal Optimization in Multi-Granularity Multi-Core Floorplanning
Michael B. Healy, Hsien-Hsin S. Lee, Gabriel H. Loh, Sung Kyu Lim (Georgia Inst. of Tech., United States)

1B-4 Temperature-Aware Dynamic Frequency and Voltage Scaling for Reliability and Yield Enhancement
Yu-Wei Yang, Katherine Shu-Min Li (National Sun Yat-Sen Univ., Taiwan)

1B-5 A Multiple Supply Voltage Based Power Reduction Method in 3-D ICs Considering Process Variations and Thermal Effects
Shih-An Yu, Pei-Yu Huang, Yu-Min Lee (National Chiao Tung Univ., Taiwan)

Tuesday, January 20, 10:15 - 12:20 Room 414+415
Session 1C: Advances in Behavioral Synthesis

Chairs: ***Shigeru Yamashita*** – NAIST, Japan
Kiyoung Choi – Seoul National Univ., Republic of Korea

1C-1 FastYield: Variation-Aware, Layout-Driven Simultaneous Binding and Module Selection for Performance Yield Optimization
Gregory Lucas, Scott Cromar, Deming Chen (Univ. of Illinois, Urbana-Champaign, United States)

1C-2 CriAS: A Performance-Driven Criticality-Aware Synthesis Flow for On-Chip Multicycle Communication Architecture
Chia-I Chen, Juinn-Dar Huang (National Chiao Tung Univ., Taiwan)

1C-3 Tolerating Process Variations in High-Level Synthesis Using Transparent Latches
Yibo Chen, Yuan Xie (Pennsylvania State Univ., United States)

1C-4 Variation-Aware Resource Sharing and Binding in Behavioral Synthesis
Feng Wang (Qualcomm Inc., United States), Yuan Xie (Pennsylvania State Univ., United States), Andres Takach (Mentor Graphics Corp., United States)

1C-5 Peak Temperature Control in Thermal-aware Behavioral Synthesis through Allocating the Number of Resources
Junbo Yu, Qiang Zhou, Jinian Bian (Tsinghua Univ., China)

Tuesday, January 20, 10:15 - 12:20 Room 416+417

Session 1D: University LSI Design Contest

Chairs: ***Jiun-In Guo*** – National Chung Cheng Univ., Taiwan
Hiroki Ishikuro – Keio Univ., Japan

1D-1 A Wireless Real-Time On-Chip Bus Trace System
Shusuke Kawai, Takayuki Ikari (Keio Univ., Japan), Yutaka Takikawa (Renesas Design Corp, Japan), Hiroki Ishikuro, Tadahiro Kuroda (Keio Univ., Japan)

1D-2 CKVdd: A Self-Stabilization Ramp-Vdd Technique for Dynamic Power Reduction
Chin-Hsien Wang, Ching-Hwa Cheng (Feng Chia Univ., Taiwan), Jiun-In Guo (National Chung Cheng Univ., Taiwan)

1D-3 A 300 nW, 7 ppm/°C CMOS Voltage Reference Circuit based on Subthreshold MOSFETs
Ken Ueno (Hokkaido Univ., Japan), Tetsuya Hirose (Kobe Univ., Japan), Tetsuya Asai, Yoshihito Amemiya (Hokkaido Univ., Japan)

1D-4 A 100Mbps, 0.19mW Asynchronous Threshold Detector with DC Power-Free Pulse Discrimination for Impulse UWB Receiver
Lechang Liu, Yoshio Miyamoto, Zhiwei Zhou, Kosuke Sakaida, Jisun Ryu, Koichi Ishida, Makoto Takamiya, Takayasu Sakurai (Univ. of Tokyo, Japan)

1D-5 Low-Power CMOS Transceiver Circuits for 60GHz Band Millimeter-wave Impulse Radio
Ahmet Oncu, Minoru Fujishima (Univ. of Tokyo, Japan)

1D-6 An Inductor-less MPPT Design for Light Energy Harvesting Systems
Hui Shao, Chi-Ying Tsui, Wing-Hung Ki (HKUST, Hong Kong)

1D-7 A 1 GHz CMOS Comparator with Dynamic Offset Control Technique
Xiaolei Zhu (Keio Univ., Japan), Sanroku Tsukamoto (Fujitsu Laboratories Ltd., Japan), Tadahiro Kuroda (Keio Univ., Japan)

1D-8 Circuit Design Using Stripe-Shaped PMELA TFTs on Glass
Keita Ikai, Jinmyoung Kim, Makoto Ikeda, Kunihiro Asada (Univ. of Tokyo, Japan)

1D-9 Low Energy Level Converter Design for Sub-V_{th} Logics
Hui Shao, Chi-Ying Tsui (HKUST, Hong Kong)

1D-10 A Time-to-Digital Converter with Small Circuitry
Kazuya Shimizu, Masato Kaneta, HaiJun Lin, Haruo Kobayashi, Nobukazu Takai (Gunma Univ., Japan), Masao Hotta (Musashi Inst. of Tech., Japan)

1D-11 A V_{DD} Independent Temperature Sensor Circuit with Scaled CMOS Process
Hiroki Oshiyama, Toshihiro Matsuda, Kei-ichi Suzuki, Hideyuki Iwata (Toyama Prefectural Univ., Japan), Takashi Ohzone (Dawn Enterprise Co. Ltd., Japan)

1D-12 A Current-mode DC-DC Converter using a Quadratic Slope Compensation Scheme
Chihiro Kawabata, Yasuhiro Sugimoto (Chuo Univ., Japan)

1D-13 Ultra Low-Power ANSI S1.11 Filter Bank for Digital Hearing Aids
Yu-Ting Kuo, Tay-Jyi Lin, Yueh-Tai Li (National Chiao Tung Univ., Taiwan), Chou-Kun Lin (ITRI, STC, Taiwan), Chih-Wei Liu (National Chiao Tung Univ., Taiwan)

1D-14 An 11,424 Gate-Count Dynamic Optically Reconfigurable Gate Array with a Photodiode Memory Architecture
Daisaku Seto, Minoru Watanabe (Shizuoka Univ., Japan)

1D-15 A Low-Power FPGA Based on Autonomous Fine-Grain Power-Gating
Shota Ishihara, Masanori Hariyama, Michitaka Kameyama (Tohoku Univ., Japan)

1D-16 A 52-mW 8.29mm^2 19-mode LDPC Decoder Chip for Mobile WiMAX Applications
Xin-Yu Shih, Cheng-Zhou Zhan, Cheng-Hung Lin, An-Yeu (Andy) Wu (National Taiwan Univ., Taiwan)

1D-17 A Full-Synthesizable High-Precision Built-In Delay Time Measurement Circuit
Ming-Chien Tsai, Ching-Hwa Cheng (Feng Chia Univ., Taiwan)

1D-18 A Dynamic Quality-Scalable H.264 Video Encoder Chip
Hsiu-Cheng Chang, Yao-Chang Yang, Jia-Wei Chen (National Chung Cheng Univ., Taiwan), Ching-Lung Su (National Yunlin Univ. of Science and Tech., Taiwan), Cheng-An Chien, Jiun-In Guo, Jinn-Shyan Wang (National Chung Cheng Univ., Taiwan)

1D-19 A High Performance LDPC Decoder for IEEE802.11n Standard
Wen Ji, Yuta Abe, Takeshi Ikenaga, Satoshi Goto (Waseda Univ., Japan)

1D-20 Design and Chip Implementation of the Ubiquitous Processor HCgorilla
Masa-aki Fukase, Kazunori Noda, Atsuko Yokoyama, Tomoaki Sato (Hirosaki Univ., Japan)

1D-21 An 8.69 Mvertices/s 278 Mpixels/s Tile-based 3D Graphics SoC HW/SW Development for Consumer Electronics
Liang-Bi Chen, Ruei-Ting Gu, Wei-Sheng Huang, Chien-Chou Wang, Wen-Chi Shiue, Tsung-Yu Ho, Yun-Nan Chang, Shen-Fu Hsiao, Chung-Nan Lee, Ing-Jer Huang (National Sun Yat-Sen Univ., Taiwan)

1D-22 A Multi-Task-Oriented Security Processing Architecture with Powerful Extensibility
Dan Cao, Jun Han, Xiao-yang Zeng, Shi-ting Lu (Fudan Univ., China)

1D-23 A Delay-Optimized Universal FPGA Routing Architecture
Fang Wu, Huowen Zhang, Lei Duan, Jinmei Lai, Yuan Wang, Jiarong Tong (Fudan Univ., China)

Tuesday, January 20, 13:30 - 15:35

Tuesday, January 20, 13:30 - 15:35 Room 411+412
Session 2A: MPSoC and IP Integration

Chairs: ***Nozomu Togawa*** – Waseda Univ., Japan
Marcello Lajolo – NEC Laboratories America, United States

2A-1 Timing Variation-Aware Task Scheduling and Binding for MPSoC
HaNeul Chon, Taewhan Kim (Seoul National Univ., Republic of Korea)

2A-2 Flexible and Abstract Communication and Interconnect Modeling for MPSoC
Katalin Popovici (TIMA Lab., France), Ahmed Jerraya (CEA-LETI, Minatec, France)

2A-3 Partial Order Method for Timed Simulation of System-Level MPSoC Designs
Eric Cheung, Harry Hsieh (Univ. of California, Riverside, United States), Felice Balarin (Cadence Design Systems, United States)

2A-4 A UML-Based Approach for Heterogeneous IP Integration
Zhenxin Sun, Weng-Fai Wong (National Univ. of Singapore, Singapore)

Tuesday, January 20, 13:30 - 15:35 Room 413
Session 2B: Power Analysis and Optimization

Chair: ***Masanori Hashimoto*** – Osaka Univ., Japan

2B-1 Statistical Modeling and Analysis of Chip-Level Leakage Power by Spectral Stochastic Method
Ruijing Shen, Ning Mi, Sheldon Tan (Univ. of California, Riverside, United States), Yici Cai, Xianlong Hong (Tsinghua Univ., China)

2B-2 On the Futility of Statistical Power Optimization
Jason Cong, Puneet Gupta, John Lee (Univ. of California, Los Angeles, United States)

2B-3 Timing Driven Power Gating in High-Level Synthesis
Shih-Hsu Huang, Chun-Hua Cheng (Chung Yuan Christian Univ., Taiwan)

2B-4 Congestion-Aware Power Grid Optimization for 3D Circuits Using MIM and CMOS Decoupling Capacitors
Pingqiang Zhou, Karthikk Sridharan, Sachin S. Sapatnekar (Univ. of Minnesota, United States)

2B-5 Incremental and On-demand Random Walk for Iterative Power Distribution Network Analysis
Yiyu Shi, Wei Yao (Univ. of California, Los Angeles, United States), Jinjun Xiong (IBM, United States), Lei He (Univ. of California, Los Angeles, United States)

Tuesday, January 20, 13:30 - 15:35 Room 414+415
Session 2C: Logic and Arithmetic Optimization

Chairs: ***Dale Edwards*** – Semiconductor Research Corp., United States
Hiroyuki Higuchi – Fujitsu Microelectronics Ltd., Japan

2C-1 SAT-Controlled Redundancy Addition and Removal — A Novel Circuit Restructuring Technique
Chi-An Wu, Ting-Hao Lin, Shao-Lun Huang, Chung-Yang (Ric) Huang (National Taiwan Univ., Taiwan)

2C-2 On Improved Scheme for Digital Circuit Rewiring and Application on Further Improving FPGA Technology Mapping
Fu Shing Chim, Tak Kei Lam, Yu Liang Wu (Chinese Univ. of Hong Kong, Hong Kong)

2C-3 Hybrid LZA: A Near Optimal Implementation of the Leading Zero Anticipator
Amit Verma (National Inst. of Tech., Rourkela, India), Ajay K. Verma, Philip Brisk, Paolo Ienne (EPFL, Switzerland)

2C-4 An Optimized Design for Serial-Parallel Finite Field Multiplication over GF(2^m) Based on All-One Polynomials
Pramod Kumar Meher (Nanyang Technological Univ., Singapore), Yajun Ha (National Univ. of Singapore, Singapore), Chiou-Yng Lee (Lunghwa Univ. of Science and Tech., Taiwan)

Tuesday, January 20, 13:30 - 15:35 Room 416+417
Session 2D: Special Session: EDA Acceleration Using New Architectures

Organizer: ***Damir A. Jamsek*** – IBM Corp., United States

2D-1 Aspects of GPU for General Purpose High Performance Computing
Reiji Suda (Univ. of Tokyo/JST CREST, Japan), Takayuki Aoki (Tokyo Inst. of Tech./JST CREST, Japan), Shoichi Hirasawa (Univ. of Electro-Communications/JST CREST, Japan), Akira Nukada (Tokyo Inst. of Tech./JST CREST, Japan), Hiroki Honda (Univ. of Electro-Communications/JST CREST, Japan), Satoshi Matsuoka (Tokyo Inst. of Tech./JST CREST/NII, Japan)

2D-2 Designing and Optimizing Compute Kernels on Nvidia GPUs
Damir A. Jamsek (IBM Research, United States)

2D-3 Parallelizing Fundamental Algorithms such as Sorting on Multi-core Processors for EDA Acceleration
Masato Edahiro (NEC Corp./Univ. of Tokyo, Japan)

Tuesday, January 20, 15:55 - 18:00

Tuesday, January 20, 15:55 - 18:00 Room 411+412
Session 3A: System-Level Design of 3D Chips and Configurable Systems

Chairs: ***Eui-Young Chung*** – Yonsei Univ., Republic of Korea
Steve Haga – National Sun Yat-Sen Univ.

3A-1 System-Level Cost Analysis and Design Exploration for Three-Dimensional Integrated Circuits (3D ICs)
Xiangyu Dong, Yuan Xie (Pennsylvania State Univ., United States)

3A-2 Synthesis of Networks on Chips for 3D Systems on Chips
Srinivasan Murali, Ciprian Seiculescu (EPFL, Switzerland), Luca Benini (Univ. of Bologna, Italy), Giovanni De Micheli (EPFL, Switzerland)

3A-3 An Application-centered Design Flow for Self Reconfigurable Systems Implementation
Fabio Cancare, Marco Domenico Santambrogio, Donatella Sciuto (Politecnico di Milano, Italy)

3A-4 System-Level Process Variability Compensation on Memory Organizations. On the Scalability of Multi-Mode Memories
Concepción Sanz, Manuel Prieto, José Ignacio Gómez (Univ. Complutense de Madrid, Spain), Antonis Papanikolaou, Francky Catthoor (Inter-Univ. Microelectronics Center, Belgium)

Tuesday, January 20, 15:55 - 18:00 Room 413
Session 3B: Advances in Timing Analysis and Modeling

Chairs: ***Shih-Hsu Huang*** – Chung Yuan Christian Univ., Taiwan
Atsushi Takahashi – Tokyo Inst. of Tech., Japan

3B-1 Accelerating Statistical Static Timing Analysis Using Graphics Processing Units
Kanupriya Gulati, Sunil P. Khatri (Texas A&M Univ., United States)

3B-2 Trade-off Analysis between Timing Error Rate and Power Dissipation for Adaptive Speed Control with Timing Error Prediction
Hiroshi Fuketa, Masanori Hashimoto, Yukio Mitsuyama, Takao Onoye (Osaka Univ., Japan)

3B-3 Statistical Analysis of On-Chip Power Grid Networks by Variational Extended Truncated Balanced Realization Method
Duo Li, Sheldon Tan (Univ. of California, Riverside, United States), Gengsheng Chen, Xuan Zeng (Fudan Univ., China)

3B-4 Bound-Based Identification of Timing-Violating Paths Under Variability
Lin Xie, Azadeh Davoodi (Univ. of Wisconsin at Madison, United States)

3B-5 Adaptive Techniques for Overcoming Performance Degradation due to Aging in Digital Circuits
Sanjay Kumar, Chris Kim, Sachin S. Sapatnekar (Univ. of Minnesota, United States)

Tuesday, January 20, 15:55 - 18:00 Room 416+417
Session 3D: Special Session: Hardware Dependent Software for Multi- and Many-Core Embedded Systems

Organizers: ***Rainer Doemer*** – Univ. of California, Irvine, United States
Andreas Gerstlauer – Univ. of Texas, Austin, United States
Wolfgang Mueller – Univ. of Paderborn, Germany

3D-1 Introduction to Hardware-dependent Software Design
Rainer Dömer (Univ. of California, Irvine, United States), Andreas Gerstlauer (Univ. of Texas, Austin, United States), Wolfgang Müller (Univ. of Paderborn, Germany)

3D-2 Using a Dataflow abstracted Virtual Prototype for HdS-Design
Wolfgang Ecker, Stefan Heinen, Michael Velten (Infineon Technologies AG, Germany)

3D-3 Needs and Trends in Embedded Software Development for Consumer Electronics
Yasutaka Tsunakawa (Sony Corp., Japan)

3D-4 Hardware-dependent Software Synthesis for Many-Core Embedded Systems
Samar Abdi, Gunar Schirner, Ines Viskic, Hansu Cho, Yonghyun Hwang, Lochi Yu, Daniel Gajski (Univ. of California, Irvine, United States)

Wednesday, January 21, 9:00 - 10:00

Wednesday, January 21, 9:00 - 10:00 Small Auditorium, 5F
Session 2K: Keynote Session II

Chair: ***Kazutoshi Wakabayashi*** – NEC Corp., Japan

Automated Synthesis and Verification of Embedded Systems: Wishful Thinking or Reality?
Wolfgang Rosenstiel (Wilhelm-Schickard-Institute for Informatics, Univ. of Tuebingen, Germany)

Wednesday, January 21, 10:15 - 12:20

Wednesday, January 21, 10:15 - 12:20 Room 411+412
Session 4A: System Level Architectures

Chair: ***Samar Abdi*** – Univ. of California, Irvine, United States

4A-1 Computation and Data Transfer Co-Scheduling for Interconnection Bus Minimization
Cathy Qun Xu (Univ. of Texas, Dallas, United States), Chun Jason Xue, Bessie C Hu (City Univ. of Hong Kong, Hong Kong), Edwin H.M. Sha (Univ. of Texas, Dallas, United States)

4A-2 Prototyping Pipelined Applications on a Heterogeneous FPGA Multiprocessor Virtual Platform
Antonino Tumeo, Marco Branca, Lorenzo Camerini, Marco Ceriani (Politecnico di Milano, Italy), Matteo Monchiero (HP Labs, United States), Gianluca Palermo, Fabrizio Ferrandi, Donatella Sciuto (Politecnico di Milano, Italy)

4A-3 Variability-Aware Robust Design Space Exploration of Chip Multiprocessor Architectures
Gianluca Palermo, Cristina Silvano, Vittorio Zaccaria (Politecnico di Milano, DEI, Italy)

4A-4 Partial Conflict-Relieving Programmable Address Shuffler for Parallel Memories in Multi-Core Processor
Young-Su Kwon, Bon-Tae Koo, Nak-Woong Eum (ETRI, Republic of Korea)

4A-5 HitME: Low Power Hit MEmory Buffer for Embedded Systems
Andhi Janapsatya, Sri Parameswaran, Aleksandar Ignjatovic (Univ. of New South Wales, Australia)

Wednesday, January 21, 10:15 - 12:20 Room 413

Session 4B: Beyond Traditional Floorplanning and Placement

Chair: ***Shigetoshi Nakatake*** – Univ. of Kitakyushu, Japan

4B-1 Signal Skew Aware Floorplanning and Bumper Signal Assignment Technique for Flip-Chip
Cheng-Yu Wang, Wai-Kei Mak (National Tsing Hua Univ., Taiwan)

4B-2 A Novel Thermal Optimization Flow Using Incremental Floorplanning for 3D ICs
Xin Li, Yuchun Ma, Xianlong Hong (Tsinghua Univ., China)

4B-3 Analog Placement with Common Centroid and 1-D Symmetry Constraints
Linfu Xiao, Evangeline Young (Chinese Univ. of Hong Kong, Hong Kong)

4B-4 A Multilevel Analytical Placement for 3D ICs
Jason Cong, Guojie Luo (Univ. of California, Los Angeles, United States)

4B-5 Exploring Adjacency in Floorplanning
Jia Wang, Hai Zhou (Northwestern Univ., United States)

Wednesday, January 21, 10:15 - 12:20 Room 414+415

Session 4C: Signal/Power Integrity and Simulation

Chairs: ***Hideki Asai*** – Shizuoka Univ., Japan
Sheldon Tan – Univ. of California, Riverside, United States

4C-1 Stochastic Current Prediction Enabled Frequency Actuator for Runtime Resonance Noise Reduction
Yiyu Shi (Univ. of California, Los Angeles, United States), Jinjun Xiong, Howard Chen (IBM, United States), Lei He (Univ. of California, Los Angeles, United States)

4C-2 Fast Analysis of Nontree-Clock Network Considering Environmental Uncertainty by Parameterized and Incremental Macromodeling
Hai Wang (Univ. of California, Riverside, United States), Hao Yu (Berkeley Design Automation, United States), Sheldon X.D. Tan (Univ. of California, Riverside, United States)

4C-3 High Performance On-Chip Differential Signaling Using Passive Compensation for Global Communication
Ling Zhang, Yulei Zhang (Univ. of California, San Diego, United States), Akira Tsuchiya (Kyoto Univ., Japan), Masanori Hashimoto (Osaka Univ., Japan), Ernest Kuh (Univ. of California, Berkeley, United States), Chung-Kuan Cheng (Univ. of California, San Diego, United States)

4C-4 Noise Minimization During Power-Up Stage for a Multi-Domain Power Network
Wanping Zhang (Qualcomm Inc./Univ. of California, San Diego, United States), Yi Zhu (Univ. of California, San Diego, United States), Wenjian Yu (Tsinghua Univ., China), Amirali Shayan, Renshen Wang (Univ. of California, San Diego, United States), Zhi Zhu (Qualcomm Inc., United States), Chung-Kuan Cheng (Univ. of California, San Diego, United States)

4C-5s Parallel Transistor Level Circuit Simulation using Domain Decomposition Methods
He Peng, Chung-Kuan Cheng (Univ. of California, San Diego, United States)

4C-6s Fast Circuit Simulation on Graphics Processing Units
Kanupriya Gulati (Texas A&M Univ., United States), John F. Croix (Nascentric, Inc., United States), Sunil P. Khatri (Texas A&M Univ., United States), Rahm Shastry (Nascentric, Inc., United States)

Wednesday, January 21, 10:15 - 12:20 Room 416+417

Session 4D: Special Session: Challenges in 3D Integrated Circuit Design

Organizer: ***Sachin Sapatnekar*** – Univ. of Minnesota, United States

4D-1 Three-Dimensional Integration Technology and Integrated Systems
Mitsumasa Koyanagi, Takafumi Fukushima, Tetsu Tanaka (Tohoku Univ., Japan)

4D-2 A 3D Prototyping Chip based on a Wafer-level Stacking Technology
Nobuaki Miyakawa (Honda Research Institute, Japan)

4D-3 CAD Challenges for 3D ICs
David Kung, Ruchir Puri (IBM Corp., United States)

4D-4 Addressing Thermal and Power Delivery Bottlenecks in 3D Circuits
Sachin S. Sapatnekar (Univ. of Minnesota, United States)

4D-5 The Road to 3D EDA Tool Readiness
Charles Chiang, Subarna Sinha (Synopsys, United States)

Wednesday, January 21, 13:30 - 15:35

Wednesday, January 21, 13:30 - 15:35 Room 411+412

Session 5A: Energy-Aware System Level Design Methodology

Chairs: ***Chia-Lin Yang*** – National Taiwan Univ., Taiwan
Juinn-Dar Huang – National Chiao Tung Univ.

5A-1 Energy-aware HW/SW Co-synthesis Algorithm for Heterogeneous NoC
Qingli Zhang, Mingyan Yu, Fangfa Fu, Peng Yun, Junjie Song, Min Fan (Harbin Inst. of Tech., China)

5A-2 System-Level Exploration Tool for Energy-Aware Memory Management in the Design of Multidimensional Signal Processing Systems
Florin Balasa (Southern Utah Univ., United States), Ilie I. Luican (Univ. of Illinois, Chicago, United States), Hongwei Zhu (ARM, Inc., United States), Doru V. Nasui (American International Radio, Inc., United States)

5A-3 Systematic Architecture Exploration based on Optimistic Cycle Estimation for Low Energy Embedded Processors
Ittetsu Taniguchi (Osaka Univ., Japan), Murali Jayapala (IMEC vzw., Belgium), Praveen Raghavan, Francky Catthoor (IMEC vzw./K.U.Leuven, Belgium), Keishi Sakanushi, Yoshinori Takeuchi, Masaharu Imai (Osaka Univ., Japan)

5A-4 A Framework for Estimating NBTI Degradation of Microarchitectural Components
Michael DeBole, Ramakrishnan Krishnan (Pennsylvania State Univ., United States), Varsha Balakrishnan, Wenping Wang (Arizona State Univ., United States), Hong Luo, Yu Wang (Tsinghua Univ., China), Yuan Xie (Pennsylvania State Univ., United States), Yu Cao (Arizona State Univ., United States), N. Vijaykrishnan (Pennsylvania State Univ., United States)

Wednesday, January 21, 13:30 - 15:35 Room 413

Session 5B: Design for Manufacturing and Reliability

Chair: ***Charles Chiang*** – Synopsys, United States

5B-1 Efficient Analytical Determination of the SEU-induced Pulse Shape
Rajesh Garg, Sunil P. Khatri (Texas A&M Univ., United States)

5B-2 Post-Routing Redundant Via Insertion with Wire Spreading Capability
Cheok-Kei Lei, Po-Yi Chiang, Yu-Min Lee (National Chiao Tung Univ., Taiwan)

5B-3 Accounting for Non-linear Dependence Using Function Driven Component Analysis
Lerong Cheng, Puneet Gupta, Lei He (Univ. of California, Los Angeles, United States)

5B-4 Risk Aversion Min-Period Retiming under Process Variations
Jia Wang, Hai Zhou (Northwestern Univ., United States)

5B-5s Timing Analysis and Optimization Implications of Bimodal CD Distribution in Double Patterning Lithography
Kwangok Jeong, Andrew B. Kahng (Univ. of California, San Diego, United States)

5B-6s Scheduled Voltage Scaling for Increasing Lifetime in the Presence of NBTI
Lide Zhang, Robert Dick (Northwestern Univ., United States)

Wednesday, January 21, 13:30 - 15:35 Room 414+415

Session 5C: Analog, RF and Mixed-Signal CAD

Chairs: ***Eric Keiter*** – Sandia National Laboratories, United States
Chin-Fong Chiu – National Chip Implementation Center, Taiwan

5C-1 Efficiently Finding the 'Best' Solution with Multi-Objectives from Multiple Topologies in Topology Library of Analog Circuit
Yu Liu, Masato Yoshioka, Katsumi Homma, Toshiyuki Shibuya (Fujitsu Laboratories Ltd., Japan)

5C-2 Automated Design and Optimization of Circuits in Emerging Technologies
Rajesh A. Thakker, Chaitanya Sathe, Angada B. Sachid, Maryam Shojaei Baghini, V. Ramgopal Rao, Mahesh B. Patil (IIT Bombay, India)

5C-3 An Automated Design Approach for CMOS LDO Regulators
Samiran DasGupta, Pradip Mandal (IIT Kharagpur, India)

5C-4 A SCORE Macromodel for PLL Designs to Analyze Supply Noise Interaction Issues at Behavioral Level
Chin-Cheng Kuo, Pei-Syun Lin, Chien-Nan Jimmy Liu (National Central Univ., Taiwan)

5C-5 Gen-Adler: The Generalized Adler's Equation for Injection Locking Analysis in Oscillators
Prateek Bhansali, Jaijeet Roychowdhury (Univ. of Minnesota, United States)

Wednesday, January 21, 13:30 - 15:35 Room 416+417

Session 5D: Designers' Forum: Consumer SoC

Chair: ***Yoshio Masubuchi*** – Toshiba Corp., Japan

5D-1 Development of Full-HD Multi-standard Video CODEC IP Based on Heterogeneous Multiprocessor Architecture
Hiroaki Nakata, Koji Hosogi, Masakazu Ehama, Takafumi Yuasa, Toru Fujihira (Hitachi, Ltd., Japan), Kenichi Iwata, Motoki Kimura, Fumitaka Izuhara, Seiji Mochizuki, Masaki Nobori (Renesas Technology Corp., Japan)

5D-2 A 65nm Dual-mode Baseband and Multimedia Application Processor SoC with Advanced Power and Memory Management
Tatsuya Kamei, Tetsuhiro Yamada, Takao Koike, Masayuki Ito, Takahiro Irita, Kenichi Nitta, Toshihiro Hattori, Shinichi Yoshioka (Renesas Technology Corp., Japan)

5D-3 UniPhier: Series Development and SoC Management
Yoshito Nishimichi, Nobuo Higaki, Masataka Osaka, Seiji Horii, Hisato Yoshida (Panasonic Corp., Japan)

Wednesday, January 21, 15:55 - 18:00

Wednesday, January 21, 15:55 - 18:00 Room 411+412

Session 6A: System Level Simulation and Modeling

Chairs: ***Vincent J Mooney*** – Georgia Inst. of Tech., United States
Tsuneo Nakata – Fujitsu Laboratories Ltd., Japan

6A-1 Automatic Instrumentation of Embedded Software for High Level Hardware/Software Co-Simulation
Aimen Bouchhima, Patrice Gerin, Frédéric Pétrot (TIMA Lab., France)

6A-2 Fast and Accurate Performance Simulation of Embedded Software for MPSoC
Eric Cheung, Harry Hsieh (Univ. of California, Riverside, United States), Felice Balarin (Cadence Design Systems, United States)

6A-3 Automatic Generation of Cycle Accurate and Cycle Count Accurate Transaction Level Bus Models from a Formal Model
Chen Kang Lo, Ren Song Tsay (National Tsing Hua Univ., Taiwan)

6A-4 A Combined Analytical and Simulation-Based Model for Performance Evaluation of a Reconfigurable Instruction Set Processor
Farhad Mehdipour (Kyushu Univ., Japan), Hamid Noori (ISIT, Japan), Bahman Javadi (Amirkabir Univ. of Tech., Iran), Hiroaki Honda (ISIT, Japan), Koji Inoue, Kazuaki Murakami (Kyushu Univ., Japan)

Wednesday, January 21, 15:55 - 18:00 Room 413

Session 6B: Chip and Package Routing Techniques

Chairs: ***Ting-Chi Wang*** – National Tsing Hua Univ., Taiwan
Yasuhiro Takashima – Univ. of Kitakyushu, Japan

6B-1 Efficient Simulated Evolution Based Rerouting and Congestion-Relaxed Layer Assignment on 3-D Global Routing
Ke-Ren Dai, Wen-Hao Liu, Yih-Lang Li (National Chiao Tung Univ., Taiwan)

6B-2 FastRoute 4.0: Global Router with Efficient Via Minimization
Yue Xu, Yanheng Zhang, Chris Chu (Iowa State Univ., United States)

6B-3s High-Performance Global Routing with Fast Overflow Reduction
Huang-Yu Chen, Chin-Hsiung Hsu, Yao-Wen Chang (National Taiwan Univ., Taiwan)

6B-4s IO Connection Assignment and RDL Routing for Flip-Chip Designs
Jin-Tai Yan, Zhi-Wei Chen (Chung Hua Univ., Taiwan)

6B-5 On Using SAT to Ordered Escape Problems
Lijuan Luo, Martin D.F. Wong (Univ. of Illinois, Urbana-Champaign, United States)

6B-6 A Fast Longer Path Algorithm for Routing Grid with Obstacles using Biconnectivity based Length Upper Bound
Yukihide Kohira, Suguru Suehiro, Atsushi Takahashi (Tokyo Inst. of Tech., Japan)

Wednesday, January 21, 15:55 - 18:00 Room 416+417
Session 6D: Designers' Forum: ESL Design Methods

ESL Design Methods

Moderator: ***Takashi Hasegawa*** – Fujitsu Microelectronics Ltd., Japan

Panelists: ***Simon Bloch*** – Mentor Graphics Corp., United States
Ahmed Jerraya – CEA-LETI, France
Gabriela Nicolescu – Ecole Polytechnique de Montreal, Canada
Shigeru Oho – Hitachi, Ltd., Japan
Koichiro Yamashita – Fujitsu Labs. Ltd., Japan

Thursday, January 22, 9:00 - 10:00

Thursday, January 22, 9:00 - 10:00 Small Auditorium, 5F
Session 3K: Keynote Session III

Chair: ***Kazutoshi Wakabayashi*** – NEC Corp., Japan

From Restrictive to Prescriptive Design
Leon Stok (IBM, United States)

Thursday, January 22, 10:15 - 12:20

Thursday, January 22, 10:15 - 12:20 Room 411+412
Session 7A: Compilation Techniques for Embedded Systems

Chairs: ***Hiroyuki Tomiyama*** – Nagoya Univ., Japan
Maziar Goudarzi – Kyushu Univ., Japan

7A-1 Thermal-aware Post Compilation for VLIW Architectures
Wen-Wen Hsieh, TingTing Hwang (National Tsing Hua Univ., Taiwan)

7A-2 A Software Solution for Dynamic Stack Management on Scratch Pad Memory
Arun Kannan, Aviral Shrivastava, Amit Pabalkar, Jong-eun Lee (Arizona State Univ., United States)

7A-3 Compiler-Managed Register File Protection for Energy-Efficient Soft Error Reduction
Jongeun Lee, Aviral Shrivastava (Arizona State Univ., United States)

7A-4 Code Decomposition and Recomposition for Enhancing Embedded Software Performance
Youngchul Cho (SAIT, Samsung Electoronics, Republic of Korea), Kiyoung Choi (Seoul National Univ., Republic of Korea)

Thursday, January 22, 10:15 - 12:20 Room 413
Session 7B: Sequential Design Verification

Chairs: ***Yosinori Watanabe*** – Cadence, United States
Chung-Yang Huang – National Taiwan Univ., Taiwan

7B-1 Dependent Latch Identification in the Reachable State Space
Chen-Hsuan Lin, Chun-Yao Wang (National Tsing Hua Univ., Taiwan)

7B-2 Complete-k-Distinguishability for Retiming and Resynthesis Equivalence Checking without Restricting Synthesis
Nikolaos Liveris, Hai Zhou (Northwestern Univ., United States), Prithviraj Banerjee (HP Labs, United States)

7B-3 Disjunctive Transition Relation Decompositions for Multithreaded Image Computation
Stergios Stergiou, Jawahar Jain (Fujitsu Laboratories of America, United States)

7B-4 Multi-Clock SVA Synthesis without Re-writing
Jiang Long, Andrew Seawright, Paparao Kavalipati (Mentor Graphics Corp., United States)

7B-5 Automatic Formal Verification of Clock Domain Crossing Signals
Bing Li, Chris Ka-Kei Kwok (Mentor Graphics Corp., United States)

Thursday, January 22, 10:15 - 12:20 Room 414+415
Session 7C: Scan Test Generation

Chair: ***Satoshi Ohtake*** – NAIST, Japan

7C-1 Fast False Path Identification Based on Functional Unsensitizability Using RTL Information
Yuki Yoshikawa (Hiroshima City Univ., Japan), Satoshi Ohtake (NAIST, Japan), Tomoo Inoue (Hiroshima City Univ., Japan), Hideo Fujiwara (NAIST, Japan)

7C-2 Conflict Driven Scan Chain Configuration for High Transition Fault Coverage and Low Test Power
Zhen Chen, Boxue Yin, Dong Xiang (Tsinghua Univ., China)

7C-3 Dynamic Test Compaction for a Random Test Generation Procedure with Input Cube Avoidance
Irith Pomeranz (Purdue Univ., United States), Sudhakar Reddy (Univ. of Iowa, United States)

7C-4 Detectability of Internal Bridging Faults in Scan Chains
Fan Yang (Univ. of Iowa, United States), Sreejit Chakravarty, Narendra Devta-Prasanna (LSI Corp., United States), Sudhakar M. Reddy (Univ. of Iowa, United States), Irith Pomeranz (Purdue Univ., United States)

7C-5 Fault Modeling and Testing of Retention Flip-Flops in Low Power Designs
Bing-Chuan Bai (National Taiwan Univ., Taiwan), Augusli Kifli (Faraday Technology Corp., Taiwan), Chien-Mo Li (National Taiwan Univ., Taiwan), Kun-Cheng Wu (Faraday Technology Corp., Taiwan)

Thursday, January 22, 10:15 - 12:20 Room 416+417
Session 7D: Designers' Forum: Analog/RF Circuit Designs

Chair: ***Makoto Ikeda*** – Univ. of Tokyo, Japan

7D-1 Design Methods for Pipeline & Delta-Sigma A-to-D Converters with Convex Optimization
Kazuo Matsukawa, Takashi Morie, Yusuke Tokunaga, Shiro Sakiyama, Yosuke Mitani, Masao Takayama, Takuji Miki, Akinori Matsumoto, Koji Obata, Shiro Dosho (Panasonic Corp., Japan)

7D-2 A Low-Jitter 1.5-GHz and Large-EMI reduction 10-dBm Spread-Spectrum Clock Generator for Serial-ATA
Takashi Kawamoto, Masaru Kokubo (Hitachi, Ltd., Japan)

7D-3 RF-Analog Circuit Design in Scaled SoC
Nobuyuki Itoh, Mototsugu Hamada (Toshiba Corp., Japan)

7D-4 An Approach to the RF-LSI Design for Ubiquitous Communication Appliances
Yuichi Kado, Mitsuru Harada (NTT, Japan)

Thursday, January 22, 13:30 - 15:35

Thursday, January 22, 13:30 - 15:35 Room 411+412
Session 8A: High-Level Design and Scheduling

Chairs: ***Yuichi Nakamura*** – NEC Corp., Japan
Keishi Sakanushi – Osaka Univ., Japan

8A-1 Improving Scalability of Model-Checking for Minimizing Buffer Requirements of Synchronous Dataflow Graphs
Nan Guan (Northeastern Univ., China), Zonghua Gu (HKUST, China), Wang Yi (Uppsala Univ., Sweden), Ge Yu (Northeastern Univ., China)

8A-2 A Reverse-Encoding-based on-chip AHB Bus Tracer for Efficient Circular Buffer Utilization
Fu-Ching Yang, Cheng-Lung Chiang, Ing-Jer Huang (National Sun Yat-Sen Univ., Taiwan)

8A-3 Analyzing and Optimizing Energy Efficiency of Algorithms on DVS Systems: a First Step towards Algorithmic Energy Minimization
Tetsuo Yokoyama, Gang Zeng, Hiroyuki Tomiyama, Hiroaki Takada (Nagoya Univ., Japan)

8A-4 Novel Task Migration Framework on Configurable Heterogeneous MPSoC Platforms
Hao Shen, Frédéric Pétrot (TIMA Lab., France)

Thursday, January 22, 13:30 - 15:35 Room 413
Session 8B: Emerging Design Methodologies and Applications

Chair: ***Chin-Long Wey*** – National Central Univ., Taiwan

8B-1 A Novel Toffoli Network Synthesis Algorithm for Reversible Logic
Yexin Zheng, Chao Huang (Virginia Tech, United States)

8B-2 A Cycle-Based Synthesis Algorithm for Reversible Logic
Zahra Sasanian, Mehdi Saeedi, Mehdi Sedighi, Morteza Saheb Zamani (Amirkabir Univ. of Tech., Iran)

8B-3 Array Like Runtime Reconfigurable MIMO Detectors for 802.11n WLAN: A Design Case Study
Pankaj Bhagawat, Rajballav Dash, Gwan Choi (Texas A&M Univ., United States)

8B-4 Mapping method for Dynamically Reconfigurable Architecture
Akira Kuroda, Mayuko Koezuka, Hidenori Matsuzaki, Takashi Yoshikawa, Shigehiro Asano (Toshiba Corp., Japan)

8B-5 A Criticality-Driven Microarchitectural Three Dimensional (3D) Floorplanner
Srinath Sridharan, Michael DeBole, Guangyu Sun, Yuan Xie, Vijaykrishnan Narayanan (Pennsylvania State Univ., United States)

Thursday, January 22, 13:30 - 15:35 Room 414+415
Session 8C: Verification, Test, and Yield

Chairs: ***Yasuo Sato*** – Hitachi, Ltd., Japan
Sudhakar M. Reddy – Univ. of Iowa, United States

8C-1 Self-Adjusting Constrained Random Stimulus Generation Using Splitting Evenness Evaluation and XOR Constraints
Shujun Deng, Zhiqiu Kong, Jinian Bian, Yanni Zhao (Tsinghua Univ., China)

8C-2 Diagnosing Integrator Leakage of Single-Bit First-Order Delta-Sigma Modulator Using DC Input
Xuan-Lun Huang, Chen-Yuan Yang, Jiun-Lang Huang (National Taiwan Univ., Taiwan)

8C-3 Path Selection for Monitoring Unexpected Systematic Timing Effects
Nicholas Callegari, Pouria Bastani, Li-C. Wang (Univ. of California, Santa Barbara, United States), Sreejit Chakravarty, Alexander Tetelbaum (LSI Corp., United States)

8C-4 Design for Burn-In Test: A Technique for Burn-In Thermal Stability under Die-to-Die Parameter Variations
Mesut Meterelliyoz, Kaushik Roy (Purdue Univ., United States)

8C-5 Test Infrastructure Design for Core-Based System-on-Chip Under Cycle-Accurate Thermal Constraints
Thomas Edison Yu, Tomokazu Yoneda (NAIST, Japan), Krishnendu Chakrabarty (Duke Univ., United States), Hideo Fujiwara (NAIST, Japan)

Thursday, January 22, 13:30 - 15:35 Room 416+417

Session 8D: Designers' Forum: Near-Future SoC Architectures – Can Dynamically Reconfigurable Processors be a Key Technology?

Near-Future SoC Architectures – Can Dynamically Reconfigurable Processors be a Key Technology?

Moderator: ***Hideharu Amano*** – Keio Univ., Japan

Panelists: ***Toru Awashima*** – NEC Corp., Japan
Hisanori Fujisawa – Fujitsu Laboratories Ltd., Japan
Naohiko Irie – Hitachi, Ltd., Japan
Takashi Miyamori – Toshiba Corp., Japan
Tony Stansfield – Panasonic Europe Ltd., Great Britain

Thursday, January 22, 15:55 - 18:00

Thursday, January 22, 15:55 - 18:00 Room 411+412

Session 9A: Memory Systems Simulation and Optimization

Chair: ***Zonghua Gu*** – HKUST, Hong Kong

9A-1 Soft Lists: A Native Index Structure for NOR-Flash-Based Embedded Devices
Li-Pin Chang, Chen-Hui Hsu (National Chiao Tung Univ., Taiwan)

9A-2 Energy-aware Register File Re-Partitioning for Clustered VLIW Architectures
Chun Jason Xue, Minming Li, Yingchao Zhao, Bessie Hu (City Univ. of Hong Kong, Hong Kong)

9A-3 Memory Subsystem Simulation in Software TLM/T Models
Eric Cheung, Harry Hsieh (Univ. of California, Riverside, United States), Felice Balarin (Cadence Design Systems, United States)

9A-4 Exact and Fast L1 Cache Simulation for Embedded Systems
Nobuaki Tojo, Nozomu Togawa, Masao Yanagisawa, Tatsuo Ohtsuki (Waseda Univ., Japan)

9A-5 Accuracy-Aware SRAM: A Reconfigurable Low Power SRAM Architecture for Mobile Multimedia Applications
Minki Cho (Georgia Inst. of Tech., United States), Jason Schlessman (Princeton Univ., United States), Wayne Wolf, Saibal Mukhopadhyay (Georgia Inst. of Tech., United States)

Thursday, January 22, 15:55 - 18:00 Room 413

Session 9B: Emerging Technologies

Chair: ***Mehdi Baradaran Tahoori*** – Northeastern Univ., United States

9B-1 High-Speed Low-Power FinFET Based Domino Logic
Seid Hadi Rasouli (Univ. of California, Santa Barbara, United States), Hanpei Koike (AIST, Japan), Kaustav Banerjee (Univ. of California, Santa Barbara, United States)

9B-2 A Stochastic Perturbative Approach to Design a Defect-Aware Thresholder in the Sense Amplifier of Crossbar Memories
M. Haykel Ben Jamaa (EPFL, Switzerland), David Atienza (Univ. Complutense de Madrid, Spain), Yusuf Leblebici, Giovanni De Micheli (EPFL, Switzerland)

9B-3 An Alternate Design Paradigm for Robust Spin-Torque Transfer Magnetic RAM (STT MRAM) from Circuit/Architecture Perspective
Jing Li, Patrick Ndai, Ashish Goel, Haixin Liu, Kaushik Roy (Purdue Univ., United States)

9B-4 A Design Methodology and Device/Circuit/Architecture Compatible Simulation Framework for Low-Power Magnetic Quantum Cellular Automata Systems
Charles Augustine, Behtash Behin-Aein, Xuanyao Fong, Kaushik Roy (Purdue Univ., United States)

9B-5 Reconfigurable Double Gate Carbon Nanotube Field Effect Transistor Based Nanoelectronic Architecture
Bao Liu (Univ. of Texas, San Antonio, United States)

Thursday, January 22, 15:55 - 18:00 Room 416+417

Session 9D: Special Session: Dependable VLSI: Device, Design and Architecture – How should they cooperate ? –

Organizer: ***Shuichi Sakai*** – Univ. of Tokyo, Japan

Dependable VLSI: Device, Design and Architecture – How should they cooperate ? –

Organizer: ***Shuichi Sakai*** – Univ. of Tokyo, Japan

Panelists: ***Hidetoshi Onodera*** – Kyoto Univ., Japan
Hiroto Yasuura – Kyushu Univ., Japan
James C. Hoe – Carnegie Mellon Univ., United States

Tutorials

Tutorial 1 (FULL DAY)
Monday, January 19, 9:30–17:00 Room 411+412

Software Development and Programming of Multicore LSI

Organizer: ***Ahmed Amine Jerraya*** – TIMA, France

Speakers: ***Wayne Wolf*** – Georgia Institute of Technology, United States
Damir Jamsek – IBM, United States
Hiroyuki Tomiyama – Nagoya University, Japan
Fabien Clermidy – CEA-LETI, France

LSI designs integrate an increasing number of heterogeneous programmable units (CPU, ASIP and DSP subsystems) and sophisticated communication interconnects. In conventional computers programming is based on an operating system that fully hide the underlying hardware architecture. Unlike classic computers, the design of LSI includes the building of application specific memory architecture and specific interconnect and other kinds of hardware components required to efficiently executing the software for a well defined class of applications. In this case, the programming model hides both hardware and software interfaces that may include sophisticated communication and synchronization concepts to handle parallel programs running on the processors. When the processors are heterogeneous, multiple software stacks may be required. Additionally, when specific Hardware peripherals are used, the development of Hardware dependent Software (HdS) requires a long, fastidious and error prone development and debug cycle. This full day tutorial deals with challenges and opportunities for the programming of such complex devices.

- Prof. Wayne Wolf will introduce and survey principles for the programming of multicore LSI.
- Dr. Damir Jamsek will detail How to accelerate CAD applications with CUDA programming environment.
- Prof. Hiroyuki Tomiyama will introduce and survey principles for RTOS (real-time operating systems) for multicore LSI.
- Dr. Fabien Clermidy will explore programming future LSI based on Network on Chip.

Tutorial 2 (HALF DAY)
Monday, January 19, 9:30–12:30 Room 413
Formal Methods for C-Based Embedded System Design Verification — Technical Trends and Practical Aspects —

Organizers: ***Masahiro Fujita*** – University of Tokyo, Japan
Speakers: ***Masahiro Fujita*** – University of Tokyo, Japan
Alan J. Hu – University of British Columbia, Canada
Andy Chou – Coverity Inc., United States

Recently there has been significant progress in formal analysis on C/C++ programs. New bugs in Linux kernels, which have several million lines of codes, have been found by formal analysis methods. In embedded system designs, C-based hardware designs are becoming common, and the techniques developed for C/C++ are expected to be applied to hardware design descriptions as well. There are basically three approaches to the verification problem: static analysis based on local traces of the descriptions, model checking with automatic abstraction/reduction of the descriptions, and equivalence checking with efficient identification of the differences between the descriptions. With appropriate usages, all of the three approaches give practical values to designers, and large and real-life design descriptions could be formally analyzed. The point here is how and where the formal methods are applied. Concentrating on their practical aspects, this tutorial gives the state-of-the-art formal methods and implemented tools for C based design descriptions. The tutorial has the following presentations:

- Prof. Masahiro Fujita gives an overview of the three approaches for the formal analysis of C-based design descriptions.
- Dr. Andy Chou presents various static checking methods and implemented tools with their applications to real life C descriptions.
- Prof. Alan J. Hu presents model checking based formal verification of C-based design descriptions with various efficiency increasing techniques
- Prof. Masahiro Fujita describes formal equivalence checking methods and implemented tools targeting designs under typical system level design flows.

Tutorial 3 (HALF DAY)
Monday, January 19, 9:30–12:30 Room 414+415
Statistical Design on the Verge of Maturity: Revisiting the Foundation

Organizer: ***Michael Orshansky*** – University of Texas, Austin, United States
Speakers: ***Sani Nassif*** – IBM, United States
Michael Orshansky – University of Texas, Austin, United States

Statistical analysis and design (optimization) methods have been actively researched over the last five years with hundreds of papers published on the subject. Many novel concepts and models have been presented, and alternative algorithms for SSTA and optimization developed. In this tutorial, we will re-assess the status of statistical analysis and design methodologies; evaluate evidence for its practical use, and point out the limitations of some of the assumptions made in the early years of the discipline.

Physical sources of variability: This tutorial will review the latest sets of variability data collected from state-of-the-art production lines. The validity of some key assumptions often made about data is specifically reviewed:

- Relative amount of variations inter-chip and intra-chip
- Relative amounts of systematic/spatial and truly random variations
- Designer control of variations, i.e. dependence of variation on device geometry and circuit structure
- Methods for reducing the impact of variability, regularity for intra-chip, and adaptation for inter-chip

Statistical timing analysis methods: The state-of-the-art SSTA methods and the patterns of their adoption in industry will be presented. Specifically, this tutorial will describe the use of SSTA as a multi-corner robustness checker.

Statistical/robust optimization: This tutorial will revisit the state of the art in statistical optimization methods for timing and power yield.

Tutorials 4 and 5 (TWO HALF DAYs, morning and afternoon)
Monday, January 19, 9:30–12:30 Room 416+417
Monday, January 19, 14:00–17:00 Room 416+417
Circuit Reliability: Modeling, Simulation, and Resilient Design Solutions
Section I (morning): Reliability Mechanisms and the Impact on IC Design
Section II (afternoon): Circuit Aging Prediction and Resilient Design

Organizer: ***Yu (Kevin) Cao*** – Arizona State University, United States

Section I
Speakers: ***Yu (Kevin) Cao*** – Arizona State University, United States
Kaushik Roy – Purdue University, United States

Section II
Speakers: ***Marek Patyra*** – Intel, United States
Subhasish Mitra – Stanford University, United States

The aggressive scaling of CMOS technology to sub-45nm nodes has inevitably leads to multiple reliability concerns, such as negative-bias-temperature-instability (NBTI), soft errors, and time-dependent-dielectric-breakdown (TDDB). These effects manifest themselves as the temporal degradation of transistor parameters, profoundly affecting all aspects of circuit performance. While traditional research in this area has focused only on technology improvement, ignoring these effects in the design process causes an excessive amount of over-margining. As these reliability concerns become much more severe with continuous scaling, it is critical to understand, simulate, and adaptively mitigate their impact during the design stage.

In this context, this tutorial will present basic and more advanced topics on reliability modeling, simulation, and design solutions, including two sections:

Section I: Reliability Mechanisms and the Impact on IC Design

- The underlying reliability mechanisms
- Compact modeling and analysis techniques of circuit aging
- Circuit design for reliability in both logic and memory circuits

Section II: Circuit Aging Prediction and Resilient Design

- Circuit reliability analysis and prediction
- Test and validation for circuit and product reliability
- Latest design practices for resilience

This tutorial will conclude with a discussion on future reliability challenges, helping shed light on the need of resilient design techniques and tools.

Tutorial 6 (HALF DAY)
Monday, January 19, 14:00–17:00 Room 414+415
Recent Advances in Low-Leakage VLSI Design

Organizer: ***Youngsoo Shin*** – KAIST, Korea
Speaker: ***Youngsoo Shin*** – KAIST, Korea
Kaushik Roy – Purdue University, United States

This tutorial will discuss recent advances for designing low-leakage VLSI circuits, as well as challenges and opportunities for future research and development. The main focus will be on cell-based semi-custom design, where considering the interaction with other tools in standard design flow when new scheme is adopted is very important. The tutorial will start from leakage estimation considering process variations, which is important to further optimization and design planning. The next part of the tutorial will be minimizing leakage when circuit is in active, or in very short idle. Conventional multiple threshold voltage technique will be discussed, but recent advances in the area of sequential circuit design will be a focus. This includes the use of flip-flops of multiple gate-length and mixed threshold voltages, and adopting clock skew scheduling for further reducing leakage of sequential circuits. We will then go on to discuss fast power-gating circuits, including zigzag power-gating, multiple sleep modes, etc. Run-time power-gating will be discussed as well. In the third part of the tutorial, we will address several circuit techniques for reducing standby leakage. This includes standard power-gating, adaptive body-bias, dynamic voltage scaling, and combination of these. Again, the main focus will be on recent advances in these circuit techniques and how to employ these circuits in cell-based semi-custom design.

Tutorial 7 (HALF DAY)
Monday, January 19, 14:00–17:00 Room 413
Memory Architectures and Software Transformations for System Level Design

Organizer: ***Nikil Dutt*** – University of California, Irvine, United States
Speakers: ***Stylianos Mamagkakis*** – IMEC, Belgium
Preeti Panda – Indian Institute of Technology, Delhi, India

Memories continue to dominate the cost, performance and power of LSI designs. As we move towards sub-nanometer technologies, memories are also susceptible to soft-errors and thus affect the reliability of LSI designs. Traditionally memory issues are considered at a late stage in a system-level design flow, often resulting in designs that do not meet performance and/or power budgets, and with unnecessarily large memory footprints for the LSI designs. A memory-aware system level design flow can address these problems by customizing both the underlying memory architectures/organizations, as well as by transforming the system-level source code to generate an input for system-level design that is better tuned to the memory architectures and organizations. Such a ”memory-aware” system level design flow can result in LSI designs exhibiting superior performance, power and memory footprint characteristics. This half-day tutorial will survey emerging memory architectural platforms and organizations, as well as software transformations that enable tuning of system-level applications to exploit the underlying memory organizations and architectures to improve performance, power and code size. Case studies on industrial LSI designs will demonstrate the efficacy of these approaches.

- Prof. Preeti Panda will survey traditional and emerging memory architectures and organizations, including caches, scratchpad memories, buffers, and describe possible ways to exploit them.
- Dr. Stylianos Mamagkakis will present CleanC, a set of techniques and tools that enable source code level parallelization and memory hierarchy/data reuse exploration techniques/tools.

ASP-DAC 2009 at a Glance

Monday, January 19

FULL-DAY Tutorial

TUTORIAL 1 (9:30–17:00) Room 411+412
Software Development and Programming of Multicore LSI

HALF-DAY Tutorials

TUTORIAL 2 (9:30–12:30) Room 413
Formal Methods for C-Based Embedded System Design Verification

TUTORIAL 3 (9:30–12:30) Room 414+415
Statistical Design on the Verge of Maturity: Revisiting the Foundation

TUTORIAL 4 (9:30–12:30) Room 416+417
Circuit Reliability: Modeling, Simulation, and Resilient Design Solutions
Section I: Reliability Mechanisms and the Impact on IC Design

TUTORIAL 5 (14:00–17:00) Room 416+417
Circuit Reliability: Modeling, Simulation, and Resilient Design Solutions
Section II: Circuit Aging Prediction and Resilient Design

TUTORIAL 6 (14:00–17:00) Room 414+415
Recent Advances in Low-Leakage VLSI Design

TUTORIAL 7 (14:00–17:00) Room 413
Memory Architectures and Software Transformations for System Level Design

	Tuesday, January 20			
	A	B	C	D
8:30	**Opening Session & Keynote Address I** (Small Auditorium, 5F)			
10:00	**Break**			
10:15	1A (Room 411+412) On-Chip Communication Architectures	1B (Room 413) Dealing with Thermal Issues	1C (Room 414+415) Advances in Behavioral Synthesis	1D (Room 416+417) University Design Contest
12:20	**Lunch Break / University Design Contest Discussion at ASP-DAC Site (Room 418)**			
13:30	2A (Room 411+412) MPSoC and IP Integration	2B (Room 413) Power Analysis and Optimization	2C (Room 414+415) Logic and Arithmetic Optimization	2D (Room 416+417) Special Session: EDA Acceleration Using New Architectures
15:35	**Coffee Break (Room 418)**			
15:55	3A (Room 411+412) System-Level Design of 3D Chips and Configurable Systems	3B (Room 413) Advances in Timing Analysis and Modeling	3D (Room 416+417) Special Session: Hardware Dependent Software for Multi-Core Embedded Systems	
18:00				

	Wednesday, January 21			
	A	B	C	D
9:00	**Keynote Address II** (Small Auditorium, 5F)			
10:00	**Break**			
10:15	4A (Room 411+412) System Level Architectures	4B (Room 413) Beyond Traditional Floorplanning and Placement	4C (Room 414+415) Signal/Power Integrity and Simulation	4D (Room 416+417) Special Session: Challenges in 3D Integrated Circuit Design
12:20	**Lunch Break / Student Forum (Room 418)**			
13:30	5A (Room 411+412) Energy-Aware System Level Design Methodology	5B (Room 413) Design for Manufacturing and Reliability	5C (Room 414+415) Analog, RF and Mixed-Signal CAD	5D (Room 416+417) Designers' Forum: Consumer SoC
15:35	**Coffee Break (Room 418)**			
15:55	6A (Room 411+412) System Level Simulation and Modeling	6B (Room 413) Chip and Package Routing Techniques	6D (Room 416+417) Designers' Forum Panel: ESL Design Methods	
18:00	Banquet 18:30–20:30 (Room 501+502)			

	Thursday, January 22			
	A	B	C	D
9:00	**Keynote Address III** (Small Auditorium, 5F)			
10:00	**Break**			
10:15	7A (Room 411+412) Compilation Techniques for Embedded Systems	7B (Room 413) Sequential Design Verification	7C (Room 414+415) Scan Test Generation	7D (Room 416+417) Designers' Forum: Analog/RF Circuit Designs
12:20	**Lunch Break**			
13:30	8A (Room 411+412) High-Level Design and Scheduling	8B (Room 413) Emerging Design Methodologies and Applications	8C (Room 414+415) Verification, Test, and Yield	8D (Room 416+417) Designers' Forum Panel: Near-Future SoC Architectures
15:35	**Coffee Break (Room 418)**			
15:55	9A (Room 411+412) Memory Systems Simulation and Optimization	9B (Room 413) Emerging Technologies	9D (Room 416+417) Special Session: Dependable VLSI: Device, Design and Architecture – How Should They Cooperate? –	
18:00				

Information

Proceedings:

ASP-DAC 2009 will be producing two versions of the ASP-DAC 2009 Proceedings; a bound paper version and a CD-ROM version. All papers will be included in both versions. Conference registration in any of the categories will include copies of both versions of the ASP-DAC 2009 Proceedings. Additional Proceedings will be available for purchase at the Conference. Prices are as follows:

Paper Form: ¥5,000; CD-ROM Form: ¥2,000;

Both versions of the proceedings will also be available for purchase after the conference; please contact IEEE for the bound version and ACM SIGDA for the CD-ROM version.

Banquet:

Conference registrants are invited to attend a banquet to be held on January 21, 2009. The banquet will be held from 18:30 to 20:30 at the fifth floor of conference center. Regular Member and Non-member Conference registrants receive a ticket to the banquet when they register at the conference. Full-time students, Designers' Forum-only registrants, and Tutorial-only registrants wishing to attend the banquet will be required to pay ¥5,000 for a ticket when they register on site.

Visa Application:

Without a legal visa, foreign participants may be denied entry into Japan. Please contact your nearest Japanese embassy in order to ensure entry. Notice that the ASP-DAC 2009 Organizing Committee issues the invitation letters and supports the VISA applications only for presenters of the conference papers. All the other attendees have to apply for VISA through their travel agents or by yourself. In some cases it may take two months to obtain a legal visa. The following Web page of Japanese embassy may be helpful.

http://www.mofa.go.jp/j_info/visit/visa/

Insurance:

The organizer cannot accept responsibility for accidents which might occur. Delegates are encouraged to obtain travel insurance (medical, personal accident, and luggage) in their home country prior to departure.

Climate:

The temperature in Yokohama during the period of the Conference ranges between 5°C and 12°C.

Currency Exchange:

Only Japanese Yen(¥) is accepted at ordinary stores and restaurants. Certain foreign currencies may be accepted at a limited number of hotels, restaurants and souvenir shops. You can exchange your currency for Japanese Yen at foreign exchange banks and other authorized money exchange offices with your passport.

Electrical Appliances:

Electrical appliances are supplied on 100 volts in Japan. The frequency is 50 Hz in eastern Japan including Tokyo, Yokohama and 60 Hz in western Japan including Kyoto and Osaka.

Shopping:

The business hours of most department stores are from 10:00 to 20:00. They are open on Sundays and national holidays, but may close on some weekday. Business hours of retail shops differ from one another, but most shops operate from 10:00 to 20:00. Shops are open on Sundays and national holidays.

Sightseeing:

http://www.city.yokohama.jp/ne/info/hotspotE.html

Participants can get sightseeing information at the JTB Travel desk in the Conference site during the Conference period.

CHINA TOWN

Being the largest Chinese settlement in Japan, Chinatown is always alive with people who come to enjoy Chinese food. It is also a fun place for shopping or just walking around its many streets and alleys lined with colorful restaurants, shops overflowing with Chinese goods and stores that sell exotic ingredients and Chinese medicines.

LANDMARK TOWER

296 meters high with 70 stories above ground and three levels underground. It is Japan's tallest skyscraper. A 40-second ride on the world's fastest elevator skyrockets you to the 69th floor's Sky Garden, the highest observatory in Japan.

Hours: 10:00-21:00 Admission: ¥1,000

Access: 3 min. walk from Minato-mirai Station

SANKEIEN GARDEN

A purely Japanese-style landscape garden. Accenting the main garden is an impressive three-story pagoda and graceful garden bridges. Inside contains several old houses and farm buildings as well as Important Cultural Properties such as Rinshunkaku Villa and Chosukaku House.

Hours:9:00-16:30 Admission:¥500

Access: From Sakuragicho Sta., take Bus No. 8 or No. 125 to Honmoku-Sankeien-mae.

MARITIME MUSEUM

The site of the previous Nippon Maru, the former training ship for Japan's Maritime Defense Force. The Yokohama Maritime Museum, which specializes in ports and ships, is located next to the Nippon Maru.

Hours: 10:00-17:00 (Closed Monday) Admission: ¥600

Access: 5 min. walk from Minato-mirai Station

Other Information:

JAPANTOURIST ORGANIZATION
http://www.jnto.go.jp/

YOKOHAMA CONVENTION & VISITORS BUREAU
http://www.welcome.city.yokohama.jp/eng/tourism/

NARITA AIRPORT
http://www.narita-airport.jp/en/

YES ! TOKYO
http://www.tcvb.or.jp/english/

Access to Pacifico Yokohama

●Traffic Information

March, 2005

By Train

- **Shibuya Sta.** — Tokyu Toyoko Line : Limited Express (Direct link to Minato Mirai Line) → Yokohama Sta.
- **Shinjuku Sta.** — JR Shonan Shinjuku Line 29min. → Yokohama Sta.
- **Tokyo Sta.** — JR Tokaido Line 25min. → Yokohama Sta.
- **Shinagawa Sta.** — Keikyu Express : Limited Express 15min. → Yokohama Sta.

By Train & Shinkansen

- **Shin Yokohama Sta.** — JR Yokohama Line 3min. → Kikuna Sta. → Tokyu Toyoko Line 6min (Connecting to Minato Mirai Line 10min. to Minato Mirai Sta.) → Yokohama Sta.
  - JR Yokohama Line (Change to Keihin-Tohoku Line at Higashikanagawa-Sta.) 15min. → Sakuragicho Sta.
  - Yokohama Subway 15min. → Sakuragicho Sta.

By Air

- **Narita Airport** — JR Narita Express 90min. → Yokohama Sta.
- **Narita Airport** — Airport Limousine Bus 90min. (120min. for PACIFICO YOKOHAMA) → Yokohama Sta.
- **Haneda Airport** — Keikyu Express 24min. → YCAT Yokohama City Air Terminal Yokohama St. East.
- **Haneda Airport** — Airport Limousine Bus 30min. → YCAT Yokohama City Air Terminal Yokohama St. East.

Yokohama Sta. → Minato Mirai Line 3min. (Connecting from Tokyu Toyoko Line) → Minato Mirai Sta. (Take Queen's Square Yokohama Exit and go upto 2nd Floor with Red Escalator) → on foot 3min. → **PACIFICO YOKOHAMA**

Yokohama Sta. → by Taxi 7min. (From taxi pool at 2nd basement of Porta shopping mall on the east exit) → **PACIFICO YOKOHAMA**

Sakuragicho Sta. → JR Keihin-Tohoku Line 3min. → Minato Mirai Sta. → on foot 12min. → **PACIFICO YOKOHAMA**

Sakuragicho Sta. → by Bus 7min. (From bus stop #1) → **PACIFICO YOKOHAMA**

Sakuragicho Sta. → by Taxi 5min. → **PACIFICO YOKOHAMA**

■Driving To Pacifico

［From Tokyo］

- **Metropolitan Expressway** — Toward Yokohama Park, Yokohane Route ▶▶▶ Minato Mirai Ramp,3min. ▶▶▶ **PACIFICO YOKOHAMA**
- **Metropolitan Expressway** — Toward Yokohama (over Bay bridge), Wangan Route ▶▶▶ Minato Mirai Ramp,3min. ▶▶▶ **PACIFICO YOKOHAMA**

［From Kansai or Chubu］

- **Tomei Expressway Yokohama Machida IC** — Hodogaya Bypass,20min. ▶ Kariba IC ▶ Toward Yokohama,Metropolitan Expressway,Kariba Route,10min. ▶ Minato Mirai Ramp,3min ▶ **PACIFICO YOKOHAMA**

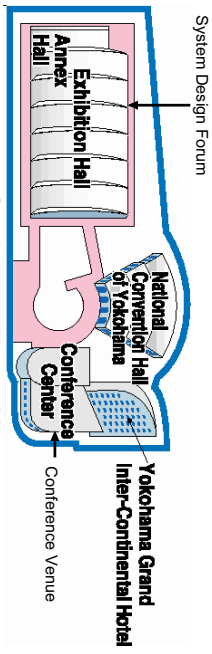
■Parking Lot

Minato Mirai Public Parking Lot +81-45-221-1301	Capacity:1,200（Standard-sized cars only）	Open 24 hours	Rates:Standard-sized car 260yen/30min. (1,300yen for max. 15hours between 8 and 23 on weekdays.)
Bus/Large Vehicles Parking Lot +81-45-221-1302	Capacity:40	Open 24 hours	Rates:Large vehicle 500yen/30min.

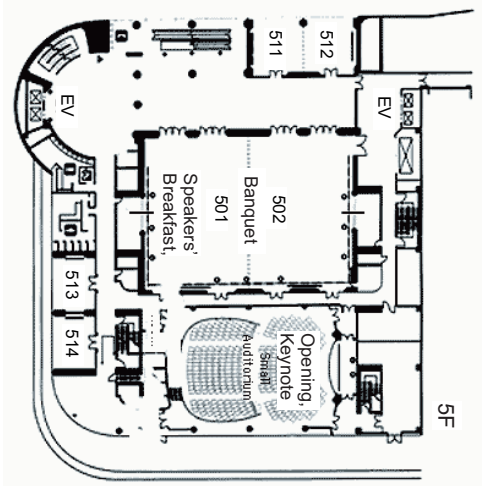
Venue Map/Room Assignment

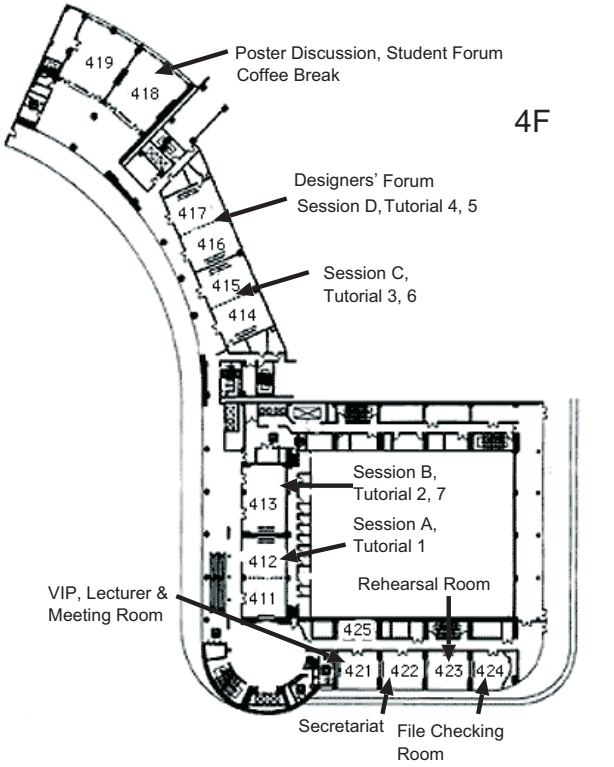
- ASP-DAC Conference is held at "Conference Center."
- EDS Fair 2009 and System Design Forum 2009 are held at "Exhibition Hall/Annex Hall." (2min. walk from Conference Center.)

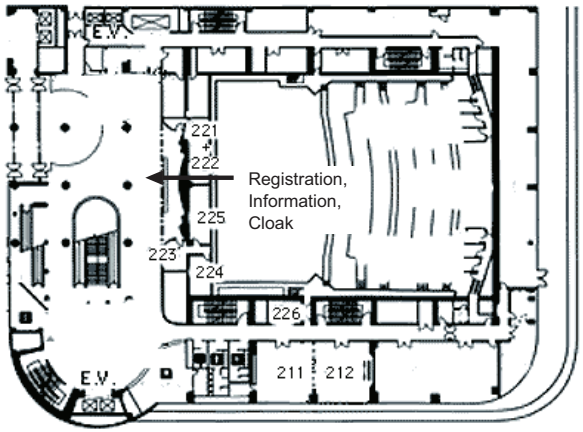
Conference Venue Map



Location	Event
Entrance Hall (2F)	Registration, Information, and Cloak
Small Auditorium (5F)	Opening and Keynotes
411+412 (4F)	Session A and Tutorial 1
413 (4F)	Session B and Tutorials 2 and 7
414+415 (4F)	Session C and Tutorials 3 and 6
416+417 (4F)	Session D, Designers' Forum and Tutorials 4 and 5
418 (4F)	Poster Discussion, Student Forum, and Coffee Break
423 (4F)	Rehearsal Room
424 (4F)	File Checking Room
501+502 (5F)	Banquet, and Speakers' Breakfast
Exhibition Hall/Annex Hall	EDS Fair and System Design Forum







Conference Center Map

Electronic Design and Solution Fair 2009

The Japan Electronics and Information Technology Industries Association (JEITA) will be hosting the Electronic Design and Solution Fair 2009 at the Pacifico Yokohama on January 22 (Thursday) and 23 (Friday), 2009.

The goal of EDSFair is to introduce and disseminate information about the latest design solutions, design technologies and EDA technologies required to produce the electronic systems and semiconductors for the IT applications that will form the foundation of the future information society, whose citizens will enjoy a ubiquitous computing environment. The fair thus contributes to the development of electronics and other IT-related industries. This will be the 16th time the fair has taken place, including its previous incarnation as the EDA TechnoFair.

JEITA forecasts that this year Japan's electronics industry will continuously have achieved a 3% increase over last year, growing for three consecutive years, reaching more than ¥21.trillion since 2006 when Japan's electronics industry recovered to a market size of ¥20.trillion for the first time in 5 years. Also, with the worldwide demand expansion for digital products, semiconductors and electronic components are expected to make sound growth and be placed more expectations on the related development of design technology and service.

"Design the Future! Cutting edge Technologies Excite the Sense" is the theme of this Electronic Design and Solution Fair 2009. You will find on display world-class, cutting-edge technologies tailored for an age that demands new solutions. There are a variety of seminars and a conference offering a wide range of up-to-date information. There are open sessions catering to young engineers, new zones that bring together both Japanese and foreign venture businesses, as well as initiatives for promoting substantive technical exchanges between industry, academia and government.

It is the fervent desire of all of us in JEITA that EDSFair will contribute to enhancing the design technologies available to Japan's electronic and IT industries, and also that both exhibitors and visitors will be able to make the best use of the opportunities afforded by this event for conducting effective and fruitful exchanges of information, and for generating new business. We greatly look forward to your visit at the upcoming EDSFair2009.

Etsuhiko Shoyama
Chairman
Japan Electronics and Information Technology Industries Association (JEITA)

System Design Forum 2009 at EDS Fair

Friday, January 23, 10:00–12:00, 12:45-16:30
Annex Hall, Pacifico Yokohama

Registration: On-line registration will be available from December 2008 at http://www.edsfair.com/e
Sponsor: Japan Electronics and Information Technology Industries Association (JEITA)
Support: Open SystemC Initiative (OSCI)

JEITA EDA Technical Committee (EDA-TC) will host System Design Forum 2009 at Pacifico Yokohama, Japan. This year's forum, consisting of 2 sessions, will be held January 23, 2009.

The first session (10:00–12:00) will cover system-level design language (SystemC), some effective methods for addressing the design crisis of SoC (System-on-a-Chip). Easy-to-understand explanations of the latest standardization, STARC transaction-level modeling Guideline and introduction of the cutting-edge design examples will be given for SystemC.

The second session (12:45–16:30) will focus on predict of 32 nm process variations and design methodology in statistics from the perspective of cutting-edge, and introduce the current state of design methodology on considering variations.

Session 1: SystemC Users Forum 2009, January 23 (10:00–12:00)

Chair: **T. Hasegawa (JEITA SystemC Working Group)**

On December 12, 2005, IEEE approved SystemC (IEEE Std. 1666-2005). Since then, SystemC that is a C-based language, has been widely used as a standard language for both verification and system-level design flows in the fields of both verification and design. Included in this session are: 1) Update of SystemC current status and road map, presented by OSCI, 2) Easy-to-understand explanations of STARC transaction-level modeling Guideline, and 3) Examples of design-related SystemC.

Session 2: Nano-Scale Physical Design Forum, January 23 (12:45-16:30)

Chair: **T. Kanamoto (JEITA Nano-Scale Physical Design Working Group)**

Along with recent advances in semiconductor devices and interconnection technologies, new issues are emerging in current design methodology. Various approaches, such as new

libraries or design schemes, have been developed to solve these issues but left un-standardized even after those become commonplace. It prevents semiconductor manufacturers and their customers from smooth exchanging design information.

In this session, the following topics will be presented to overview the current status of variation-aware design methodology: 1) Variations of device characteristics in the process of next-generation, 2) Variations of circuit characteristics in the process of next-generation, 3) Process variations of SRAM and design methodology in statistics from the perspective of cutting-edge, 4) Design methodology for reducing variation and variations in statistics.

Note: Most of the presentations at the System Design Forum 2009 will be given in Japanese.

For more information, visit the following web site:
http://www.edsfair.com/e/.