D-A Converter Based Variation Analysis for Analog Layout Design

Bo Liu, Toru Fujimura, Bo Yang, and Shigetoshi Nakatake
The University of Kitakyushu, Japan

Contents

Introduction

CS(current source) is an essential function in analog circuit.

Task: its characteristic variation degrades the accuracy performance.

we do ..

- **propose a new evaluation methodology**

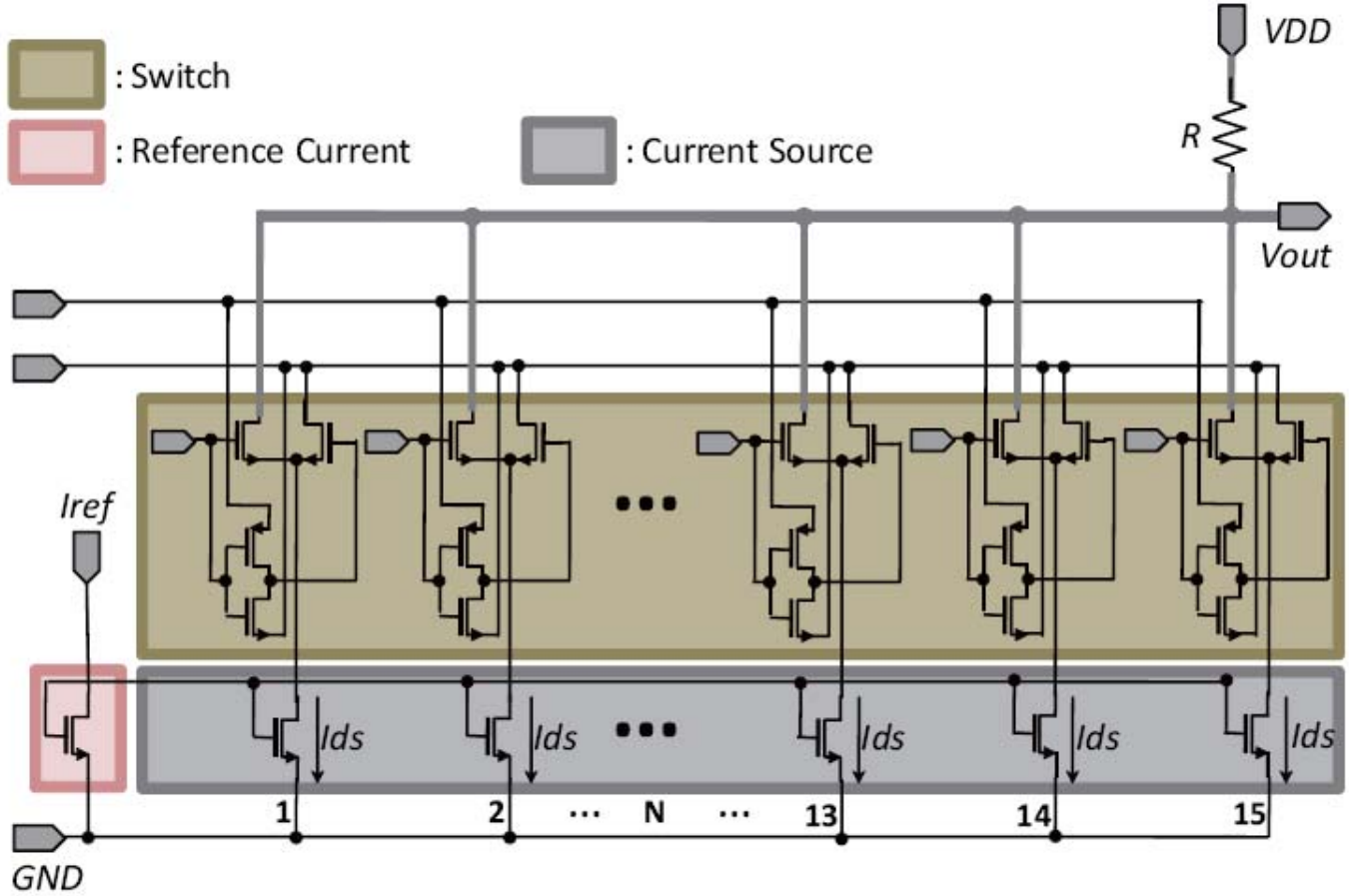
  for analyzing the variation of CS transistor.
- **implement 112-kind current-driven DACs**

  to investigate the dependency of CS upon the relative accuracy and λ .
- **evaluate and analyze the layout-dependent variation**

we find ..

diffusion-sharing and gate-folding significantly influence to the variation of λ and relative accuracy

-- 4-bit current-driven DAC



$$V_{out} = VDD - N_{on} \times I_{ds} \times R$$

N_{on} : **the number of CS transistors switched on**

I_{ds} : **the current value from drain to source**

-- Operating modes of DAC

- Our DACs operate in 2 modes by control signals.
  - Accumulating mode: accumulating CS transistor switched on in (a).
  - 1-bit mode: just one CS transistor turns on in (b).

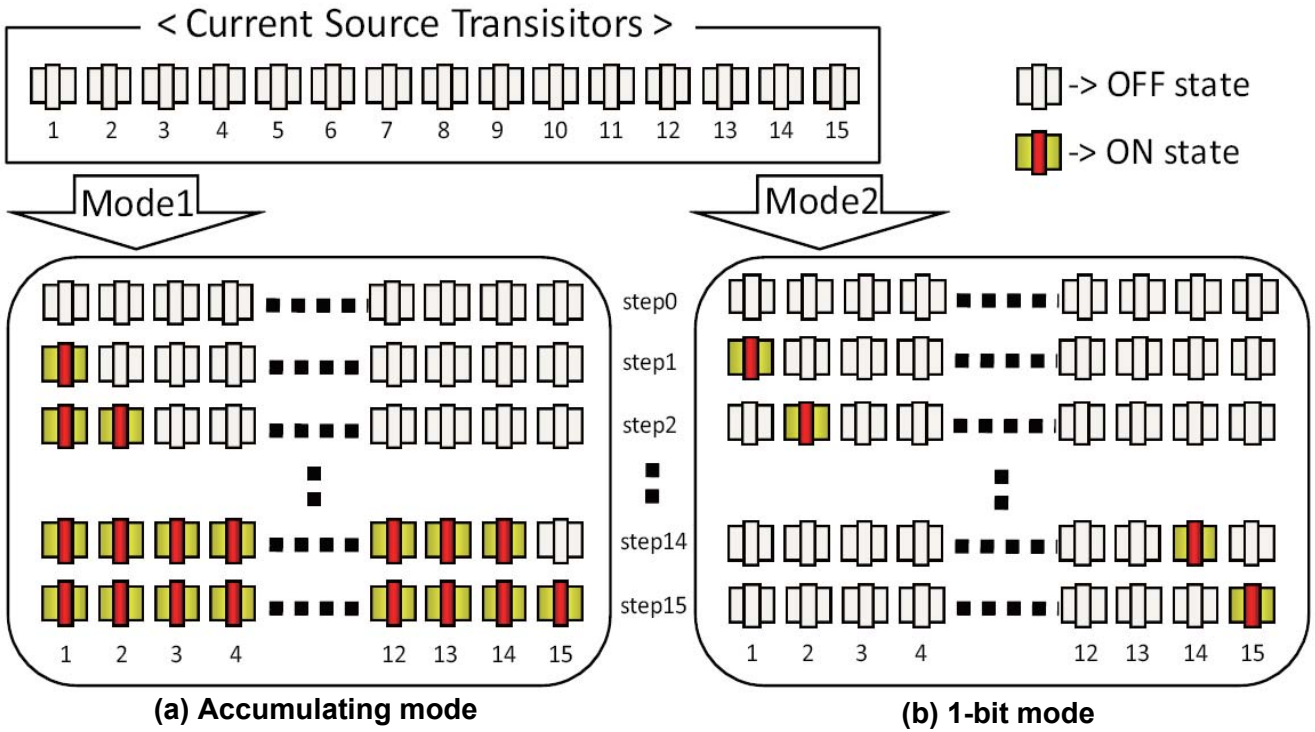


Fig. Operating modes of a 4-bit DAC

--Variation Definition based on DNL

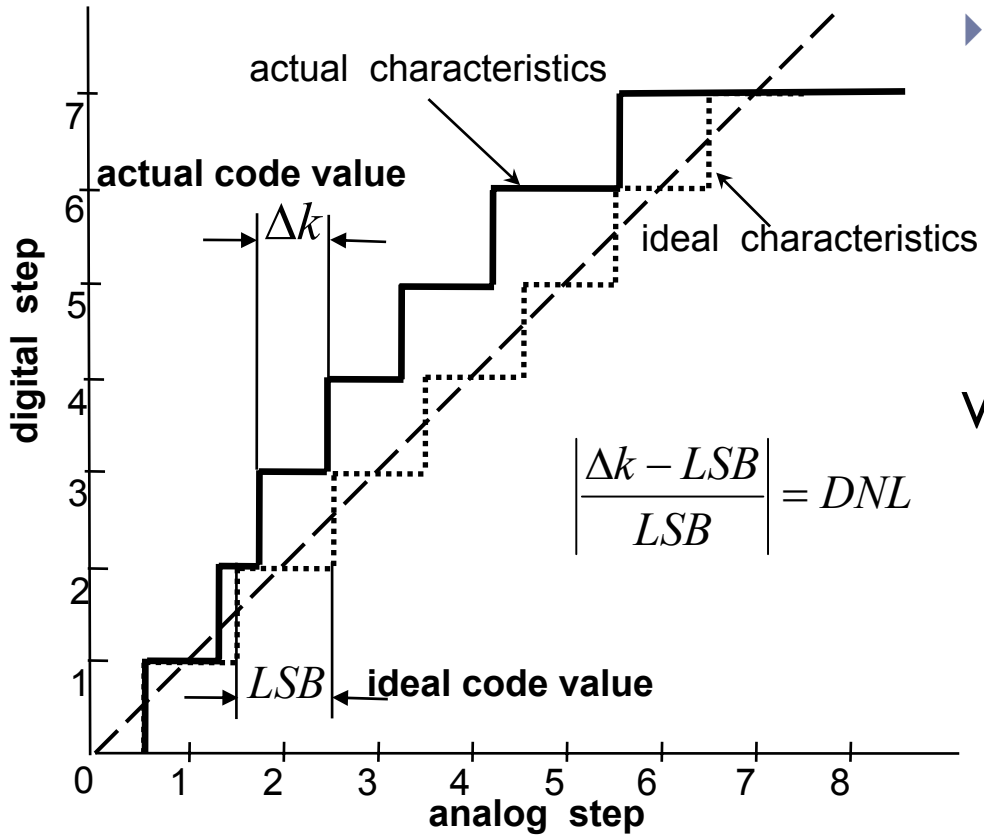


Fig. DNL in 3-bit D-A

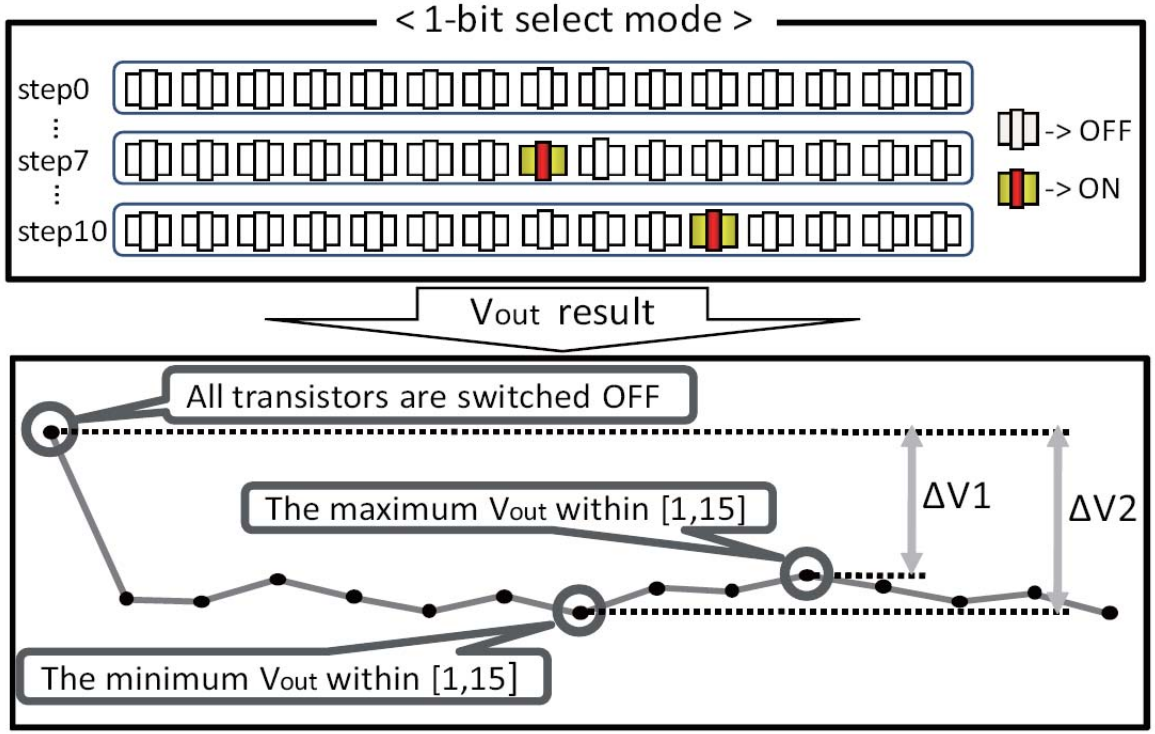
- DNL(Differential Non Linearity)
  - performance parameter of a DAC
  - can capture relative error

We employ DNL as variation parameter

$$DNL = \max \frac{|\Delta(k) - LSB|}{LSB}$$

--Relative Variation

- Evaluating relative variation based on 1-bit mode



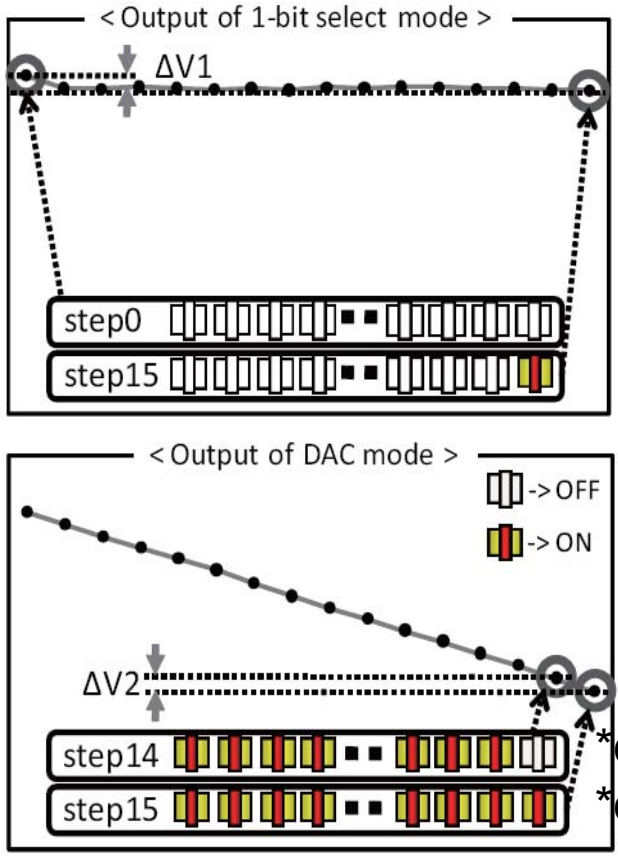
$$DNL1 = \frac{|\Delta V1 - LSB|}{LSB}$$

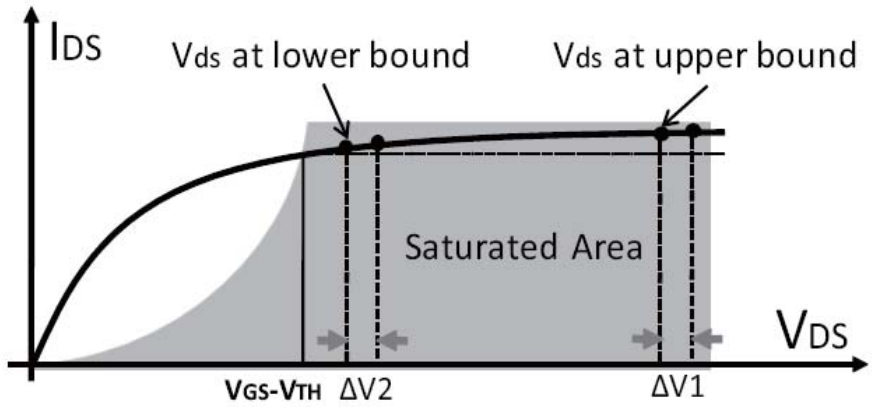
$$DNL2 = \frac{|\Delta V2 - LSB|}{LSB}$$

$$(Relative \quad Variation) = |DNL1 - DNL2|$$

-- λ-Dependent Variation

- A large λ worsens DC characteristics of a Tr in saturation area.
- Evaluating λ based on 1-bit and accumulating mode.





$$DNL1 = \frac{|\Delta V1 - LSB|}{LSB} \qquad DNL2 = \frac{|\Delta V2 - LSB|}{LSB}$$

$$*on\,(\lambda - Dependent \quad Variation) = |DNL1 - DNL2|$$

*off

--8 Layout Structures of CS

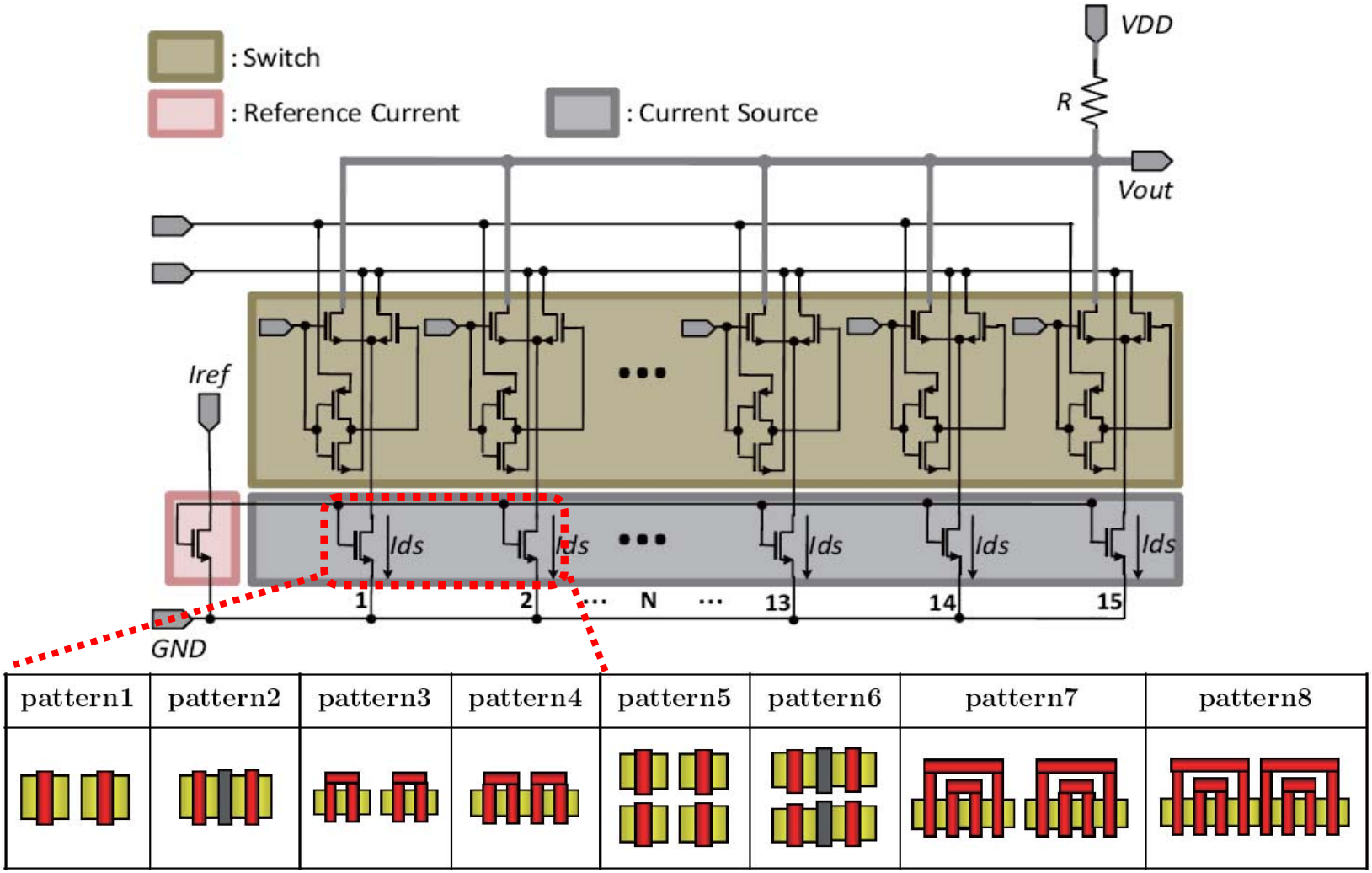


Fig. 8 layout structures of current source transistors

Analysis of Layout Structure Dependent Variation

--Discussion of the Analysis Results

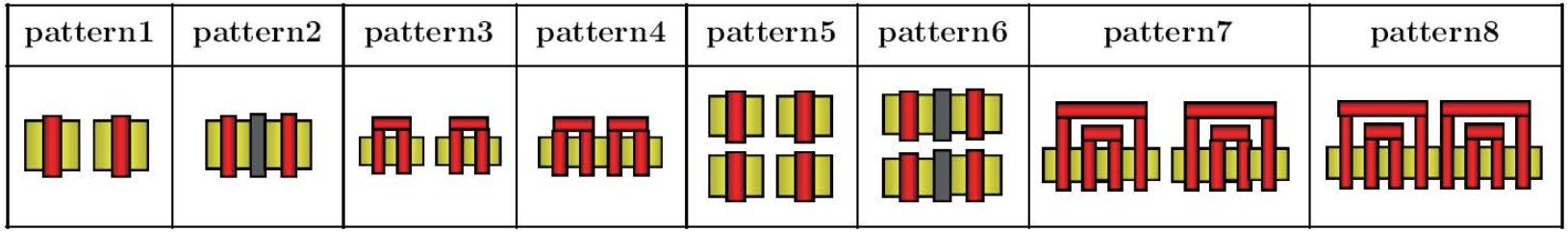


Fig. 8 layout structures of current source transistors

TABLE I. Comprehensive Results of (1)Relative-Variation (2) λ -Dependent-Variation

	(L, W)	pattern1	pattern2	pattern3	pattern4	pattern5	pattern6	pattern7	pattern8
(1)	ave(%)	1	+15.2%	-1.4%	+8.9%	-22.4%	+9.9%	-1.9%	+23.6%
(2)	ave(%)	1	+16.0%	+4.5%	+19.2%	+49.1%	+16.3%	+55.4%	+7.8%

[I] Comparison of patterns with/without **diffusion-sharing**:

(1) Without diffusion-sharing(pattern1, 3, 5, 7) becomes predominant to **relative-variation** .

(2) Pattern1 and 3 have better capability to suppress **λ -dependent-variation**.

[II] Comparison of patterns with/without **gate-folding** (to non-cascode pattern1-4):

(1) Pattern 3 and 4 have better **relative accuracy** than without gate-folding structure.

(2) Pattern 1 and 2 have better capability to suppress **λ -dependent-variation**.

Analysis of Layout Structure Dependent Variation

--Discussion of the Analysis Results

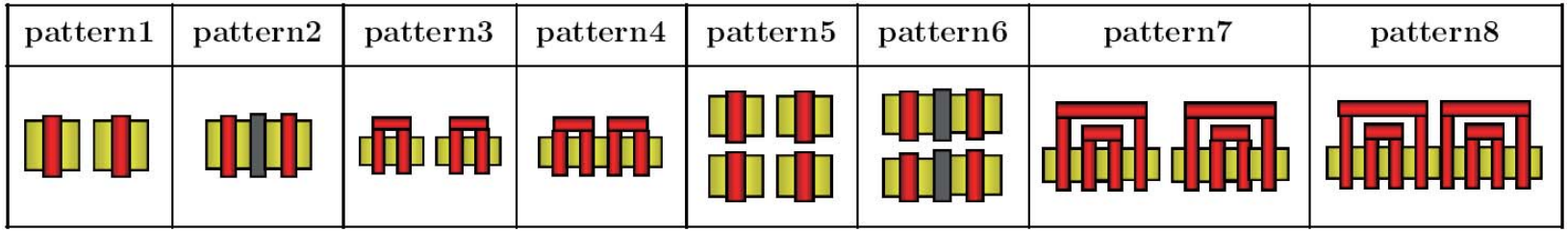


Fig. 8 layout structures of current source transistors

TABLE I. Comprehensive Results of (1)Relative-Variation (2) λ -Dependent-Variation

	(L, W)	pattern1	pattern2	pattern3	pattern4	pattern5	pattern6	pattern7	pattern8
(1)	ave(%)	1	+15.2%	-1.4%	+8.9%	-22.4%	+9.9%	-1.9%	+23.6%
(2)	ave(%)	1	+16.0%	+4.5%	+19.2%	+49.1%	+16.3%	+55.4%	+7.8%

[I] Comparison of patterns with/without **diffusion-sharing**:

(1) Without diffusion-sharing(pattern1, 3, 5, 7) becomes predominant to **relative-variation** .

(2) Pattern1 and 3 have better capability to suppress **λ -dependent-variation**.

[II] Comparison of patterns with/without **gate-folding** (to non-cascode pattern1-4):

(1) Pattern 3 and 4 have better **relative accuracy** than without gate-folding structure.

(2) Pattern 1 and 2 have better capability to suppress **λ -dependent-variation**.

Analysis of Layout Structure Dependent Variation

--Discussion of the Analysis Results

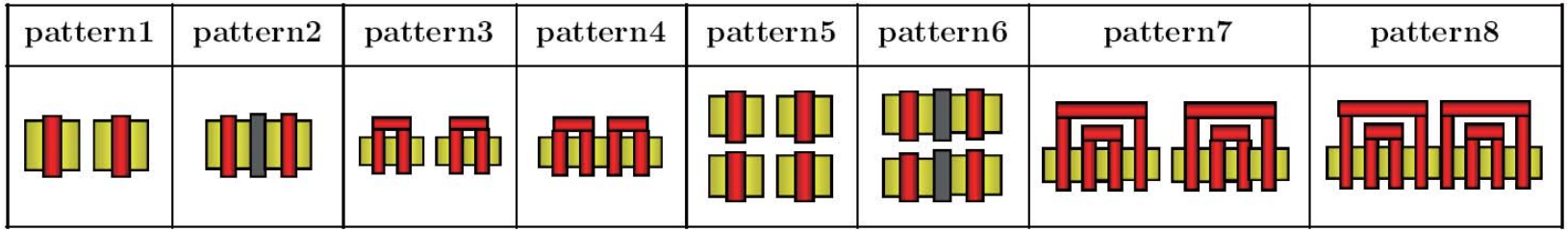


Fig. 8 layout structures of current source transistors

TABLE I. Comprehensive Results of (1)Relative-Variation (2) λ -Dependent-Variation

	(L, W)	pattern1	pattern2	pattern3	pattern4	pattern5	pattern6	pattern7	pattern8
(1)	ave(%)	1	+15.2%	-1.4%	+8.9%	-22.4%	+9.9%	-1.9%	+23.6%
(2)	ave(%)	1	+16.0%	+4.5%	+19.2%	+49.1%	+16.3%	+55.4%	+7.8%

[I] Comparison of patterns with/without **diffusion-sharing**:

(1) Without diffusion-sharing(pattern1, 3, 5, 7) becomes predominant to **relative-variation** .

(2) Pattern1 and 3 have better capability to suppress **λ -dependent-variation**.

[II] Comparison of patterns with/without **gate-folding** (to non-cascode pattern1-4):

(1) Pattern 3 and 4 have better **relative accuracy** than without gate-folding structure.

(2) Pattern 1 and 2 have better capability to suppress **λ -dependent-variation**.

Analysis of Layout Structure Dependent Variation

--Discussion of the Analysis Results

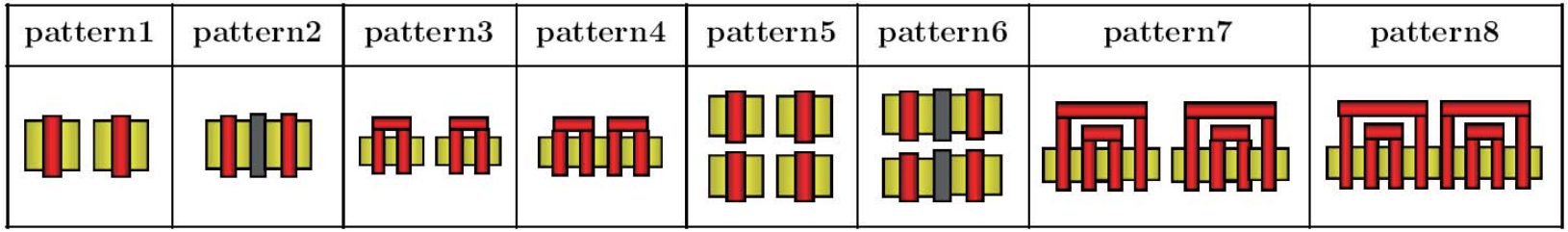


Fig. 8 layout structures of current source transistors

TABLE I. Comprehensive Results of (1)Relative-Variation (2) λ -Dependent-Variation

	(L, W)	pattern1	pattern2	pattern3	pattern4	pattern5	pattern6	pattern7	pattern8
(1)	ave(%)	1	+15.2%	-1.4%	+8.9%	-22.4%	+9.9%	-1.9%	+23.6%
(2)	ave(%)	1	+16.0%	+4.5%	+19.2%	+49.1%	+16.3%	+55.4%	+7.8%

[I] Comparison of patterns with/without **diffusion-sharing**:

(1) Without diffusion-sharing(pattern1, 3, 5, 7) becomes predominant to **relative-variation** .

(2) Pattern1 and 3 have better capability to suppress **λ -dependent-variation**.

[II] Comparison of patterns with/without **gate-folding** (to non-cascode pattern1-4):

(1) Pattern 3 and 4 have better **relative accuracy** than without gate-folding structure.

(2) Pattern 1 and 2 have better capability to suppress **λ -dependent-variation**.

--Trade-off Between Variation and Area Efficiency

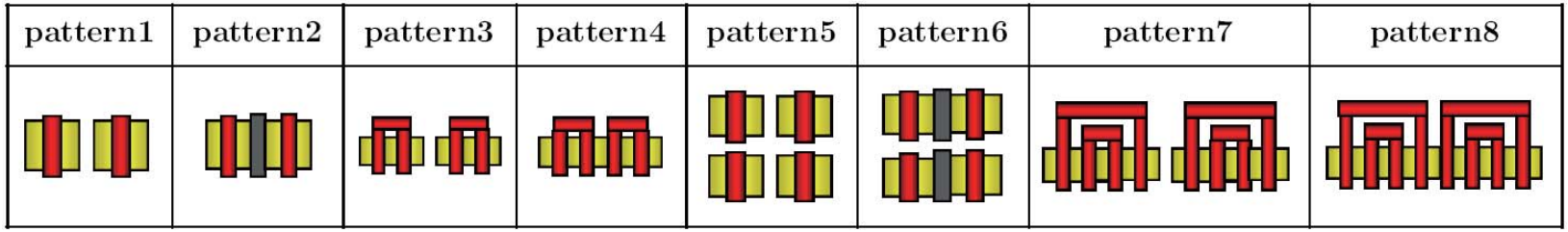


Fig. 8 layout structures of current source transistors

TABLE II. Comprehensive Results of (1)Relative-Variation (2) λ -Dependent-Variation (3)Layout Area

	(L, W)	pattern1	pattern2	pattern3	pattern4	pattern5	pattern6	pattern7	pattern8
(1)	ave(%)	1	+15.2%	-1.4%	+8.9%	-22.4%	+9.9%	-1.9%	+23.6% *1
(2)	ave(%)	1	+16.0%	+4.5%	+19.2%	+49.1%	+16.3%	+55.4%	+7.8%
(3)	ave(%)	1	+4.2%	+2.7%	-23.9% *2	+85%	+64.9%	+84.3%	+18.2%

Guideline

Non-cascode structure(pattern1, 2, 3, 4):

- good variation relevance : Pattern 1
- good area efficiency : Pattern 4

Cascode structure(pattern5, 6, 7, 8):

- good relative accuracy : Pattern 5
- good λ characteristic + area efficiency : Pattern 8

***1, *2 : 2 mistaken data in TABLE I and TABLE III of paper**

Conclusion

- We presented a new methodology to evaluate layout-dependent variation.
- We implemented 112 DACs into a TEG chip along with 8 layout-structures of the CS transistors to collect variation data.
- We evaluated and analyzed the layout-structure-dependency of relative-variation and λ -dependent-variation.

As the result, we ..

1) **observed the layout-structure-dependent variations with respect to the diffusion-sharing and gate-folding.**
2) **showed a guideline to meet the analog design requirement by making choice of variant layout-structure.**