D-A Converter Based Variation Analysis for Analog Layout Design

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Introduction

CS (current source) is an essential function in analog circuit. **Task:** its characteristic variation degrades the accuracy performance.

- propose a new evaluation methodology for analyzing the variation of CS transistor.
- implement 112-kind current-driven DACs to investigate the dependency of CS upon the relative accuracy and $\lambda$.
- evaluate and analyze the layout-dependent variation

we do..

- diffusion-sharing and gate-folding significantly influence to the variation of $\lambda$ and relative accuracy.
Evaluation Methodology

-- 4-bit current-driven DAC

\[ V_{out} = VDD - N_{on} \times I_{ds} \times R \]

- \( V_{out} \): the number of CS transistors switched on
- \( N_{on} \): the current value from drain to source
Evaluation Methodology

-- Operating modes of DAC

- Our DACs operate in 2 modes by control signals.
  - Accumulating mode: accumulating CS transistor switched on in (a).
  - 1-bit mode: just one CS transistor turns on in (b).

Fig. Operating modes of a 4-bit DAC
Evaluation Methodology

--Variation Definition based on DNL

- DNL (Differential Non Linearity)
  - performance parameter of a DAC
  - can capture relative error

We employ DNL as variation parameter

\[
DNL = \max \left| \frac{\Delta(k) - LSB}{LSB} \right|
\]

Fig. DNL in 3-bit D-A
Evaluation Methodology

--- Relative Variation

- Evaluating relative variation based on 1-bit mode

\[
\begin{align*}
DNL_1 &= \frac{|\Delta V_1 - LSB|}{LSB} \\
DNL_2 &= \frac{|\Delta V_2 - LSB|}{LSB}
\end{align*}
\]

\[
(Relative Variation) = |DNL_1 - DNL_2|
\]
Evaluation Methodology

-- $\lambda$-Dependent Variation

- A large $\lambda$ worsens DC characteristics of a Tr in saturation area.
- Evaluating $\lambda$ based on 1-bit and accumulating mode.

$$DNL1 = \frac{|\Delta V1 - LSB|}{LSB} \quad DNL2 = \frac{|\Delta V2 - LSB|}{LSB}$$

$$(\lambda - \text{Dependent Variation}) = |DNL1 - DNL2|$$
Analysis of Layout Structure Dependent Variation

-- 8 Layout Structures of CS

Fig. 8 layout structures of current source transistors
Analysis of Layout Structure Dependent Variation

--Discussion of the Analysis Results

Fig. 8 layout structures of current source transistors

<table>
<thead>
<tr>
<th>pattern1</th>
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TABLE I. Comprehensive Results of (1) Relative-Variation (2) $\lambda$-Dependent-Variation

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<tbody>
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<td>(1) ave(%)</td>
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[Ⅰ] Comparison of patterns with/without **diffusion-sharing**:  
(1) Without diffusion-sharing (pattern1, 3, 5, 7) becomes predominant to relative-variation .  
(2) Pattern1 and 3 have better capability to suppress $\lambda$-dependent-variation.

[Ⅱ] Comparison of patterns with/without **gate-folding** (to non-cascode pattern1-4):  
(1) Pattern 3 and 4 have better relative accuracy than without gate-folding structure.  
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Analysis of Layout Structure Dependent Variation

--Discussion of the Analysis Results

![Fig. 8 layout structures of current source transistors](image)

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**TABLE I. Comprehensive Results of** (1) Relative-Variation (2) λ -Dependent-

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![Fig. 8 layout structures of current source transistors](image)

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Analysis of Layout Structure Dependent Variation

---Trade-off Between Variation and Area Efficiency

Cascode structure (pattern 5, 6, 7, 8):
- good relative accuracy: Pattern 5
- good λ characteristic + area efficiency: Pattern 8

Non-cascode structure (pattern 1, 2, 3, 4):
- good variation relevance: Pattern 1
- good area efficiency: Pattern 4

*1, *2: 2 mistaken data in TABLE I and TABLE III of paper

### TABLE II. Comprehensive Results of (1) Relative-Variation (2) λ-Dependent-Variation (3) Layout Area

<table>
<thead>
<tr>
<th>Pattern</th>
<th>(L, W)</th>
<th>Pattern1</th>
<th>Pattern2</th>
<th>Pattern3</th>
<th>Pattern4</th>
<th>Pattern5</th>
<th>Pattern6</th>
<th>Pattern7</th>
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</tr>
</thead>
<tbody>
<tr>
<td>Ave(%)</td>
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<td>Ave(%)</td>
<td>Ave(%)</td>
<td>Ave(%)</td>
<td>Ave(%)</td>
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<td>Ave(%)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>+15.2%</td>
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<td></td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>+16.0%</td>
<td>+4.5%</td>
<td>+19.2%</td>
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<td>+7.8%</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>+4.2%</td>
<td>+2.7%</td>
<td>-23.9%</td>
<td>+85%</td>
<td>+64.9%</td>
<td>+84.3%</td>
<td>+18.2%</td>
<td></td>
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</table>

Guideline

Fig. 8 layout structures of current source transistors

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Conclusion

We presented a new methodology to evaluate layout-dependent variation.

We implemented 112 DACs into a TEG chip along with 8 layout-structures of the CS transistors to collect variation data.

We evaluated and analyzed the layout-structure-dependency of relative-variation and $\lambda$-dependent-variation.

As the result, we..

1) observed the layout-structure-dependent variations with respect to the diffusion-sharing and gate-folding.

2) showed a guideline to meet the analog design requirement by making choice of variant layout-structure.