On-Chip Power Network Optimization with Decoupling Capacitors and Controlled-ESRs

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Outline of Optimization with Decap and Controlled-ESR

- Introduction
  - Existing works add decap to reduce noise
  - Controlled-ESR is shown to be effective to suppress the resonance
- Power network model with controlled-ESR
- Problem statement
  - Power network noise considering overshoot
  - Formulation
- Revised sensitivity computation
  - Sensitivity computation with merged adjoint network
  - Revised sensitivity computation considering voltage overshoot
- SQP based optimization
- Experimental results
- Conclusions

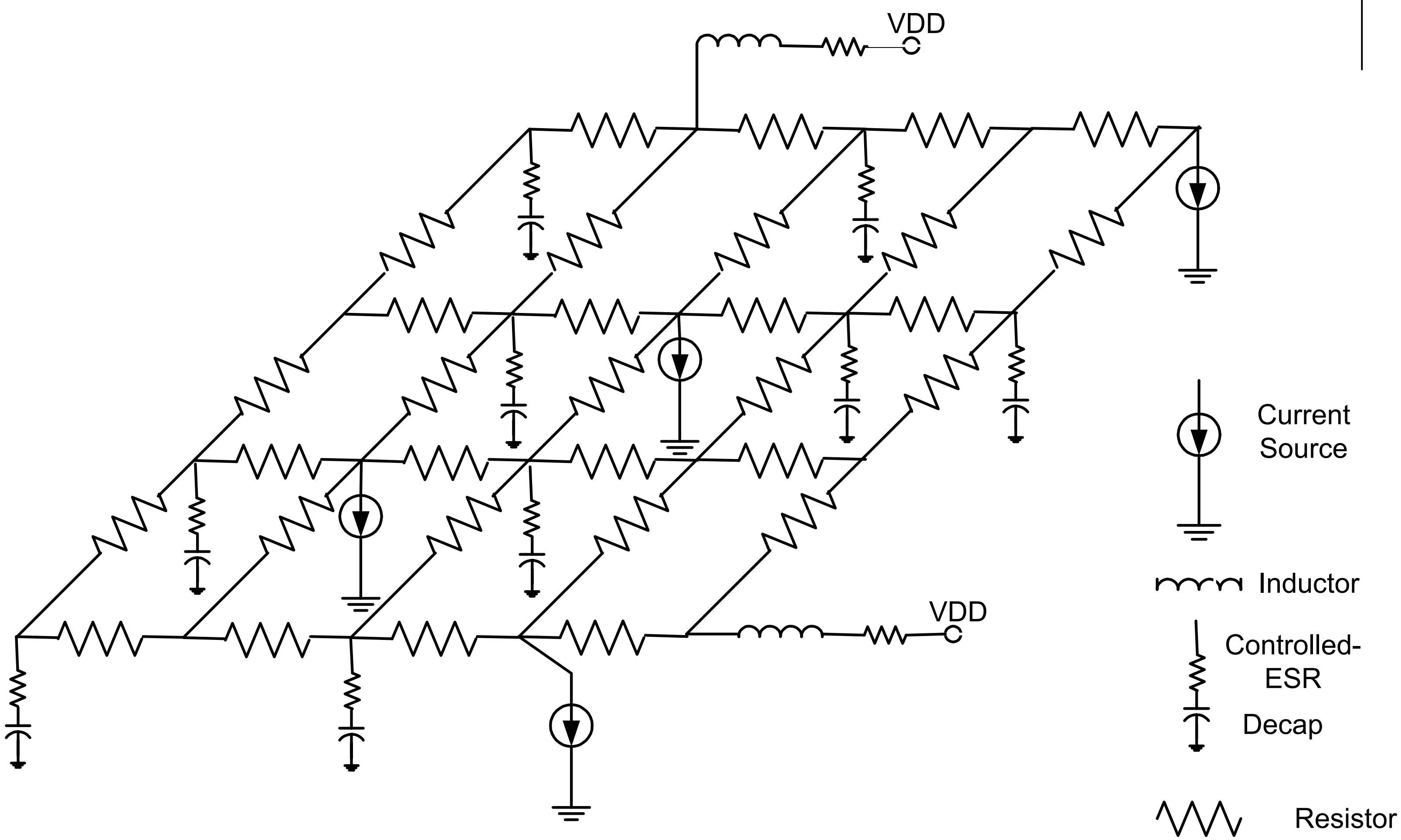
Our Contributions

- We propose to allocate decaps and controlled-ESRs simultaneously to suppress the resonance and reduce SSN of power network.

- We consider both voltage drop and overshoot for voltage violation. Derive revised sensitivity.

- An optimization formulation with the objective function of minimizing the voltage violation area and a constraint of decap budget is presented, and solved with an efficient SQP algorithm.

Power Network Model with Controlled-ESR



Voltage Variation Analysis with Circuit State Equation

From KCL and KVL, we have the circuit state equation:

$$\begin{bmatrix} C & 0 \\ 0 & L \end{bmatrix}\begin{bmatrix} \dot{v} \\ \dot{i} \end{bmatrix} = \begin{bmatrix} -G & -E \\ E^T & -R \end{bmatrix}\begin{bmatrix} v \\ i \end{bmatrix} + BU \quad (1)$$

which is denoted to be:

$$C\dot{x} = Ax + Bu \quad (2)$$

If add extra decap ⊿*C* and controlled-ESR ⊿*A*, solution *x* will be updated by ⊿*x*, so (2) becomes:

$$(C+\Delta C)(\dot{x}+\Delta\dot{x}) = (A+\Delta A)(x+\Delta x) + Bu \quad (3)$$

By subtracting (2) from (3):

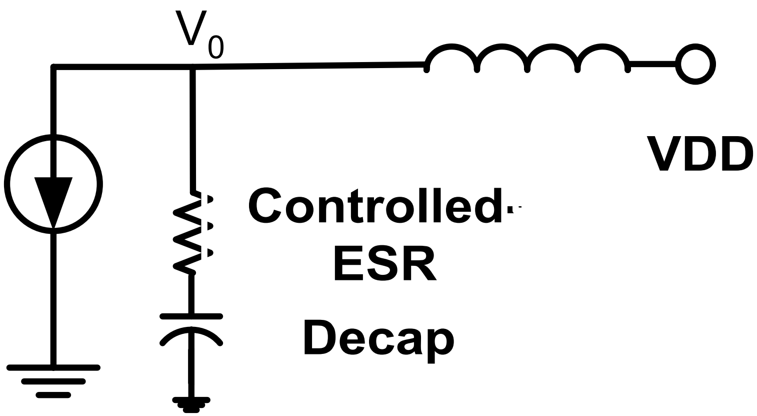
$$(C+\Delta C)\Delta\dot{x} = (A+\Delta A)\Delta x + (\Delta A x - \Delta C\dot{x}) \quad (4)$$

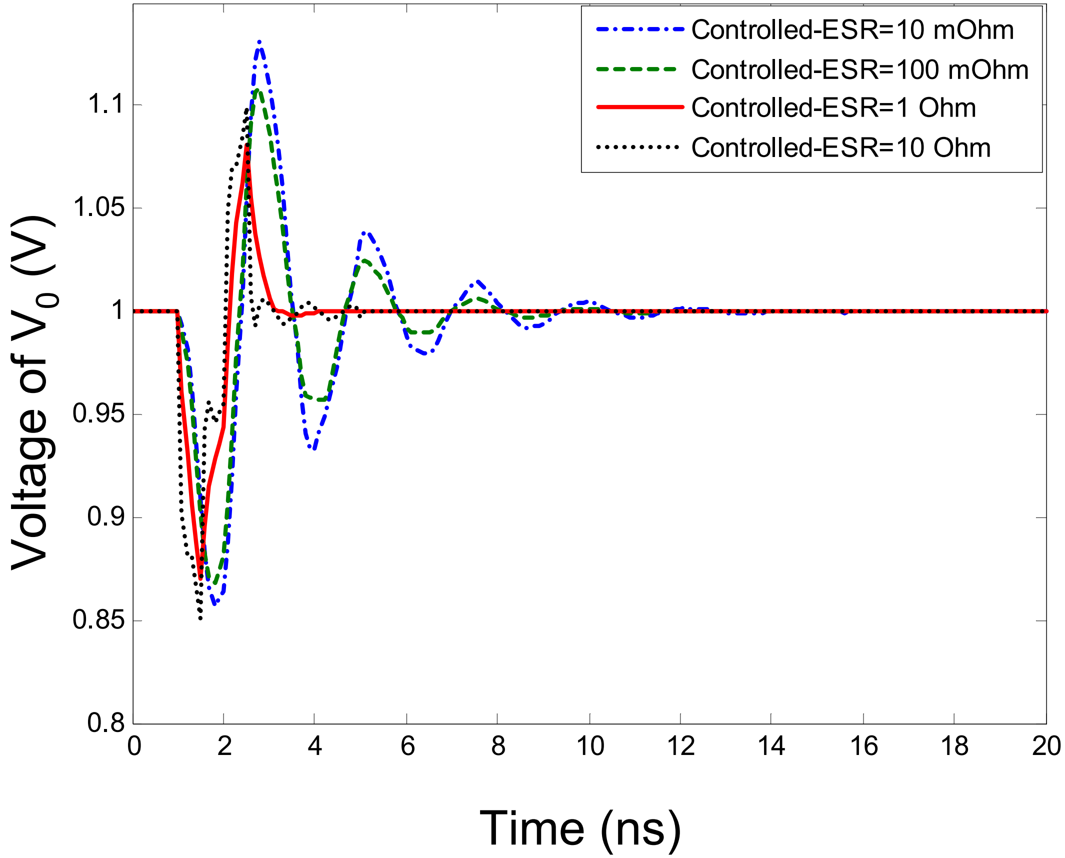
The solution of (4) is:

$$\Delta x = e^{\tilde{C}^{-1}\tilde{A}(t-t_0)}\Delta x_0 + \int_{t_0}^{t} e^{\tilde{C}^{-1}\tilde{A}(t-\tau)}\tilde{C}^{-1}\tilde{U}(\tau)d\tau \quad (5)$$

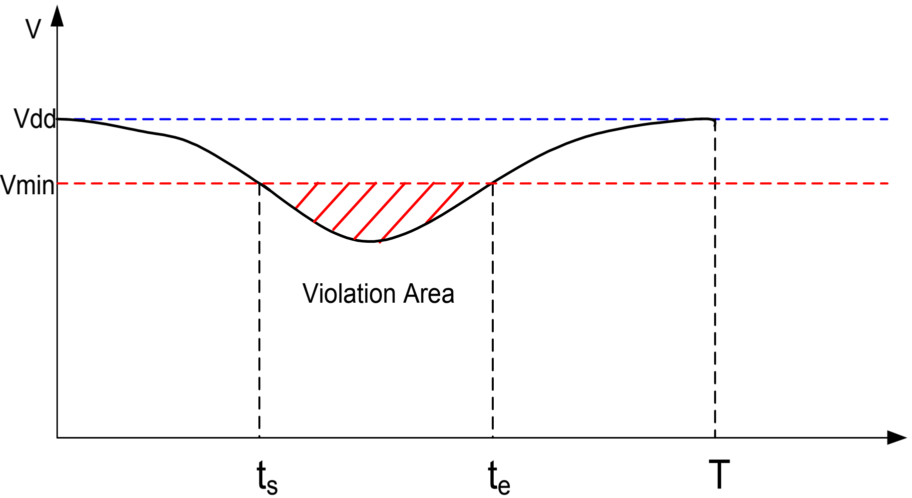
where: $\tilde{C} \equiv C + \Delta C,\ \ \tilde{A} \equiv A + \Delta A,\ \ \tilde{U} \equiv \Delta A x - \Delta C\dot{x} \qquad e^{\tilde{A}} \equiv I + \tilde{A} + \frac{\tilde{A}^2}{2!} + \frac{\tilde{A}^3}{3!} + \ldots$

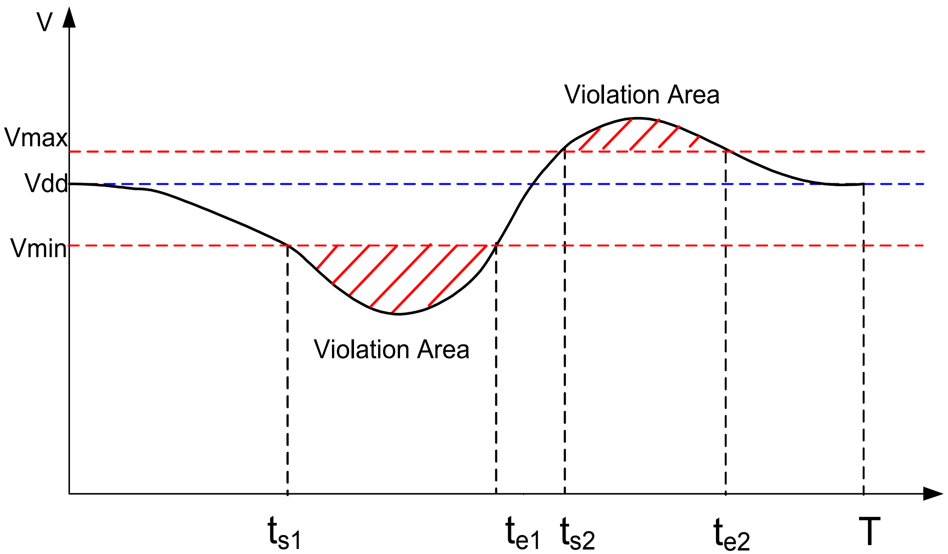
Effect of Controlled-ESR on reducing the noise





Power Network Noise Considering Overshoot





$$g_j = \int_0^T \max(V_{\min} - v_j(t),\ 0)\,dt$$

$$g_j = \int_0^T \max[\max(V_{\min} - v_j(t),\ 0),\ \max(v_j(t) - V_{\max},\ 0)]\,dt$$

Problem Formulation

- Objective function:
  - Min $\sum_{j=1}^{N} g_j$
- Constraints:
  - (1) Voltage response satisfies the circuit equation with given stimulus;
  - (2) Total decap budget: $\sum_{i=1}^{M} c_i \leq Q$
  - (3) Space constraint for each decap location: $0 \leq c_i \leq c_{\max i}$
  - (4) Space constraint for each controlled-ESR location:

$$0 \leq CtrlESR_i \leq CtrlESR_{\max i}$$

Sensitivity Computation with Merged Adjoint Network

The sensitivity s_{ij} is defined to be the contribution of decap added at node *i* to remove violation at node *j*:

$$s_{ij} = \frac{\partial g_j}{\partial c_i}$$

The merged adjoint sensitivity is defined to be the contribution of decap added at node *i* to remove the violation for all nodes.

The merged adjoint network has a current source $u(t - t_s) - u(t - t_e)$ applied at every node *j*

Merged adjoint sensitivity is calculated with

$$s_i = \sum_{j=1}^{N} s_{ij} = \int_0^T (\tilde{v}_{i,all}(T - t)) \times \dot{v}_i(t)\,dt, \; (i = 1, 2, \ldots, M)$$

Revised Sensitivity Computation Considering Overshoot

We denote the port currents and voltages by vectors I_p and V_p. Denote the non-source branch currents and voltages by vectors I_b and V_b. From Tellegen's theorem, we have

$$\int_0^T [-\hat{i}_p(\tau)\Delta v_p(t) + \hat{v}_p(\tau)\Delta i_p(t)]_{\tau=T-t} dt$$

$$= \int_0^T [\hat{i}_b(\tau)\Delta v_b(t) + \hat{v}_b(\tau)\Delta i_b(t)]_{\tau=T-t} dt$$

We set all voltage sources in the adjoint network to zero and apply a current source for each violation node:

$$I_s = \sum_{k=1}^{N_v} D_k [u(t-t_{sk}) - u(t-t_{ek})]$$

$$D_k = \begin{cases} -1, & \text{if } v(t_{sk}) > \mathrm{Vdd} \\ 1, & \text{if } v(t_{sk}) < \mathrm{Vdd} \end{cases}$$

Left hand:

$$\Delta g = \int_0^T \left\{ -\sum_{k=1}^{N_v} D_k [u(t-t_{sk}) - u(t-t_{ek})] \Delta v_p(t) \right\}_{\tau=T-t} dt$$

Right hand:

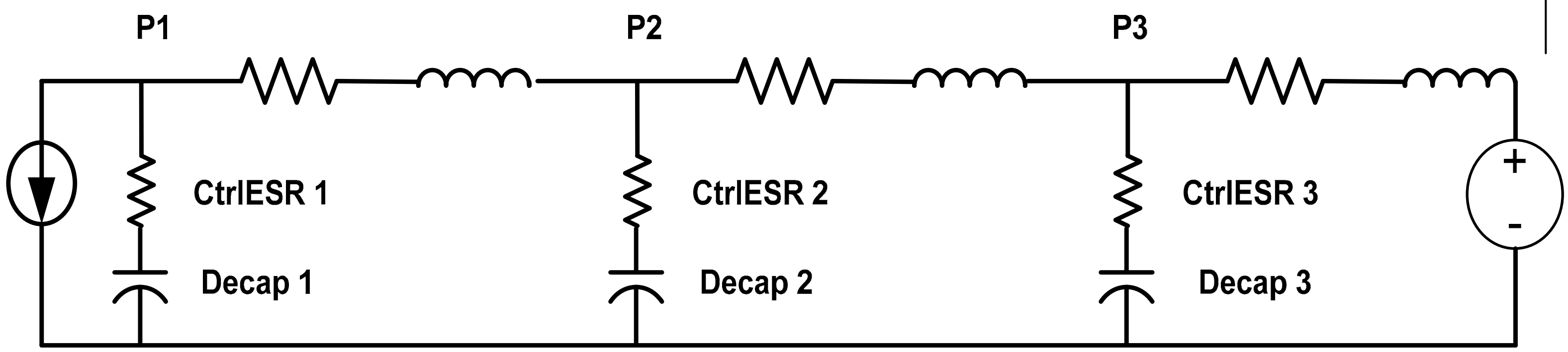
$$s_C = \frac{\Delta g}{\Delta C} = \int_0^T -[\hat{v}_c(\tau)\dot{v}_c(t)]_{\tau=T-t} dt \qquad s_R = \frac{\Delta g}{\Delta R} = \int_0^T [\hat{i}_R(\tau) i_R(t)]_{\tau=T-t} dt$$

SQP Based Optimization

Algorithm for the SQP based optimization:

1. Select the intrinsic capacitance and controlled-ESR to be the initial solution $X^{(0)}$.
2. Simulate the power network circuit, and compute the sensitivity as gradient using the revised method.
3. Use the gradient to approximate the problem with a linearly constrained QP subproblem at $X^{(t)}$.
4. Solve for the step size $d^{(t)}$ to move.
5. If meet with termination condition, stop;
   Else, let $X^{(t+1)} = X^{(t)} + d^{(t)}$.
6. Increase t and return to step 2.

A Simple Case



- Initial values:
  - R = 1 ohm and L=1 nH. Decap=0.01 nF, controlled-ESR = 1.0e-4 ohm.
  - *Vdd* is 1V, and the allowable voltage drop is 0.05V.
- Constraints:
  - Maximum allowable decap at each node to be 0.1 nF,
  - Total decap should not exceed 0.2 nF,
  - Maximum allowable controlled-ESR at each node is 0.2 Ohm
- Without optimization: The overall noise is 193.7 V*ps.
- Optimize with decap only:
  - Decap at each node are: 0.1 nF, 0.09 nF, and 0.01 nF.
  - The noise after optimization is 6.3 V*ps.
- Optimize with both decap and controlled-ESR:
  - Controlled-ESR values at each node are: 0.2 Ohm, 2.77e-2 Ohm, and 1.0e-4 Ohm.
  - The noise is further reduced to be 5.3 V*ps.
  - The controlled-ESR improves the noise by 15.9%.

Experimental Results

Table I. Effect of considering voltage overshoot

Circuit	# Node	Consider voltage drop only		Consider both voltage drop and overshoot		Noise underestimation due to neglecting overshoot
		Noise (V*ps)	# Violation node	Noise (V*ps)	# Violation node	
CKT1	858	306.7	46	324.8	46	5.6%
CKT2	1794	7406.3	325	8127.8	347	8.9%
CKT3	2006	5111.3	309	5324.9	309	4.0%
CKT4	3634	9770.1	268	10049.6	268	2.8%
CKT5	8330	5608.1	2470	5829.1	2470	4.0%
CKT6	14852	31420.8	2243	32477.3	2243	3.4%

- The noise is the voltage violation area and the number of violation nodes.
- Total noise is on average underestimated by 4.8% due to neglecting the voltage overshoot.
- The number of violation nodes is almost the same for both cases.

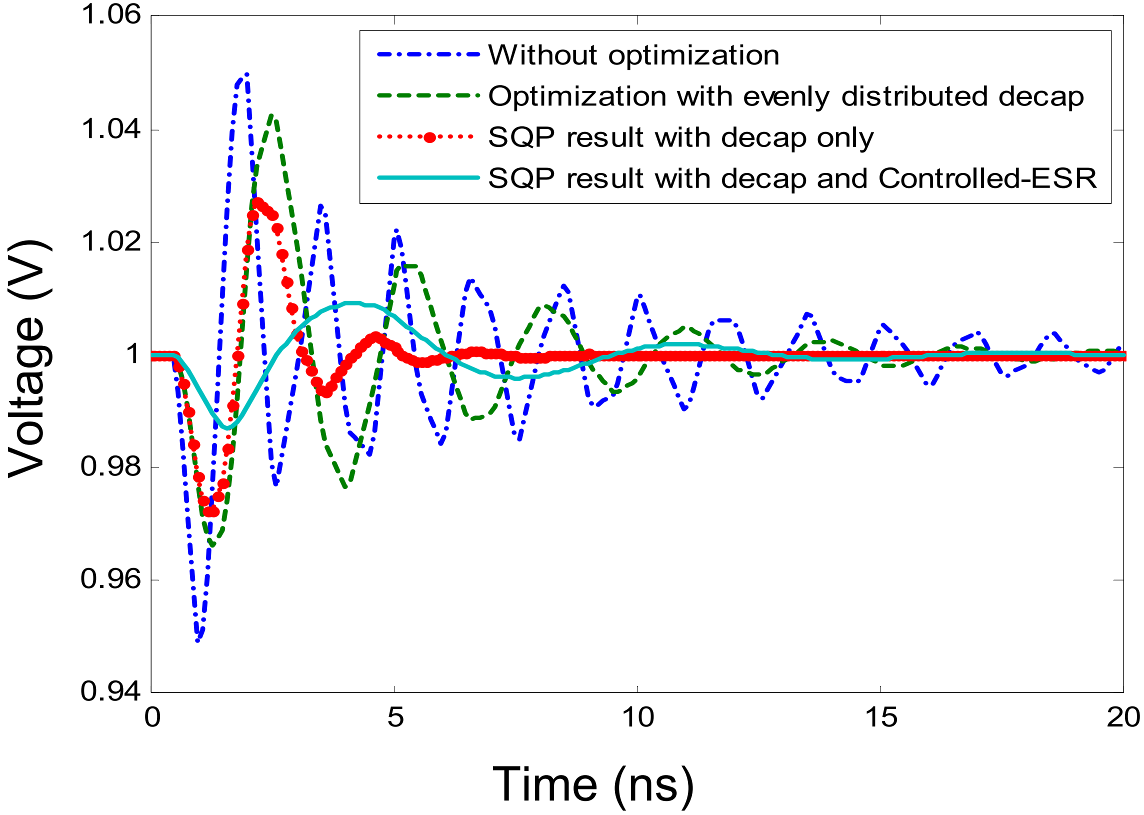
Experimental Results

Table II. Comparison among three methods for the minimization of power network noise

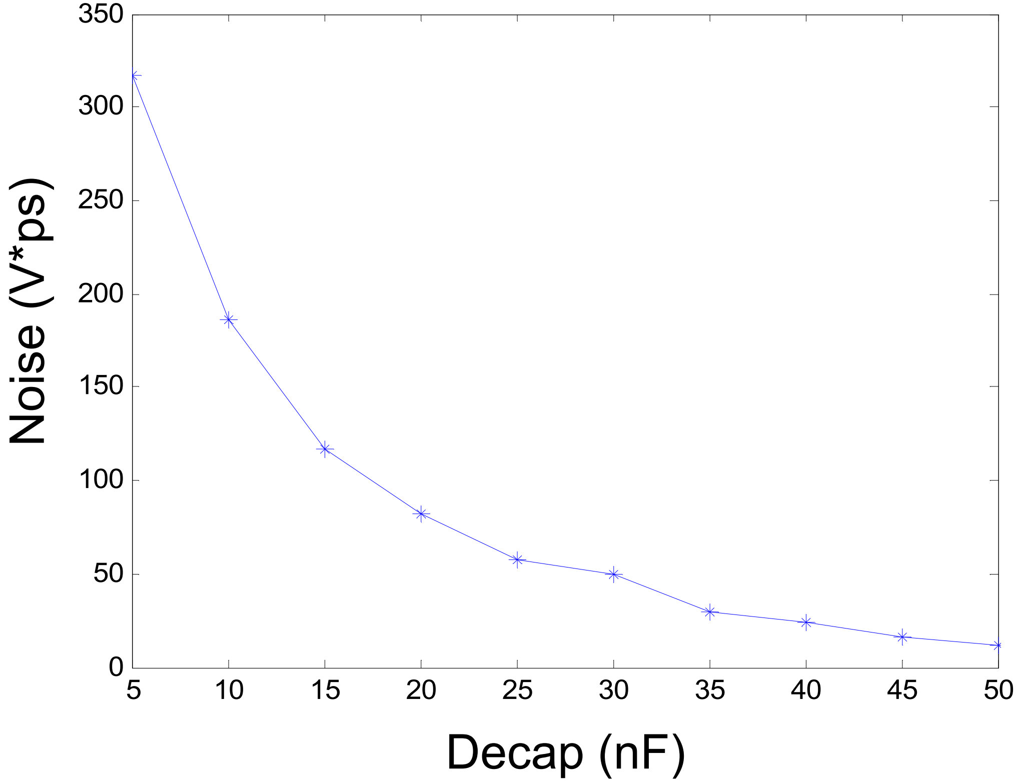
Circuit	Evenly allocate the decaps		Allocate decaps only with the SQP-based method		Allocate both decaps and controlled-ESRs with the SQP-based method			
	Noise (V*ps)	# Violation node	Noise (V*ps)	# Violation node	Noise (V*ps)	# Violation node	CPU time (s)	Noise reduction compared to allocating decaps only
CKT1	229.5	20	113.4	23	82.1	16	26.2	27.6%
CKT2	6137.1	156	2538.0	104	2023.4	47	172.8	20.3%
CKT3	4597.9	141	2308.3	88	2077.2	78	116.7	10.0%
CKT4	8939.0	235	2212.5	96	1527.0	47	141.6	30.8%
CKT5	5352.3	1245	1694.3	617	1073.0	333	1195.2	36.7%
CKT6	26916.9	1191	6538.1	390	4853.6	204	2564.1	25.8%

- The noise (column 2, 4, 6) and the number of violation nodes (column 3, 5, 7) are reduced.
- The improvement brought by considering the controlled-ESRs is 25% on average.
- With the third method, the average allocated controlled-ESR ranges from 0.038 Ohm to 0.083 Ohm for different cases.

Voltage Waveforms with Different Optimizations



Relationship between Decap Budget and Noise



- Larger decap budget leads to smaller noise
- Tradeoff between the noise reduction and the decap investment

Conclusions

- Optimize power network with both decap and controlled-ESR.
- Revised sensitivity computation considering voltage overshoot.
- SQP based optimization

Thank You!

Q & A