Power and Slew-aware Clock Network Design for Through-Silicon-Via (TSV) based 3D ICs

Xin Zhao and Sung Kyu Lim
School of Electrical and Computer Engineering
Georgia Institute of Technology
Atlanta, Georgia, U.S.A.
Outline

• Introduction

• Problem formulation

• 3D clock tree synthesis

• Simulation and discussions

• Conclusions
Related works

• Through-silicon-via (TSV)
  – Fabrication and characterization
  – Reliability issues [Ramm, etc. ECTC’08] [Wright, etc. ECTC’08]…

• Low-power 3D clock network
  – A fabricated 3D clock distribution network [Pavlidis, etc. CICC’08]
  – A separate layer of clock distribution network for power reduction
    [Arunachalam, etc. VLSI’08]

• 3D clock network design and optimization
  – Thermal-aware 3D clock design, 3D clock routing algorithm [Minz, etc. ASPDAC’08]
  – Pre-bond testable 3D clock synthesis [Zhao, etc. ICCAD’09]
Contributions

• The major goals
  – Clock skew minimization
  – Clock slew control
  – Clock power reduction

• Investigate the impact of design techniques on 3D clock network
Electrical model and TSV usage

• Electrical model
  – Wire
  – TSV
  – Clock buffer

• TSV upper bound
  – Maximum number of TSVs allowed between adjacent dies

• TSV count (#TSVs)
  – Total number of TSVs used in 3D tree
  – Stacked-TSV
Problem formulation: 3D clock tree synthesis

- **Input**
  - Sink set (N dies), clock source location
  - Upper bound of TSV usage
  - Slew constraint

- **Output**
  - Zero-Elmore-skew 3D clock tree

- **Object**
  - Zero-Elmore-skew
  - Minimize wirelength, clock power

- **Constraint**
  - Maximum slew
  - Upper bound of TSV usage
3D clock tree design flow

- **Input:**
  - a set a sinks on N die
  - Upper bound of TSV

Upper bound of TSV = 3, clock source locates on die-0
3D clock tree design flow (cont.)

- Step-1:
  - Recursive top-down partition
  - 3D Method of Means and Medians (3D-MMM)
  - 3D abstract binary-tree generation
3D clock tree design flow (cont.)

• Step-2:
  – Merging and slew-aware buffering, embedding
  – 3D clock tree with multiple TSVs

• Unique property of 3D clock tree
  – A complete tree + many sub-trees
3D clock routing algorithm

1. Sinks of all dies, upper bound of TSVs, CMAX
2. 3D abstract tree generation (3D-MMM)
3. Slew-aware buffering, merging and embedding
4. A 3D clock network

3D clock tree synthesis
3D-MMM and 3D abstract tree

TSV=1

TSV=2

TSV=4

2D version

3D version

3D abstract tree
3D-MMM and 3D abstract tree (cont.)

- 3D abstract tree for the N-die stack
  - N-colored binary tree
  - Clock source location

Given three sinks

Clock src on die-3

Clock src on die-2

Clock src on die-1

3D abstract tree

3D clock tree
3D clock tree in multiple-die stack

- A complete tree + many sub-trees

Four-die 3D clock tree, src on die-4

Four-die 3D clock tree, src on die-3
Clock source location

- Clock source on middle die tends to reduce #TSVs and wirelength
- Theoretical maximum TSV usage:
  - $M$ sinks evenly distribute on $N$ dies, clock source locates on die-$s$

$$\frac{M}{N} \times \left( \sum_{i=1}^{s-1} (s - i) + \sum_{i=s+1}^{N} (i - s) \right)$$
Buffering and merging

- **Goal**
  - Slew control
    - Maximum loading capacitance (CMAX) of clock buffers
  - Wirelength reduction

- **Object**
  - Zero-Elmore skew
  - Clock power minimization
Detail experiment settings

- 45nm technology:
  - Frequency = 1GHz, $V_{dd} = 1.2V$
  - Clock slew < 10% of clock period (CMAX = 300fF)
  - Clock skew < 3%~4% of clock period
  - Wire: $R = 0.1 \ \Omega/\text{um}$, $C = 0.2 \ \text{fF/um}$
  - Buffer: $R_d = 122 \ \Omega$, $C_L = 24 \ \text{fF}$, $t_d = 17 \ \text{ps}$
  - TSV: $R_{TSV} = 0.035 \ \Omega$, $C_{TSV} = 15.48 \ \text{fF}$
    - 10 um X 10 um, via-last
    - Thinned-die height = 20 um

- Results are from SPICE simulation
  - Skew, slew, power

- We use two cases: four-die and six-die

<table>
<thead>
<tr>
<th>Circuits</th>
<th># Sinks</th>
</tr>
</thead>
<tbody>
<tr>
<td>r1</td>
<td>267</td>
</tr>
<tr>
<td>r2</td>
<td>598</td>
</tr>
<tr>
<td>r3</td>
<td>862</td>
</tr>
<tr>
<td>r4</td>
<td>1903</td>
</tr>
<tr>
<td>r5</td>
<td>3101</td>
</tr>
</tbody>
</table>
Sample 3D clock trees

r5, six-die

#TSVs = 20
Impact of TSV bound on wirelength and power

Point A: 20% power saving, TSV bound ≥ 70% of #sinks
Multi-TSV vs Single-TSV: four-die stack

![Graph showing normalized wirelength and power comparison between Single TSV, Bounded multi-TSV, and Relaxed multi-TSV across different rings r1 to r5.](image)

<table>
<thead>
<tr>
<th>Ring</th>
<th>#TSVs (Bnd)</th>
<th>#TSVs (Relax)</th>
</tr>
</thead>
<tbody>
<tr>
<td>r1</td>
<td>139</td>
<td>265</td>
</tr>
<tr>
<td>r2</td>
<td>309</td>
<td>579</td>
</tr>
<tr>
<td>r3</td>
<td>432</td>
<td>819</td>
</tr>
<tr>
<td>r4</td>
<td>1003</td>
<td>1893</td>
</tr>
<tr>
<td>r5</td>
<td>1631</td>
<td>3097</td>
</tr>
</tbody>
</table>
Multi-TSV vs Single-TSV: six-die stack

![Graph showing normalized wirelength and power comparisons between Single TSV, Bounded multi-TSV, and Relaxed multi-TSV across different scenarios.](image)

- **Normalized wirelength**
  - r1: Single TSV 1.0, Bounded multi-TSV 0.6, Relaxed multi-TSV 0.4
  - r2: Single TSV 1.0, Bounded multi-TSV 0.6, Relaxed multi-TSV 0.4
  - r3: Single TSV 1.0, Bounded multi-TSV 0.6, Relaxed multi-TSV 0.4
  - r4: Single TSV 1.0, Bounded multi-TSV 0.6, Relaxed multi-TSV 0.4
  - r5: Single TSV 1.0, Bounded multi-TSV 0.6, Relaxed multi-TSV 0.4

- **Normalized power**
  - r1: Single TSV 1.0, Bounded multi-TSV 0.8, Relaxed multi-TSV 0.6
  - r2: Single TSV 1.0, Bounded multi-TSV 0.8, Relaxed multi-TSV 0.6
  - r3: Single TSV 1.0, Bounded multi-TSV 0.8, Relaxed multi-TSV 0.6
  - r4: Single TSV 1.0, Bounded multi-TSV 0.8, Relaxed multi-TSV 0.6
  - r5: Single TSV 1.0, Bounded multi-TSV 0.8, Relaxed multi-TSV 0.6

### #TSVs (Bnd):
- r1: 222
- r2: 483
- r3: 701
- r4: 1594
- r5: 2588

### #TSVs (Relax):
- r1: 399
- r2: 908
- r3: 1301
- r4: 2980
- r5: 4782
Clock skew in four- and six- die stack

![Graph showing clock skew in four- and six- die stack. The graph compares clock skew for Single TSV, Bounded multi-TSV, and Relaxed multi-TSV in both four- and six-die stacks. The x-axis represents different rows (r1 to r5), and the y-axis represents clock skew (of clk period) in percentage. The graph indicates higher clock skew in the six-die stack compared to the four-die stack for all TSV configurations.]
Spatial distribution of clock delay

Delay (ns)

Skew
17.8 ps

r5, six-die
Impact of TSV bound on slew distribution

(a) Single TSV

- r5, six-die
- CMAX=300fF
- \([11.4\text{ps}, 86.2\text{ps}]\)
- Avg. 53.9ps
- #Bufs: 2933

(b) Multi-TSV

- \([10.9\text{ps}, 79.6\text{ps}]\)
- Avg. 42.6ps
- #Bufs: 2638
Impact of CMAX on slew variations

- Using single TSV
- Using multiple TSVs

r5, six-die
Impact of clock source location on power and wirelength

A uses 33% fewer TSVs than B

r5, six-die
Distribution of stacked-TSV heights

r5, six-die

#TSVs = 3720  #TSVs = 2791
Conclusions

• Explored design optimization techniques for reliable, low-power, low-slew 3D clock network design.

• Using multiple TSVs helps to reduce wirelength and power. Multi-TSV also has better control on slew variations.

• Smaller CMAX efficiently lowers the clock slew.

• Clock source location affects wirelength, power and TSV usage of the 3D clock network. Middle-die sourcing policy reduces the TSV usage under the same power budget.
Thank you