Power and Slew-aware Clock Network Design for Through-Silicon-Via (TSV) based 3D ICs
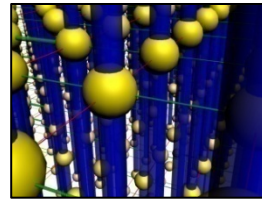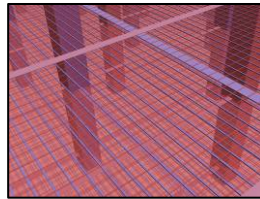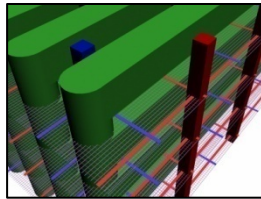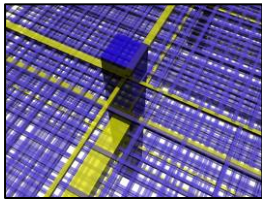
Xin Zhao and Sung Kyu Lim
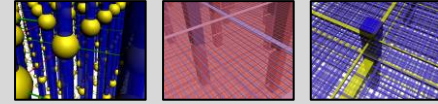
School of Electrical and Computer Engineering

Georgia Institute of Technology

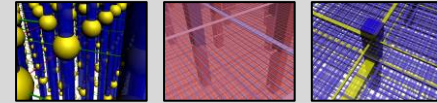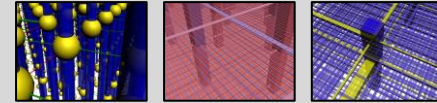**Atlanta, Georgia, U.S.A.**

Outline

- **Introduction**

- **Problem formulation**

- **3D clock tree synthesis**

- **Simulation and discussions**

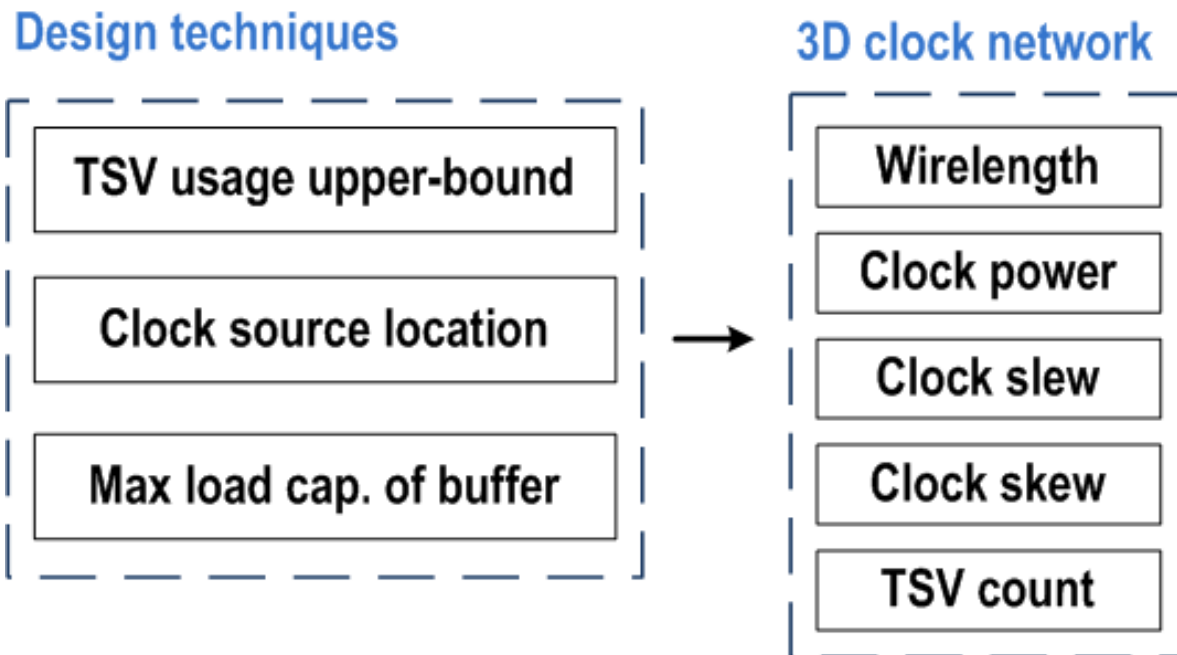- **Conclusions**

Related works

- ## Through-silicon-via (TSV)
  - Fabrication and characterization
  - Reliability issues [Ramm, etc. ECTC'08] [Wright, etc. ECTC'08]…

- ## Low-power 3D clock network
  - A fabricated 3D clock distribution network [Pavlidis, etc. CICC'08]
  - A separate layer of clock distribution network for power reduction [Arunachalam, etc. VLSI'08]

- ## 3D clock network design and optimization
  - Thermal-aware 3D clock design, 3D clock routing algorithm [Minz, etc. ASPDAC'08]
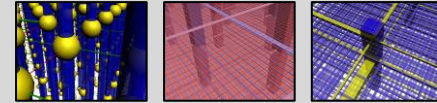 - Pre-bond testable 3D clock synthesis [Zhao, etc. ICCAD'09]

Contributions

- **The major goals**
  - **Clock skew minimization**
  - **Clock slew control**
  - **Clock power reduction**
- **Investigate the impact of design techniques on 3D clock network**

Design techniques

TSV usage upper-bound

Clock source location

Max load cap. of buffer

3D clock network

Wirelength

Clock power

Clock slew

Clock skew

TSV count

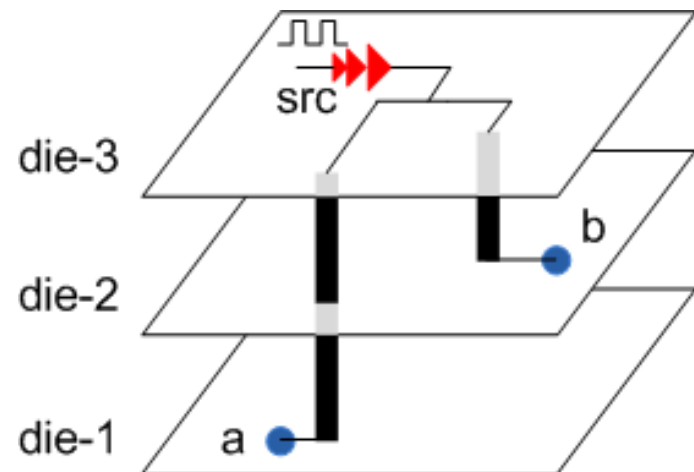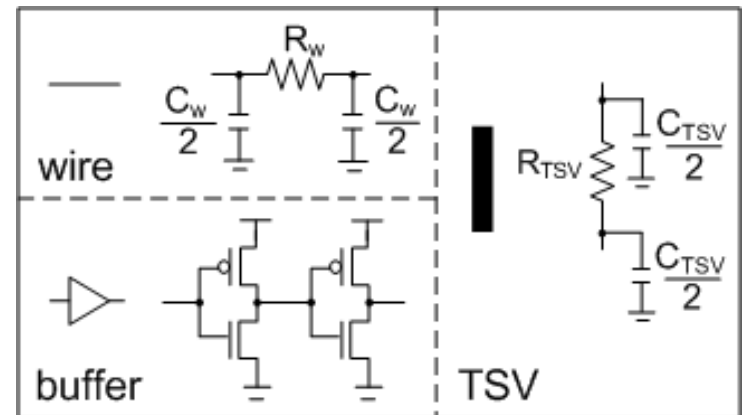# Electrical model and TSV usage

- **Electrical model**
  - Wire
  - TSV
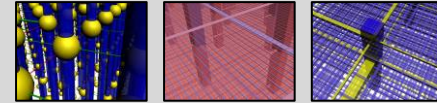 - Clock buffer

- **TSV upper bound**
  - Maximum number of TSVs allowed between adjacent dies

- **TSV count (#TSVs)**
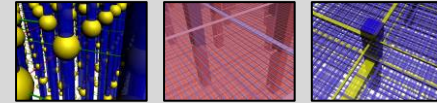 - Total number of TSVs used in 3D tree
  - Stacked-TSV

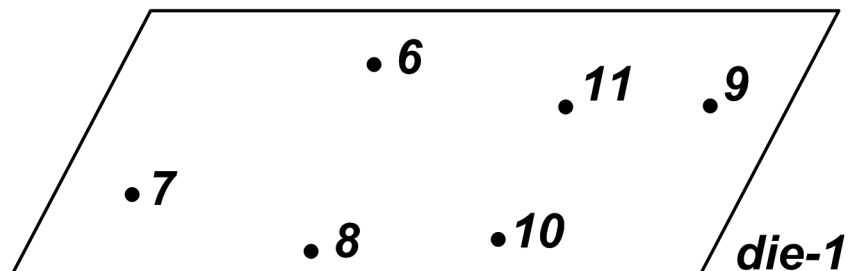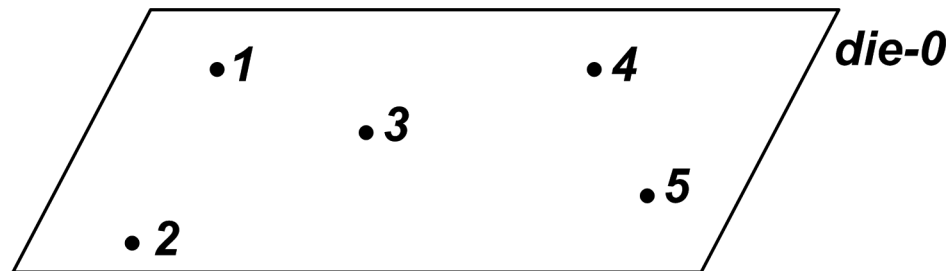# Problem formulation: 3D clock tree synthesis

- **Input**
  - **Sink set (N dies), clock source location**
  - **Upper bound of TSV usage**
  - **Slew constraint**

- **Output**
  - **Zero-Elmore-skew 3D clock tree**

- **Object**
  - **Zero-Elmore-skew**
  - **Minimize wirelength, clock power**

- **Constraint**
  - **Maximum slew**
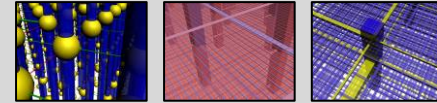 - **Upper bound of TSV usage**

3D clock tree design flow

- **Input:**
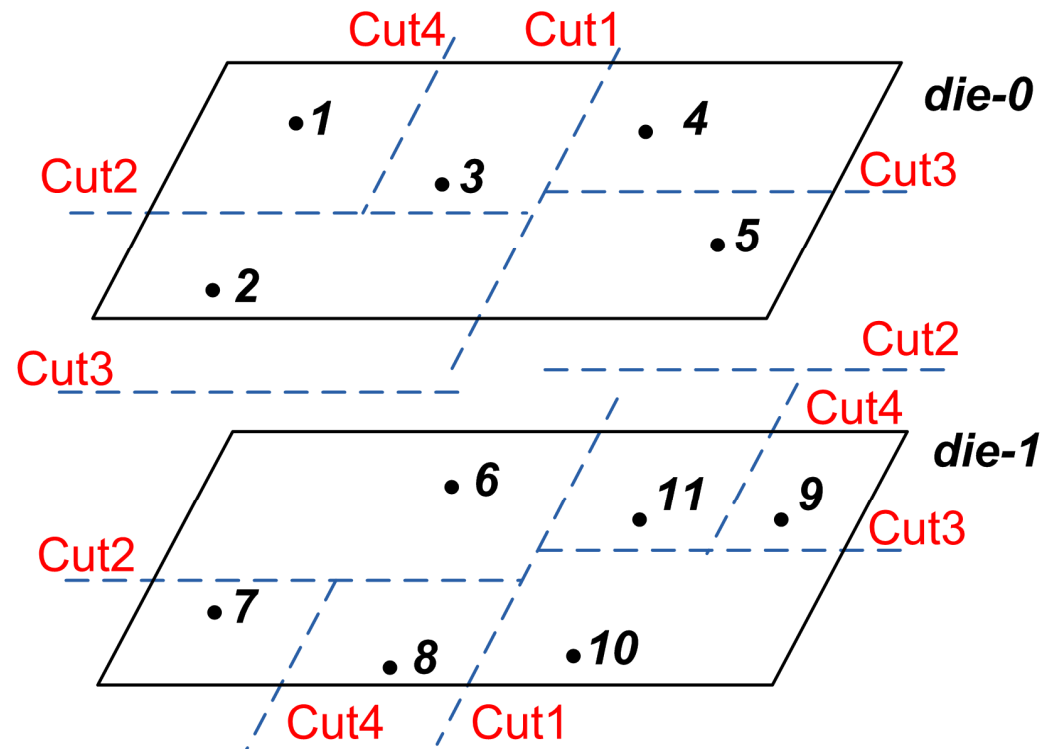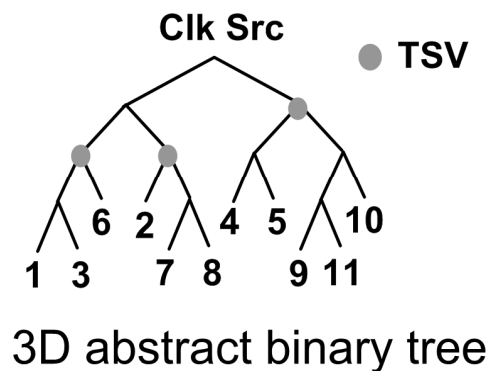 - **a set a sinks on N die**
  - **Upper bound of TSV**

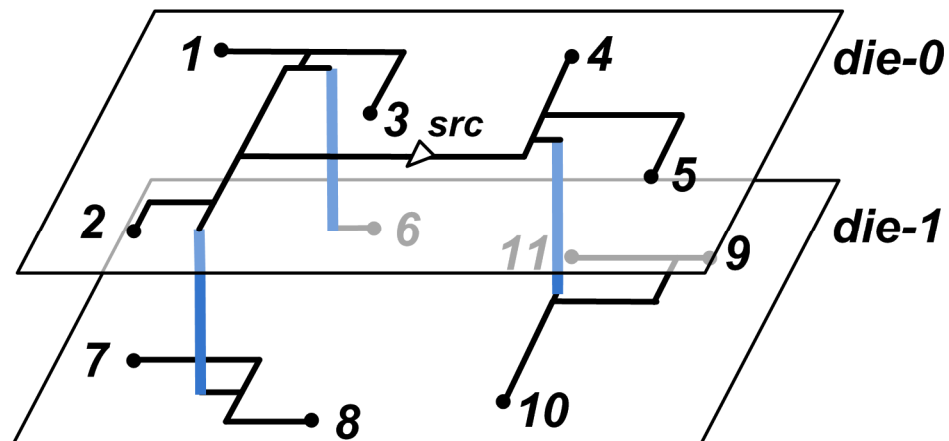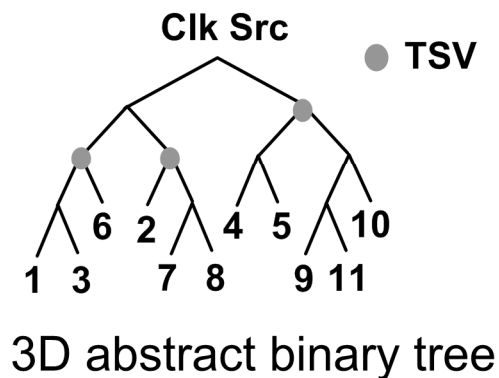**Upper bound of TSV = 3, clock source locates on die-0**

- ## Step-1:
  - **Recursive top-down partition**
  - **3D Method of Means and Medians (3D-MMM)**
  - **3D abstract binary-tree generation**
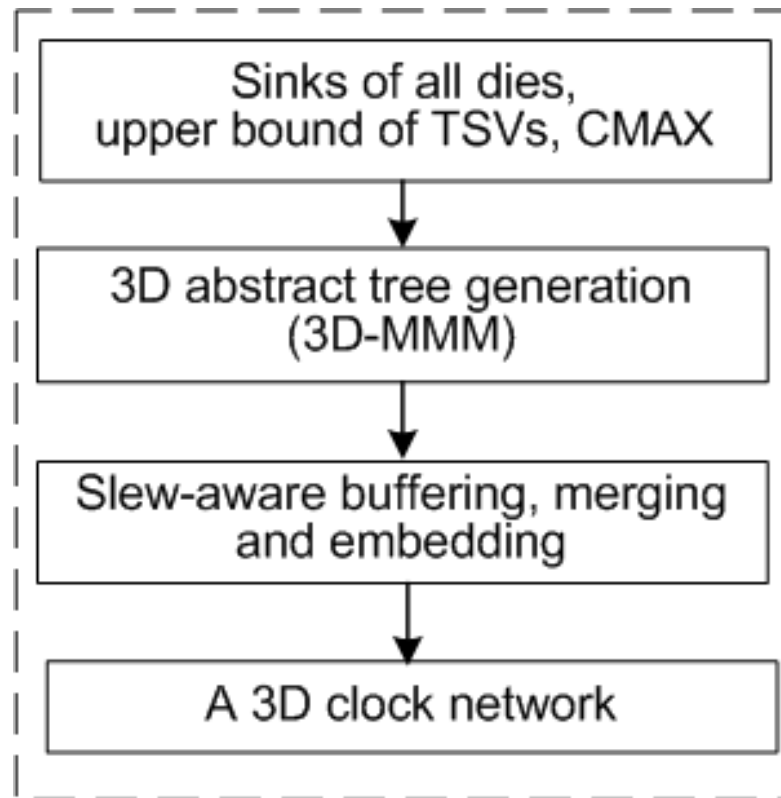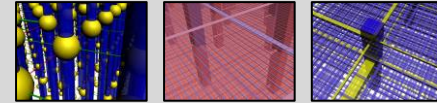

3D abstract binary tree

3D clock tree design flow (cont.)

- ## Step-2:
  - **Merging and slew-aware buffering, embedding**
  - **3D clock tree with multiple TSVs**

- ## Unique property of 3D clock tree
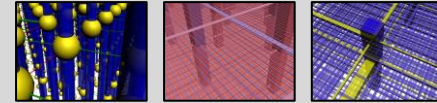 - **A complete tree + many sub-trees**

3D abstract binary tree

3D clock routing algorithm

Sinks of all dies,
upper bound of TSVs, CMAX

↓

3D abstract tree generation
(3D-MMM)

↓

Slew-aware buffering, merging
and embedding

↓

A 3D clock network

3D clock tree synthesis
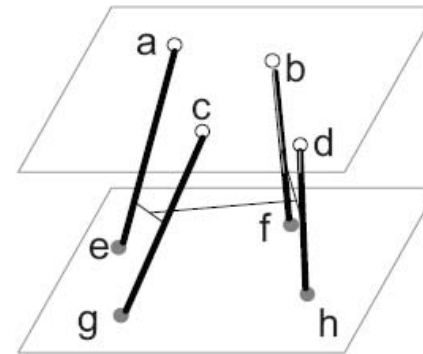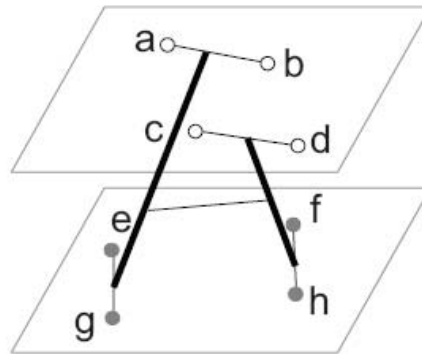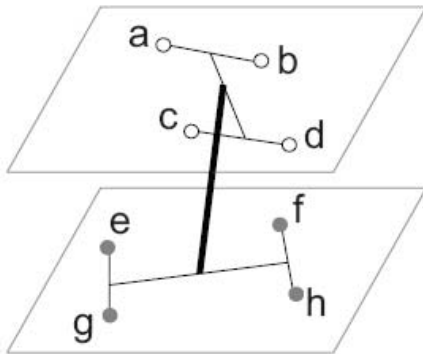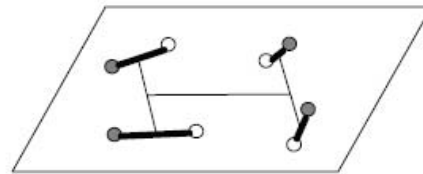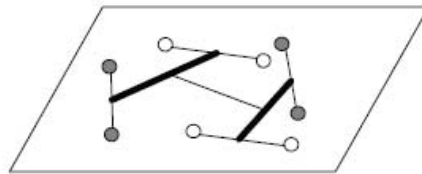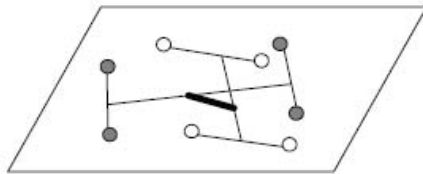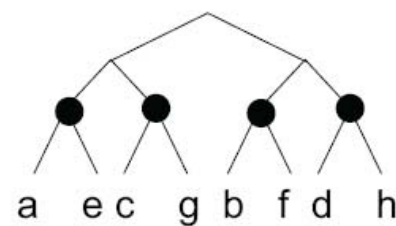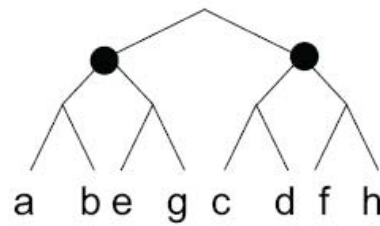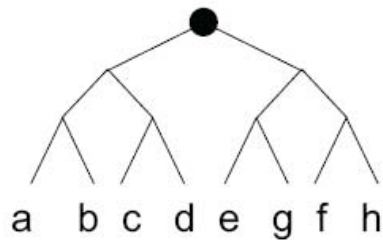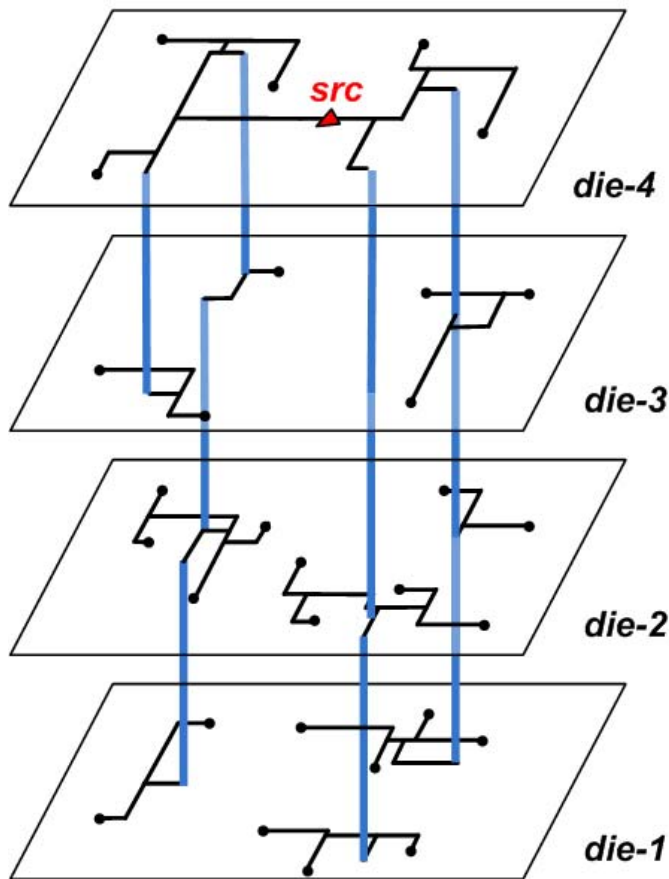
- **3D abstract tree for the N-die stack**
  - **N-colored binary tree**
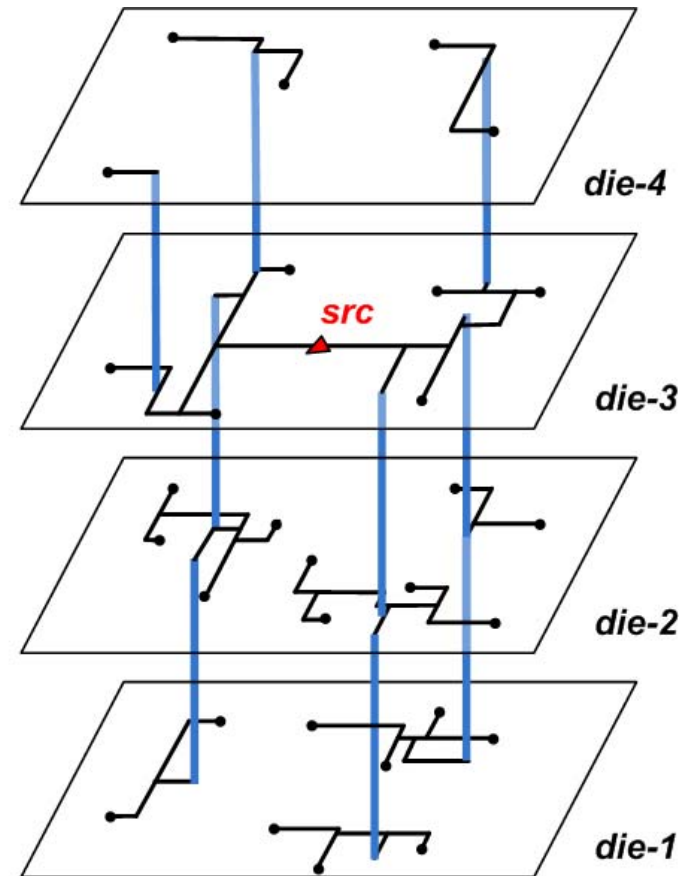 - **Clock source location**
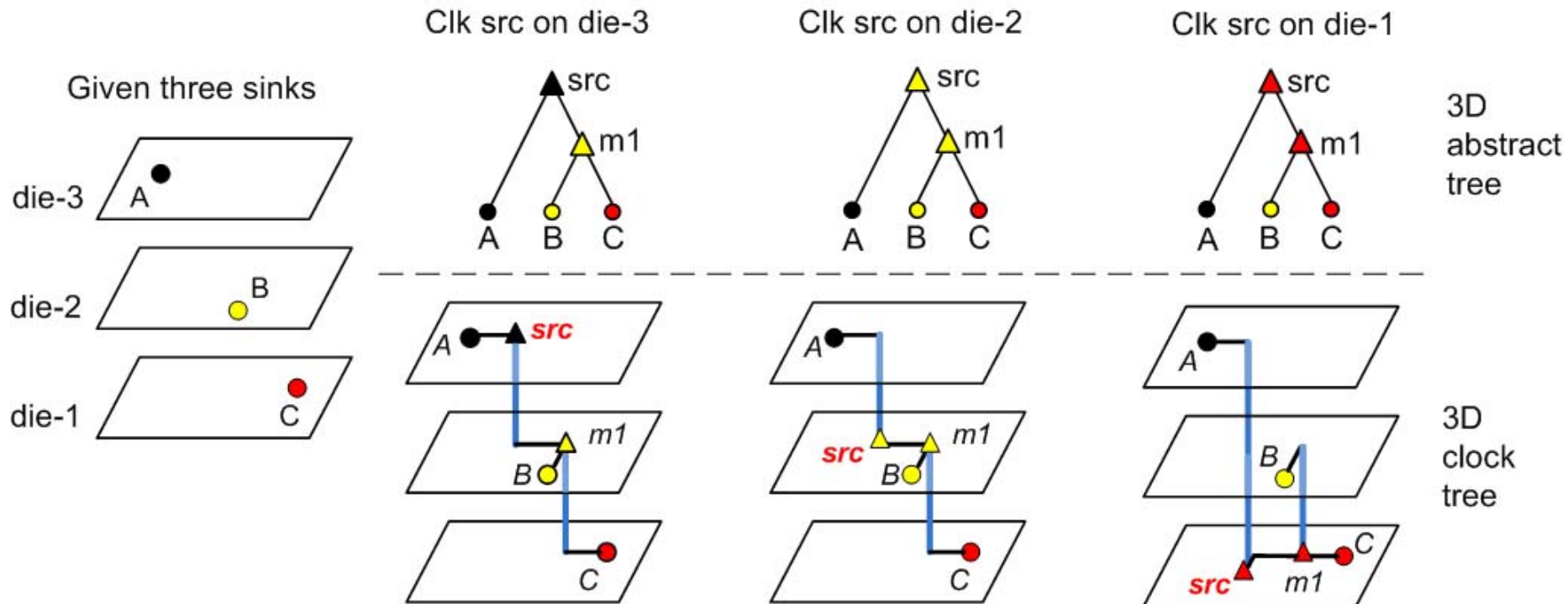
3D clock tree in multiple-die stack
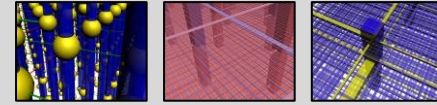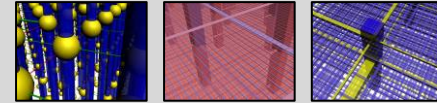
- **A complete tree + many sub-trees**

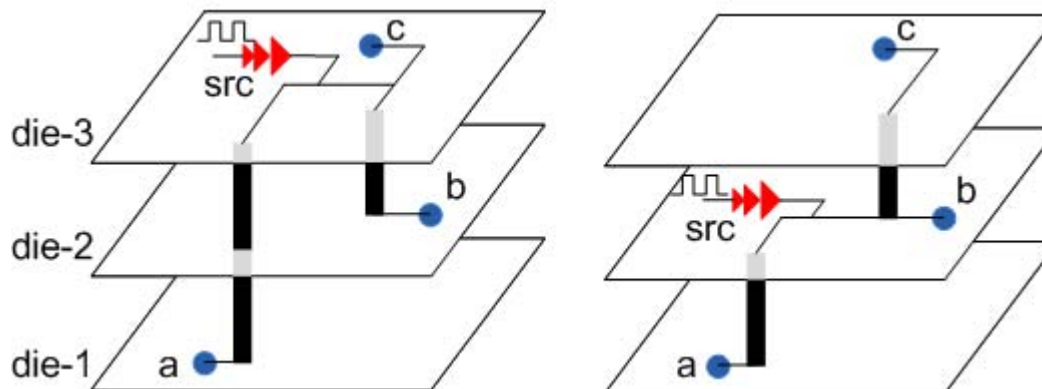Four-die 3D clock tree, src on die-4

Four-die 3D clock tree, src on die-3
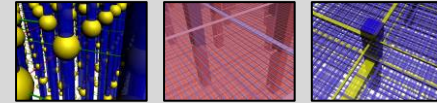
Clock source location

- **Clock source on middle die tends to reduce #TSVs and wirelength**
- **Theoretical maximum TSV usage:**
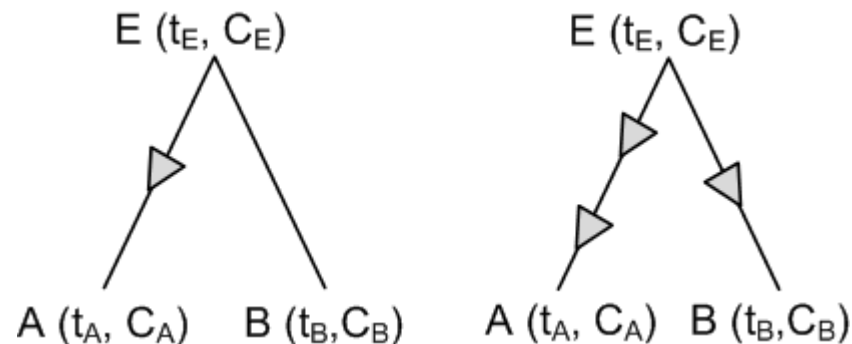 - M sinks evenly distribute on N dies, clock source locates on die-s

$$\frac{M}{N} \times \left(\sum_{i=1}^{s-1} (s-i) + \sum_{i=s+1}^{N} (i-s) \right)$$
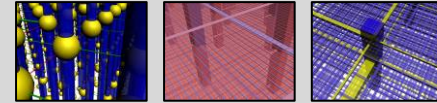
Buffering and merging

- **Goal**
  - **Slew control**
    - **Maximum loading capacitance (CMAX) of clock buffers**
  - **Wirelength reduction**
- **Object**
  - **Zero-Elmore skew**
  - **Clock power minimization**

$E\ (t_E, C_E)$ $E\ (t_E, C_E)$

$A\ (t_A, C_A)$ $B\ (t_B, C_B)$ $A\ (t_A, C_A)$ $B\ (t_B, C_B)$

Detail experiment settings

- **45nm technology:**
  - Frequency = 1GHz, V_{dd} = 1.2V
  - Clock slew < 10% of clock period (CMAX = 300fF)
  - Clock skew < 3%~4% of clock period
  - Wire: R = 0.1 Ω/um, C = 0.2 fF/um
  - Buffer: R_d=122 Ω, C_L = 24 fF, t_d = 17 ps
  - TSV: R_{TSV} = 0.035 Ω, C_{TSV} = 15.48fF
    - 10 um X 10 um, via-last
    - Thinned-die height = 20 um
- **Results are from SPICE simulation**
  - Skew, slew, power
- **We use two cases: four-die and six-die**

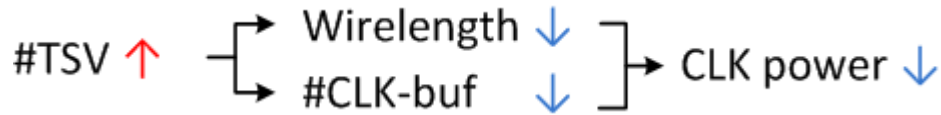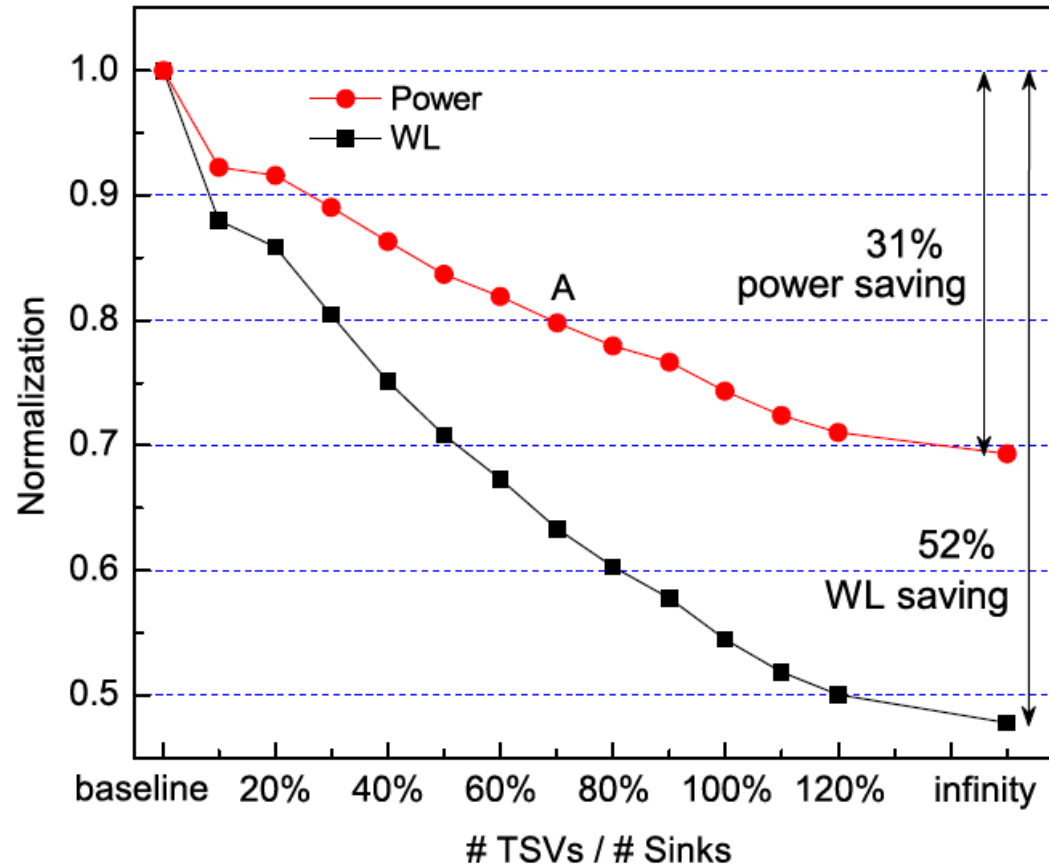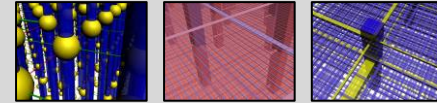| Circuits	# Sinks
r1	267
r2	598
r3	862
r4	1903
r5	3101

Sample 3D clock trees

r5, six-die

die 1

die 3
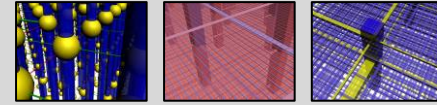
source
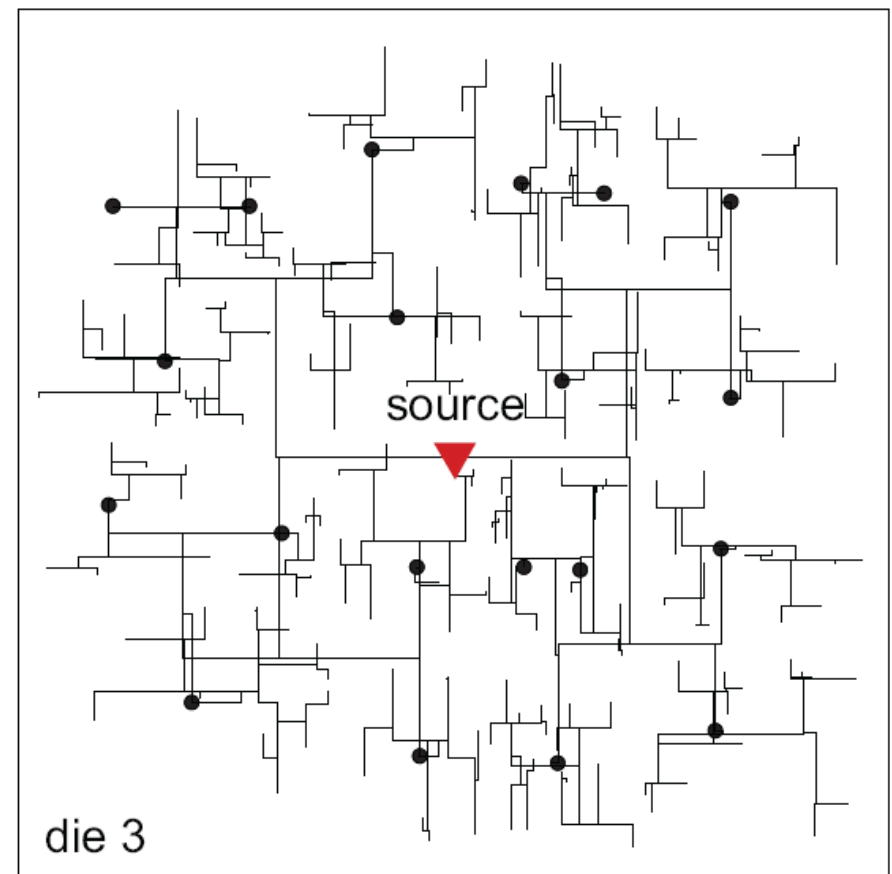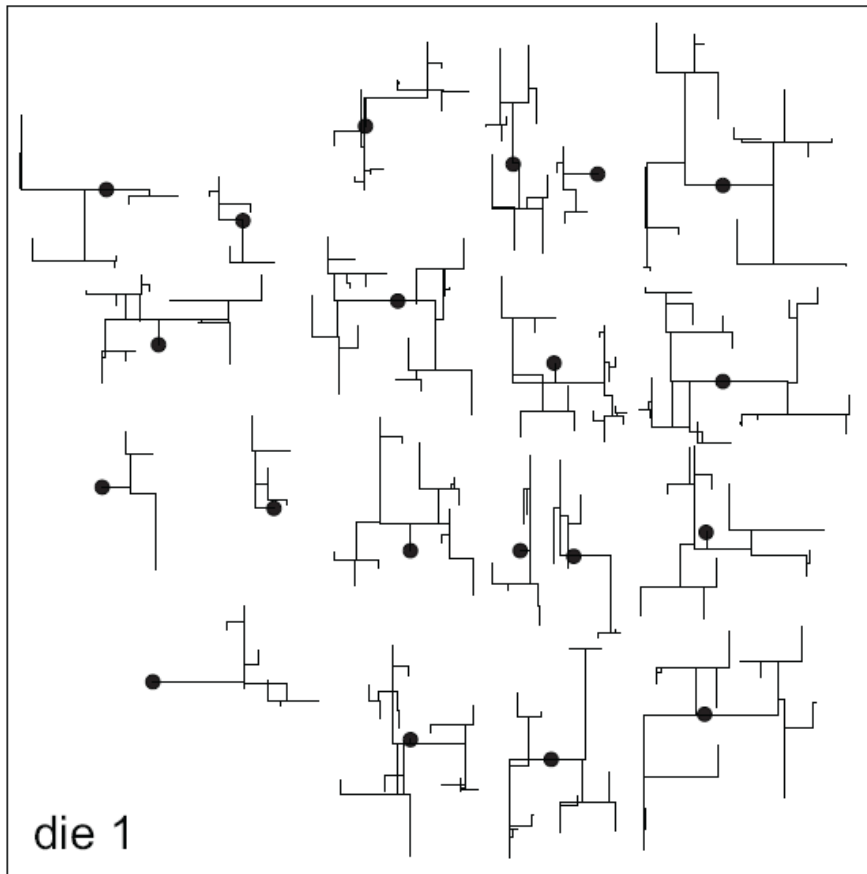
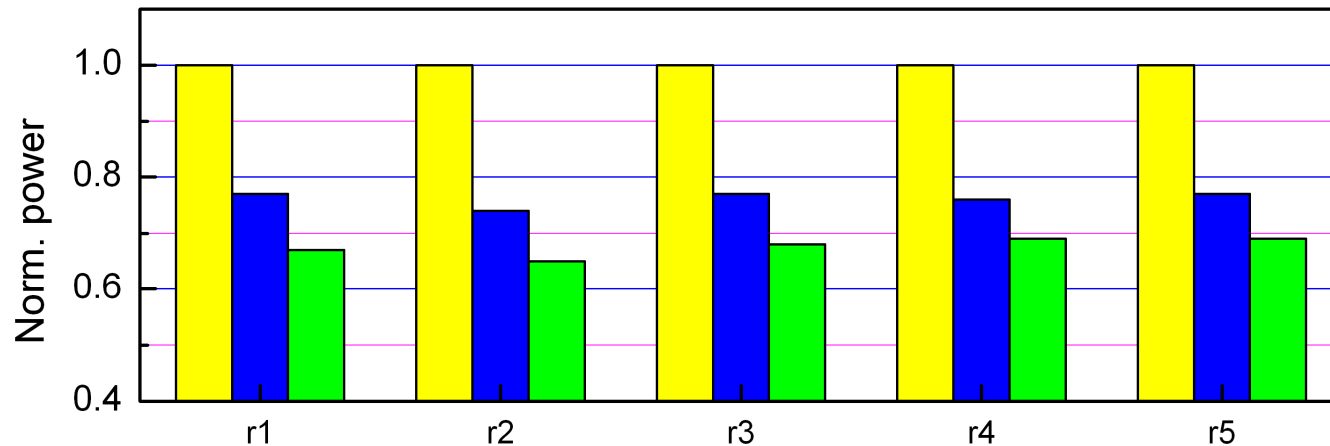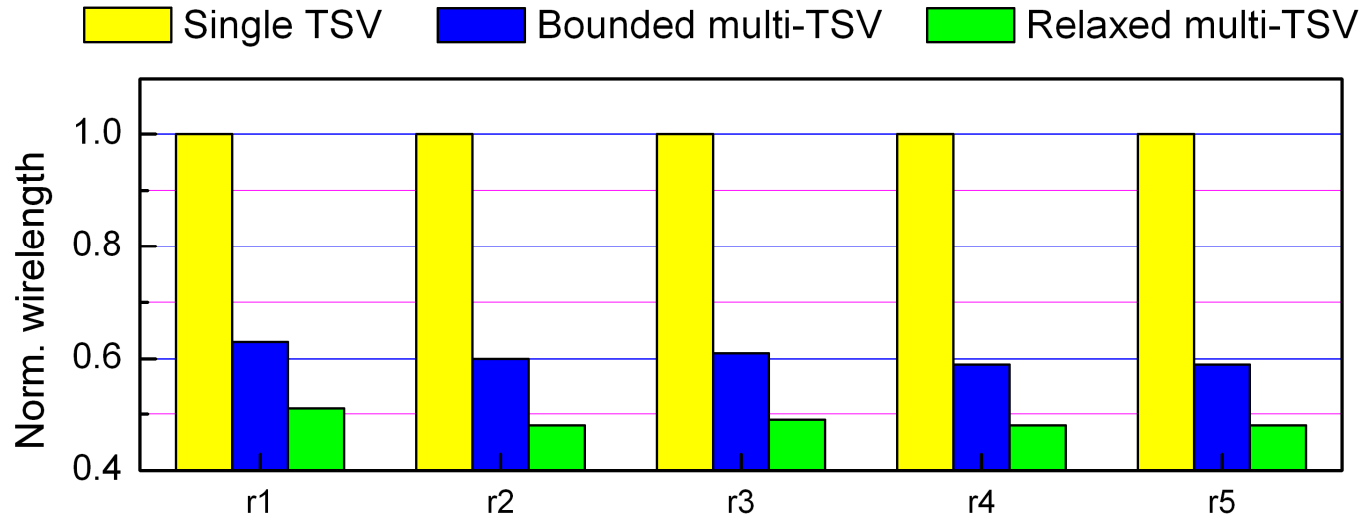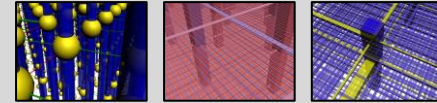**#TSVs = 20**

Impact of TSV bound on wirelength and power

Point A: 20% power saving, TSV bound ⩾ 70% of #sinks

Multi-TSV vs Single-TSV: four-die stack

Legend: ■ Single TSV ■ Bounded multi-TSV ■ Relaxed multi-TSV
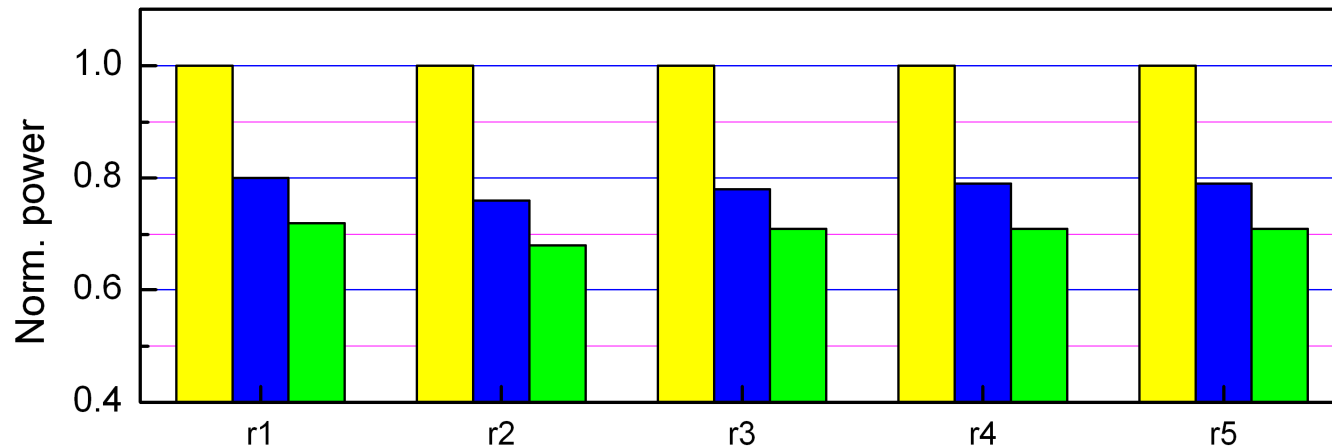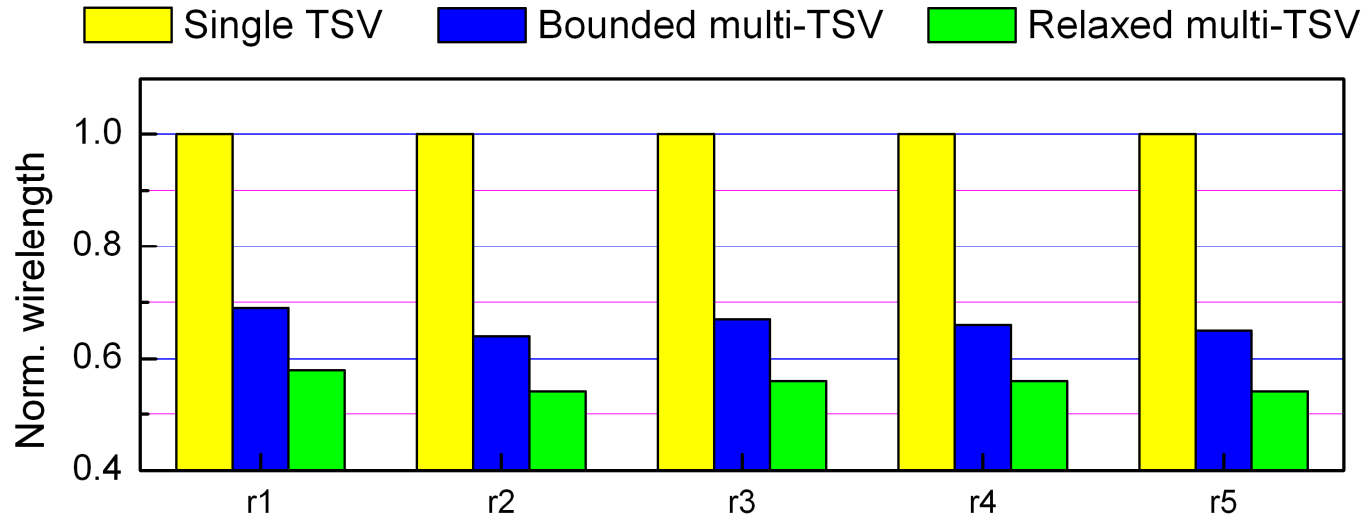
#TSVs (Bnd):   139   309   432   1003   1631
#TSVs (Relax): 265   579   819   1893   3097

Multi-TSV vs Single-TSV: six-die stack

Legend: Single TSV (yellow), Bounded multi-TSV (blue), Relaxed multi-TSV (green)

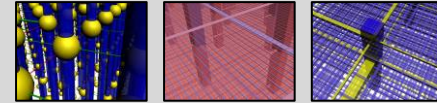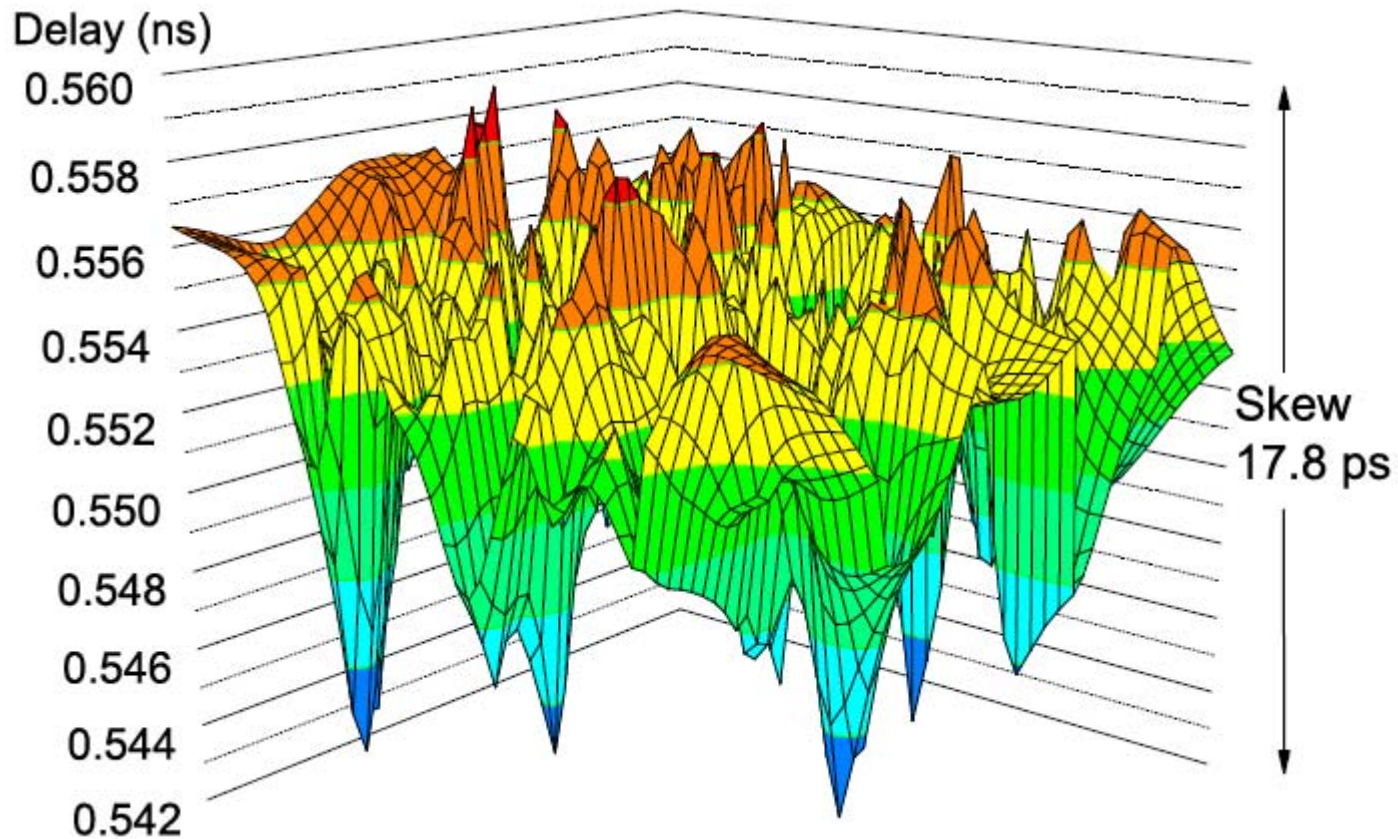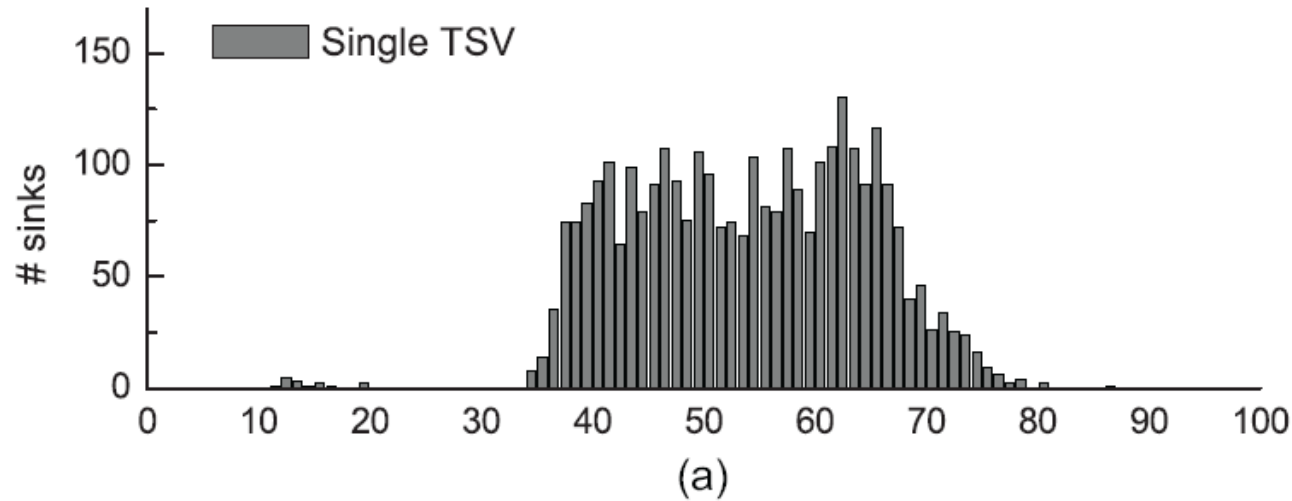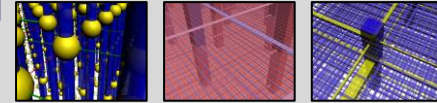|	r1	r2	r3	r4	r5
#TSVs (Bnd):	222	483	701	1594	2588
#TSVs (Relax):	399	908	1301	2980	4782

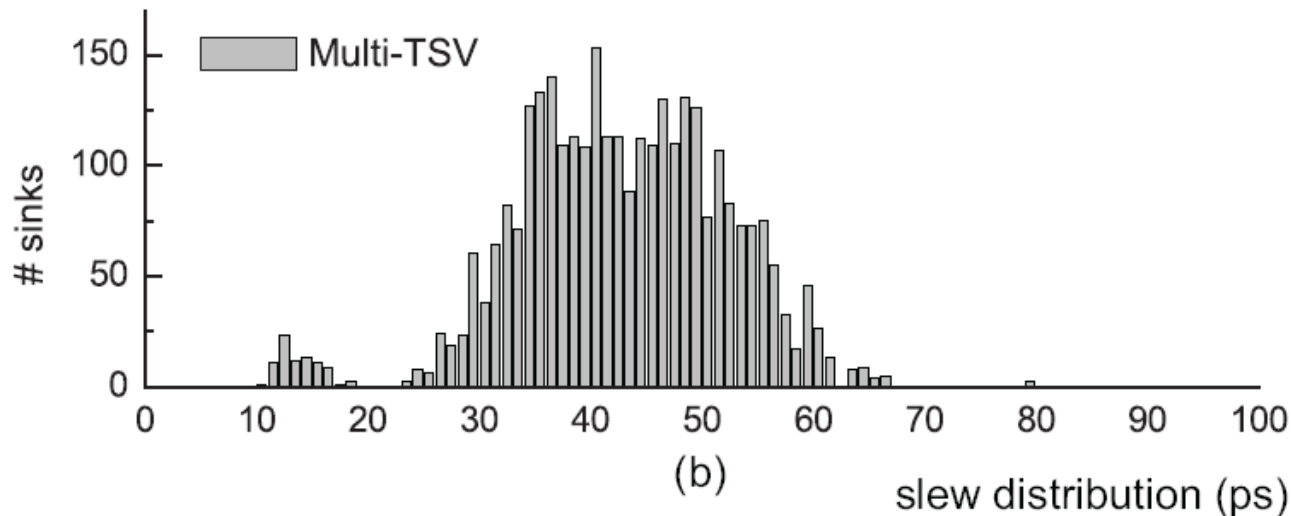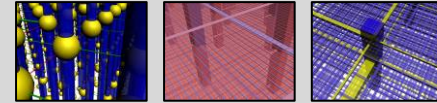# Clock skew in four- and six- die stack
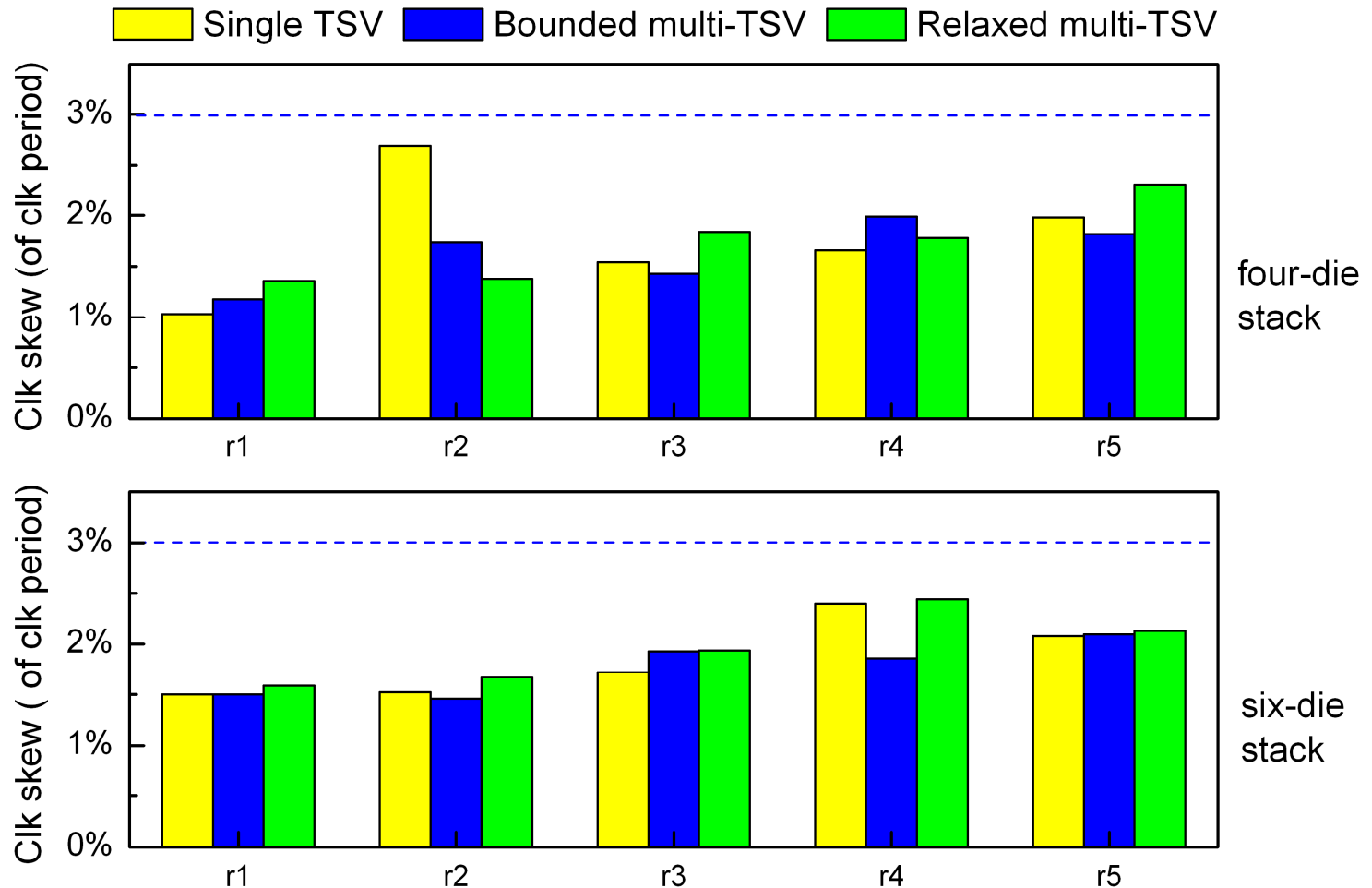
r5, six-die

Impact of TSV bound on slew distribution

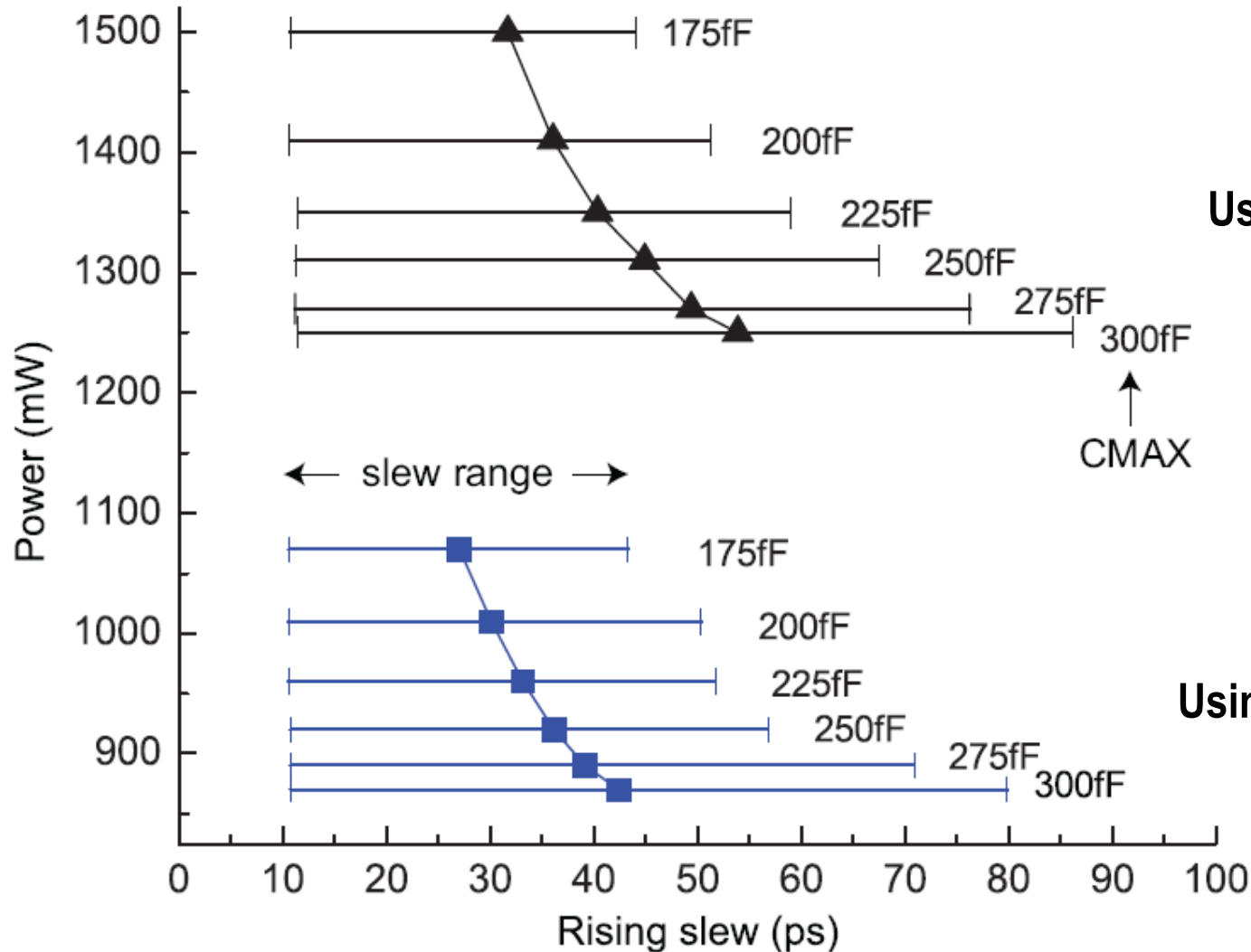r5, six-die
CMAX=300fF

[11.4ps, 86.2ps]
Avg. 53.9ps
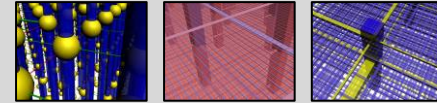#Bufs: 2933

[10.9ps, 79.6ps]
Avg. 42.6ps
#Bufs: 2638

r5, six-die

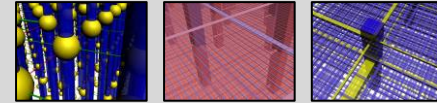**Using single TSV**

Using multiple TSVs
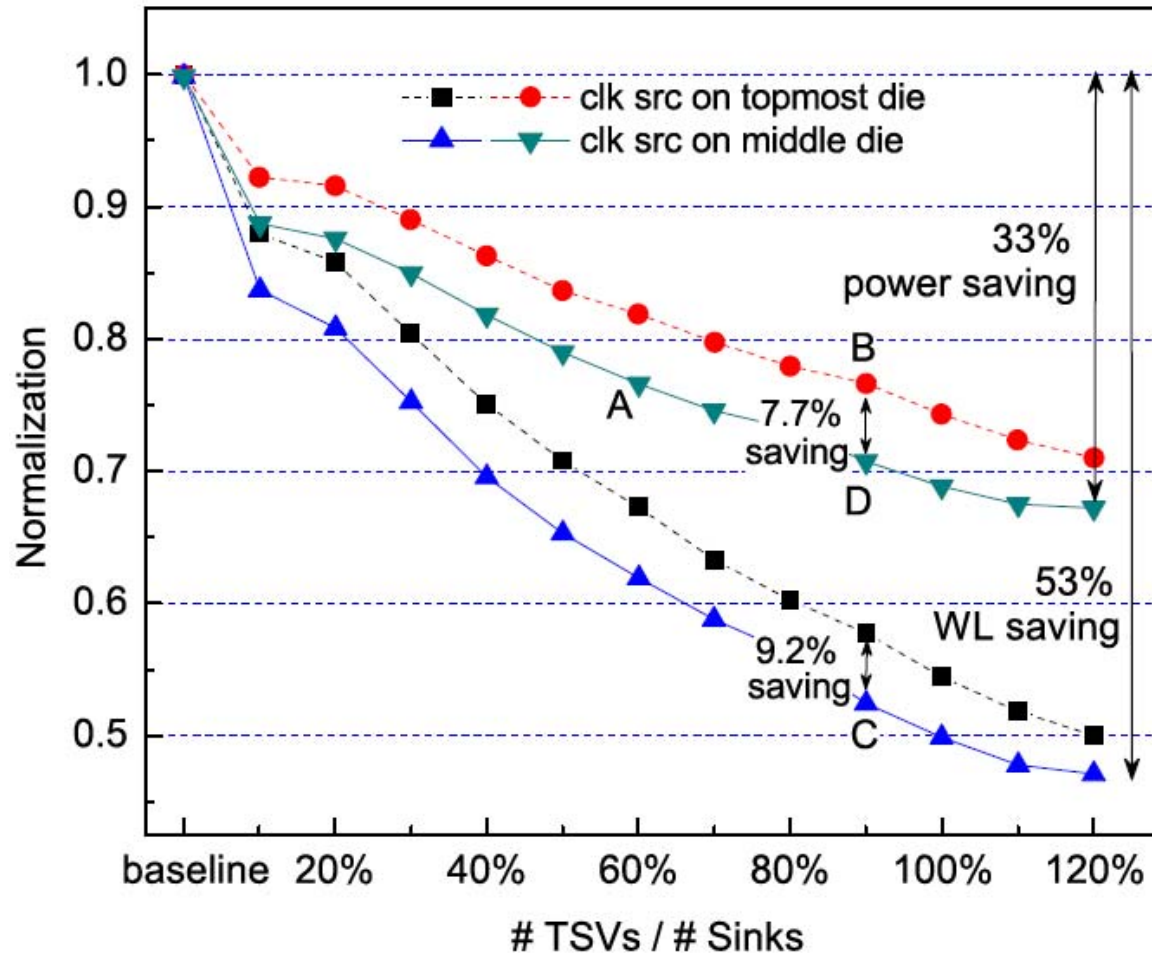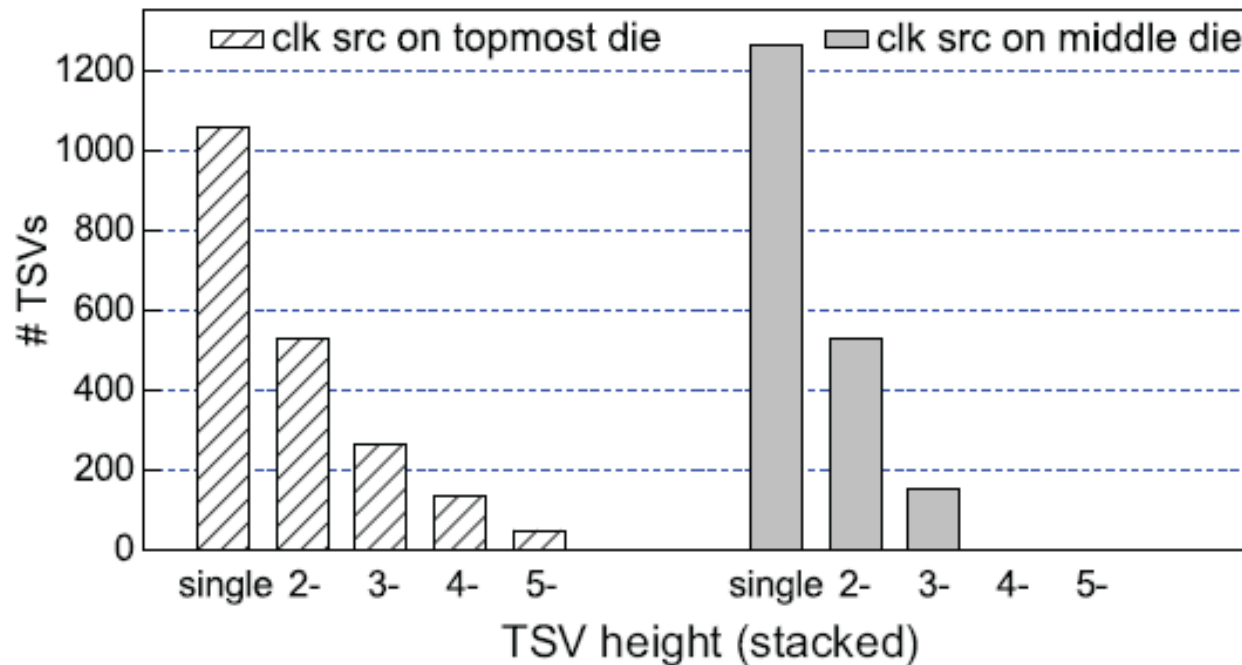
r5, six-die

A uses 33% fewer TSVs than B

Distribution of stacked-TSV heights
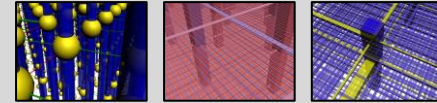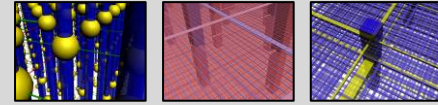
r5, six-die

#TSVs = 3720   #TSVs = 2791

Conclusions

- **Explored design optimization techniques for reliable, low-power, low-slew 3D clock network design.**

- **Using multiple TSVs helps to reduce wirelength and power. Multi-TSV also has better control on slew variations.**

- **Smaller CMAX efficiently lowers the clock slew.**

- **Clock source location affects wirelength, power and TSV usage of the 3D clock network. Middle-die sourcing policy reduces the TSV usage under the same power budget.**

Thank you