CAD Reference Flow for 3D Via-Last Integrated Circuits

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Outline

- Introduction to 3D Integration
- 3D CAD Reference Flow in ITRI
- Conclusions
Motivation for 3D Integration

- Challenges below 22 nm
  - Process Variation
    - New materials = $$$
  - Advanced Lithography
    - Extreme UV, or E-beam
    - Both = $$$

- Thin/Small, Multi-function
- High performance, Low power
- Heterogeneous integration
- ...

Source: ITRS, 2007
Keys of 3D Integration

Source: ZyCube / Tohoku, MRS, 2009
Source: Leti (Fr), D43D, 2009  15th ASP-DAC, Jan. 20, 2010
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TSV-Related Terminologies

- Through silicon via (TSV)
- Front metal (FM)
- Front via (FV)
- Front pad (FP)
- Back metal (BM)
- Back pad (BP)
ITRI Integration Approach

- Treat each TSV as a cell through silicon to FM
- Scalable face-to-back bonding
- Align BP with TSV to eliminate BP placement
Layer Partition

- TSMC 90nm-G process with TSV and FP cells

15th ASP-DAC, Jan. 20, 2010
Multi-Tier P&R Methodology

- Technology Lef: FM/FV
- Liberty: FP/STC
- Wire Model: FM/FV
- GDS: FP/STC/FTC
- FP/STC Location
- Timing Constraints
- Clock Skew
- Netlists

DRC/LVS Verification

Multi-Tier Mergence: DSPF and GDSII

Parasitic Extration

Timing Analysis

Floorplanning

TSV-Aware Placement with Via-Alignment Constraint

Multi-Tier Balanced CTS

Timing-Driven Routing

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TSV-aware Placement with Via-alignment Constraints

- Property 2: On the same tier, any cell and block, except for the FP, can overlap with the STC, and any metal line can be routed over.

- Theorem 1: The alignment constraints can always be satisfied, if the placement of FP and STC is performed from the topmost tier to the bottommost tier.
Multi-Tier Balanced CTS

Tier 1
- Latency: 0.6ns
- Skew: +0.1ns
- Clock Root

Tier 2
- Latency: 0.7ns
- Skew: -0.1ns

Tier 3
- Latency: 0.5ns
- Skew: +0.2ns

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3-Tier Case with Power TSV

- Support 2 kinds of TSV diameters
  - 5um Signal, 50um Power/Ground
# Clock Tree Synthesis Results

<table>
<thead>
<tr>
<th>Tier</th>
<th>Max Latency</th>
<th>Min Latency</th>
<th>Inter-Tier Skew</th>
<th>Max Latency</th>
<th>Min Latency</th>
<th>Inter-Tier Skew</th>
<th>ΔSkew</th>
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<tbody>
<tr>
<td>2 Tiers</td>
<td>0.252</td>
<td>0.252</td>
<td>0.296</td>
<td>0.252</td>
<td>0.252</td>
<td>0.008</td>
<td>-0.288</td>
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<tr>
<td>1</td>
<td>0.111</td>
<td>0.104</td>
<td></td>
<td>0.351</td>
<td>0.344</td>
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<tr>
<td>3 Tiers</td>
<td>0.401</td>
<td>0.386</td>
<td>0.608</td>
<td>0.369</td>
<td>0.35</td>
<td>0.05</td>
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<td>2</td>
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<td>0.381</td>
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<td>0.545</td>
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<td>0.323</td>
<td>0.298</td>
<td></td>
<td>0.68</td>
<td>0.657</td>
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<tr>
<td>4 Tiers</td>
<td>0.635</td>
<td>0.624</td>
<td>1.546</td>
<td>0.627</td>
<td>0.614</td>
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<td>1.27</td>
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</tr>
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</table>
Routing – DRC/LVS

- Design rules are provided for the five extra mask layers

- 3D LVS need to evolve to tackle the vertical interconnect issues across tiers
Different LVS Checking Types

- PortText_A
- PortText_B
- PortText_C
- PortText_D
- PortText_E

Tier (n)

- PortText_W
- PortText_X
- PortText_Y
- PortText_Z

Tier (n+1)

- PortText_M
- PortText_N
- PortText_O

- TSV/BM
- FP

- Mis-port
- Mis-Size
- Mis-alignment

PASS
BEOL & FM Routing
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Conclusions

- Multi-Tier P&R Methodology
  - TSV co-placement
  - Via alignment constraints
  - Balanced CTS
  - DRC/LVS

- Future works on 3D Integration
  - Thermal
  - Mechanical
THANKS FOR YOUR ATTENTION

謝謝您的聆聽