ITRI
Industrial Technology
Research Institute

# CAD Reference Flow for 3D Via-Last Integrated Circuits

**Chang-Tzu Lin (林昌賜)**

Information and Communications Research Lab. (ICL), ITRI, Taiwan

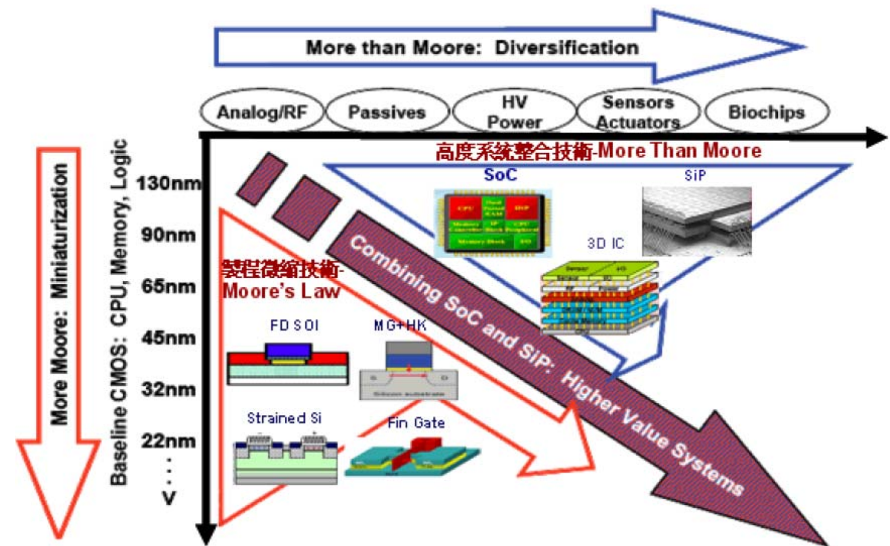
15th ASP-DAC, Jan. 20, 2010

# Outline

- Introduction to 3D Integration
- 3D CAD Reference Flow in ITRI
- Conclusions

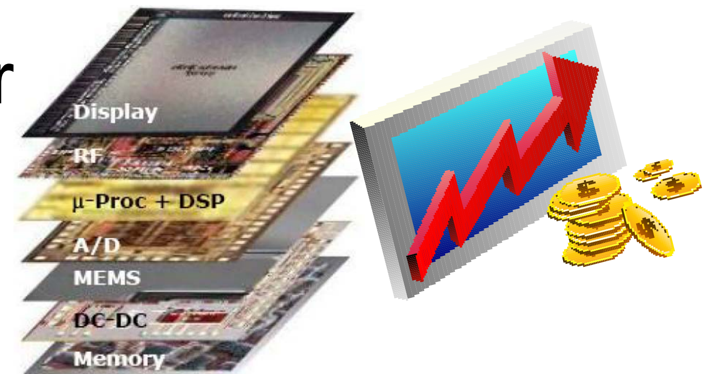
# Motivation for 3D Integration

- Challenges below 22 nm
  - Process Variation
    - New materials = $$$
  - Advanced Lithography
    - Extreme UV, or E-beam
    - Both = $$$

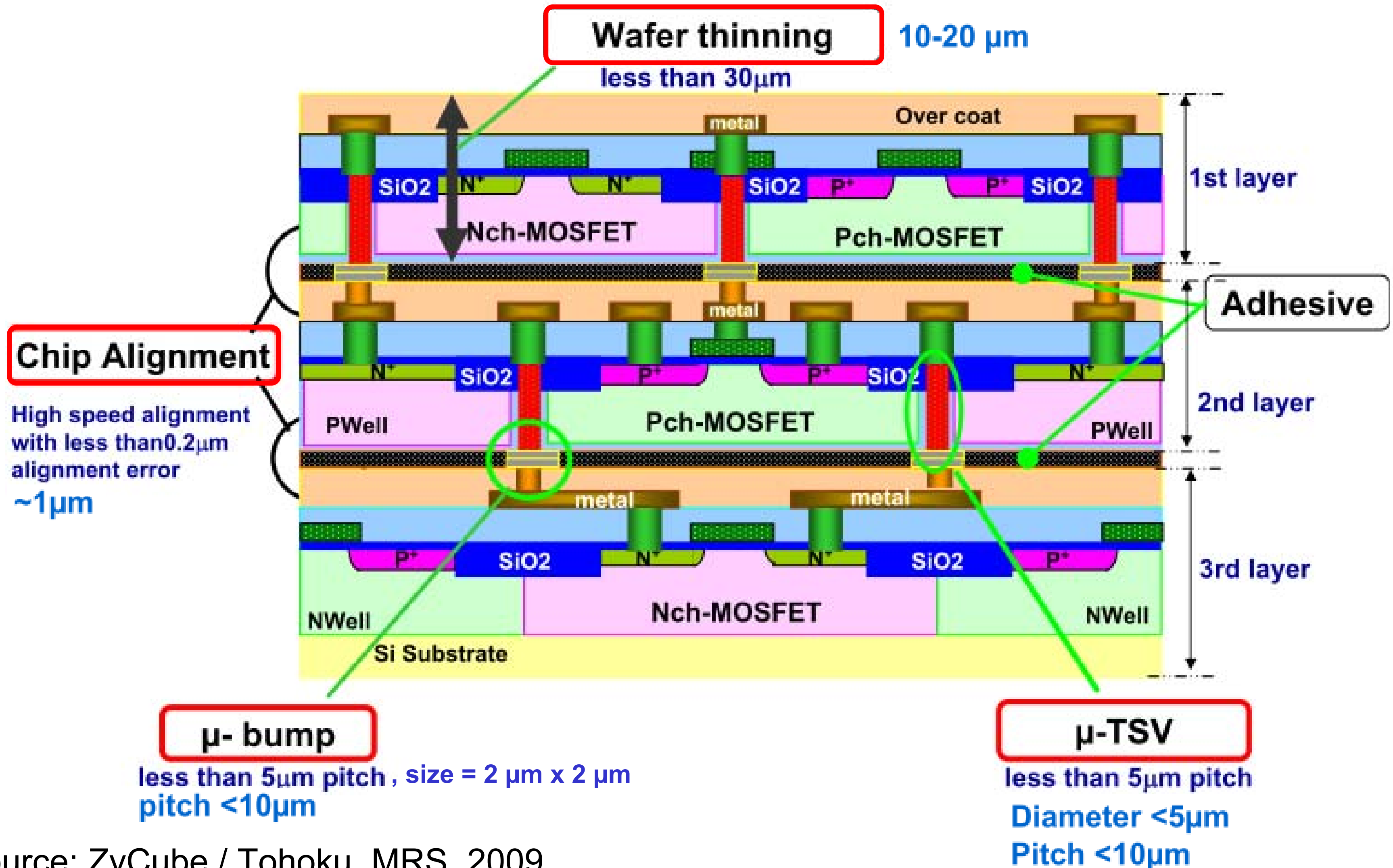



Source: ITRS, 2007

- Thin/Small, Multi-function
- High performance, Low power
- Heterogeneous integration
- ...



# Keys of 3D Integration




Source: ZyCube / Tohoku, MRS, 2009

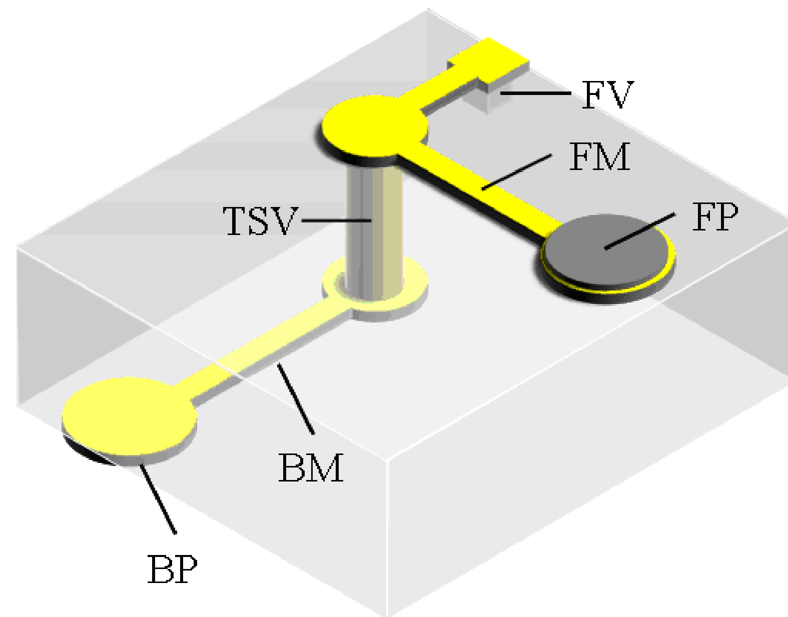
Source: Leti (Fr), D43D, 2009

# Outline

- Introduction to 3D Integration
- 3D CAD Reference Flow in ITRI
- Conclusions

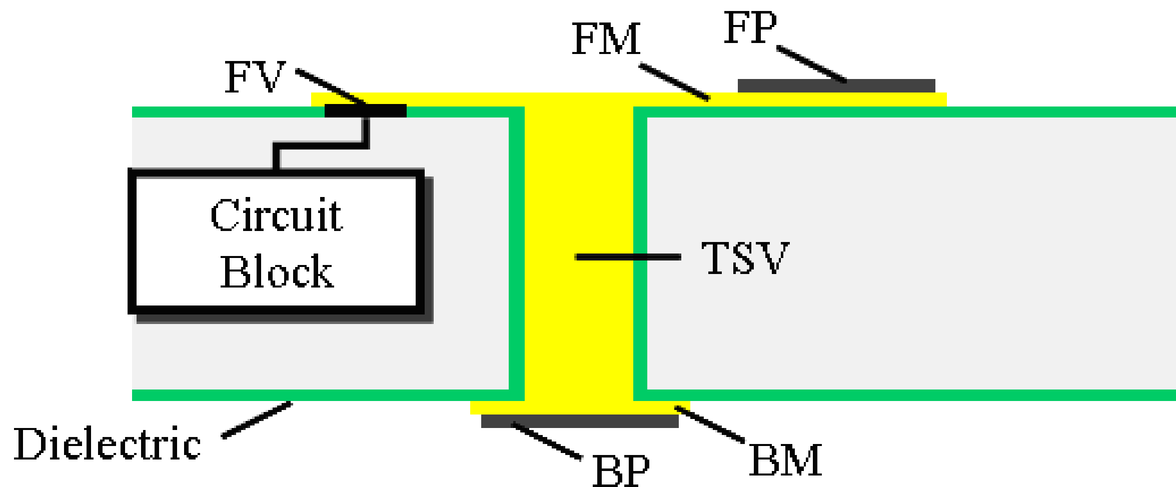
# TSV-Related Terminologies

- Through silicon via (TSV)
- Front metal (FM)
- Front via (FV)
- Front pad (FP)
- Back metal (BM)
- Back pad (BP)



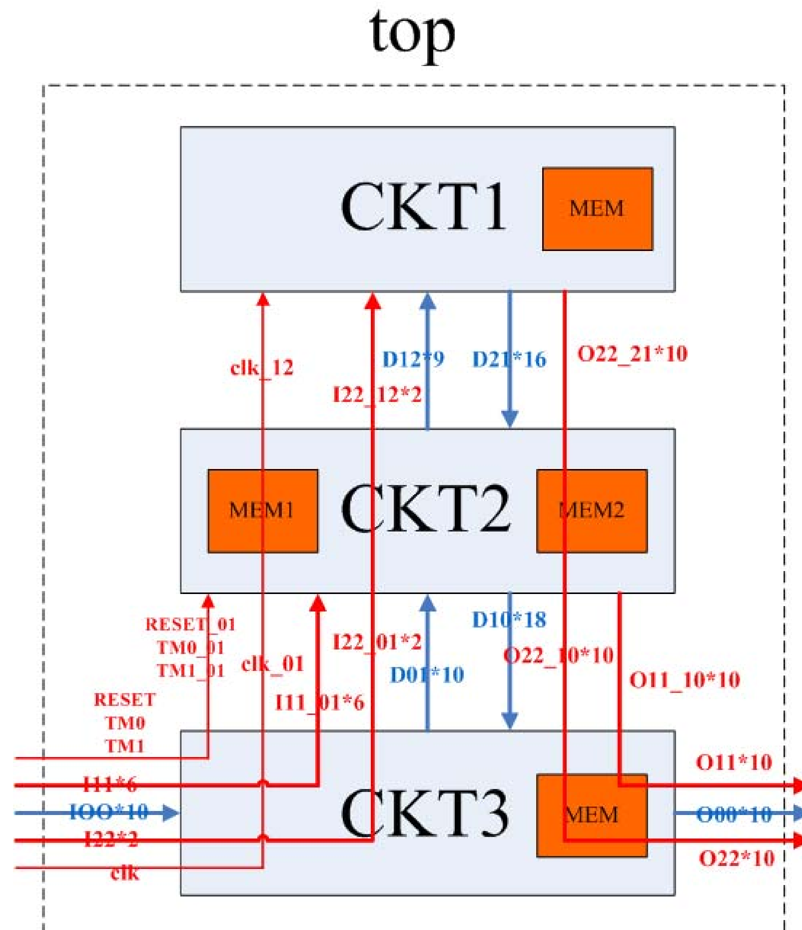
# ITRI Integration Approach

- Treat each TSV as a cell through silicon to FM
- Scalable face-to-back bonding
- Align BP with TSV to eliminate BP placement

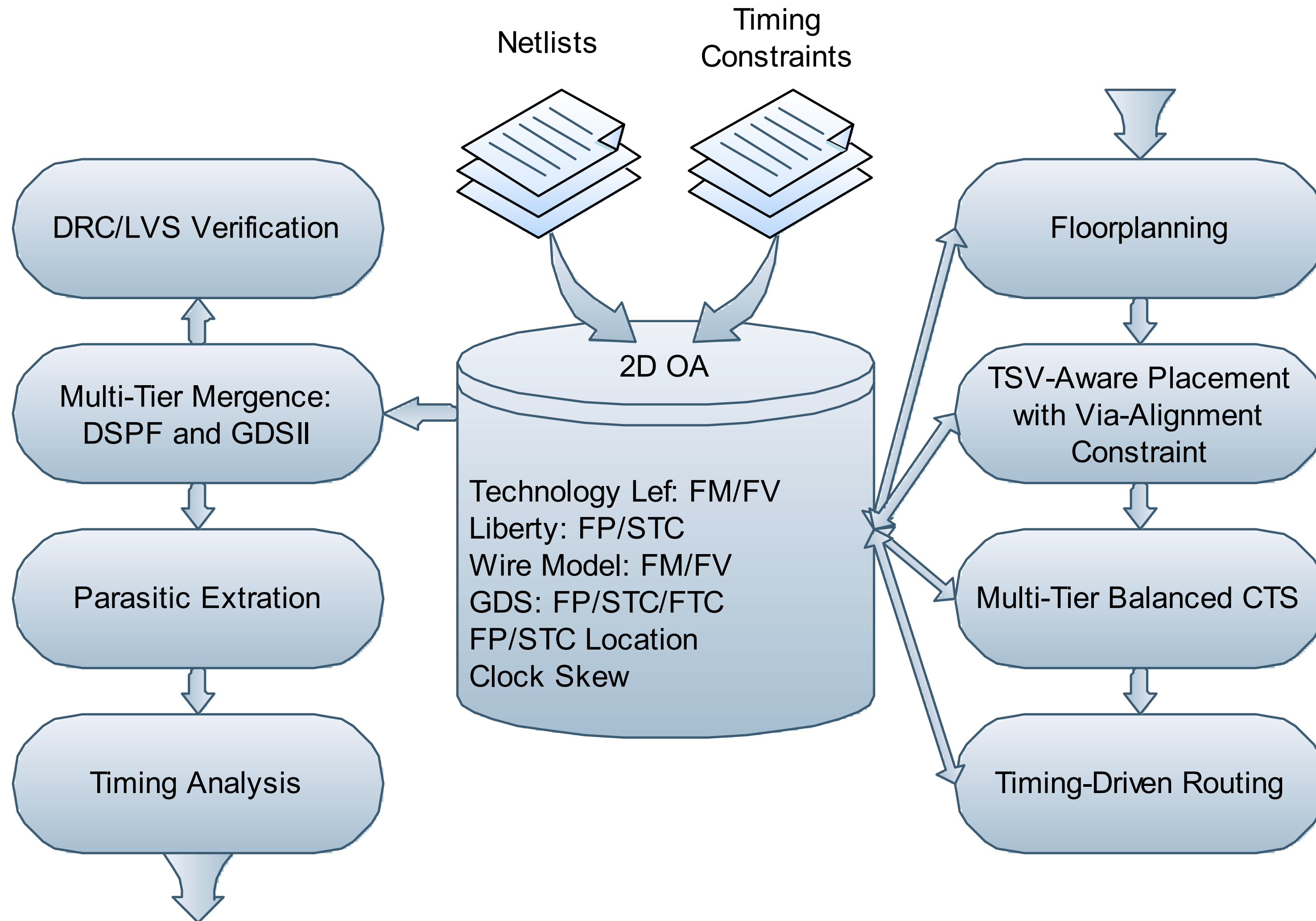


# Layer Partition

- TSMC 90nm-G process with TSV and FP cells



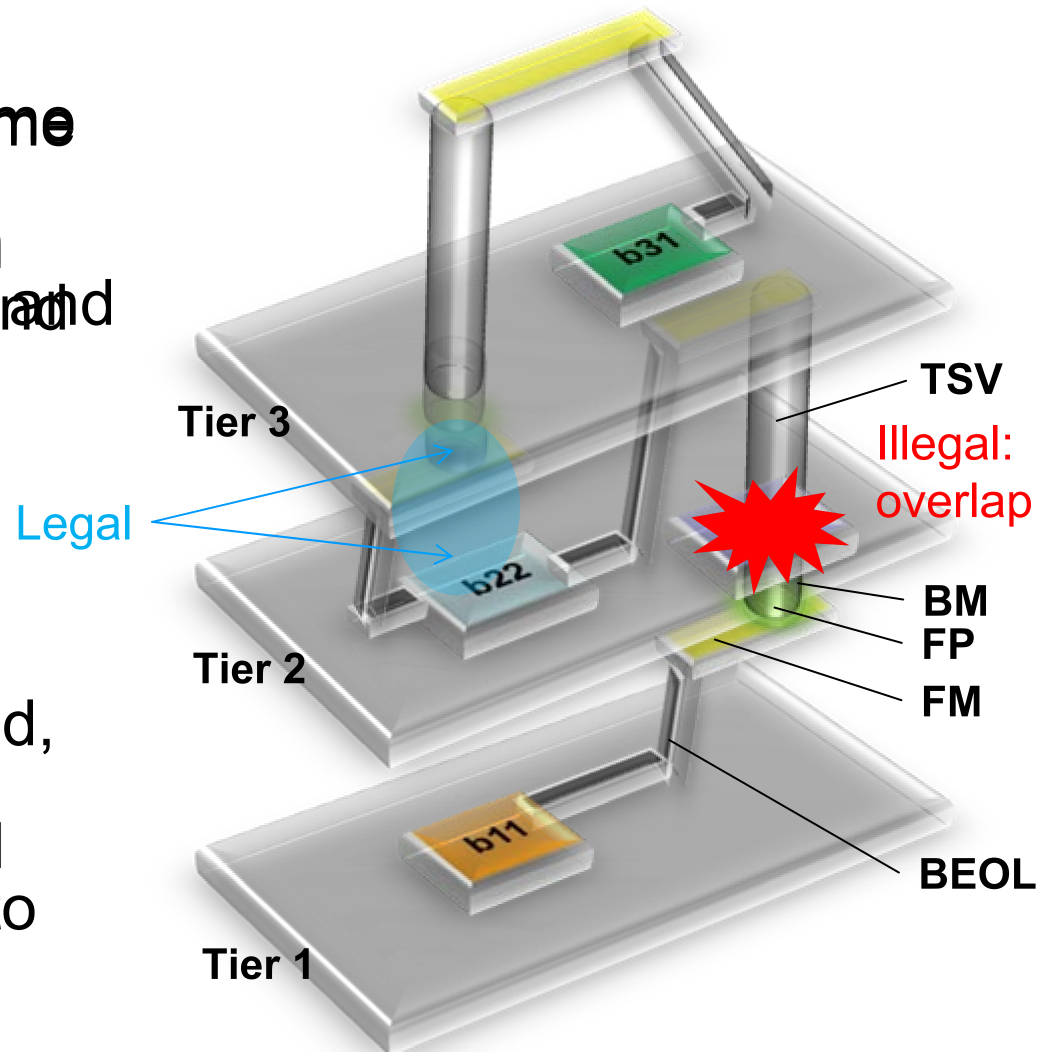
# Multi-Tier P&R Methodology



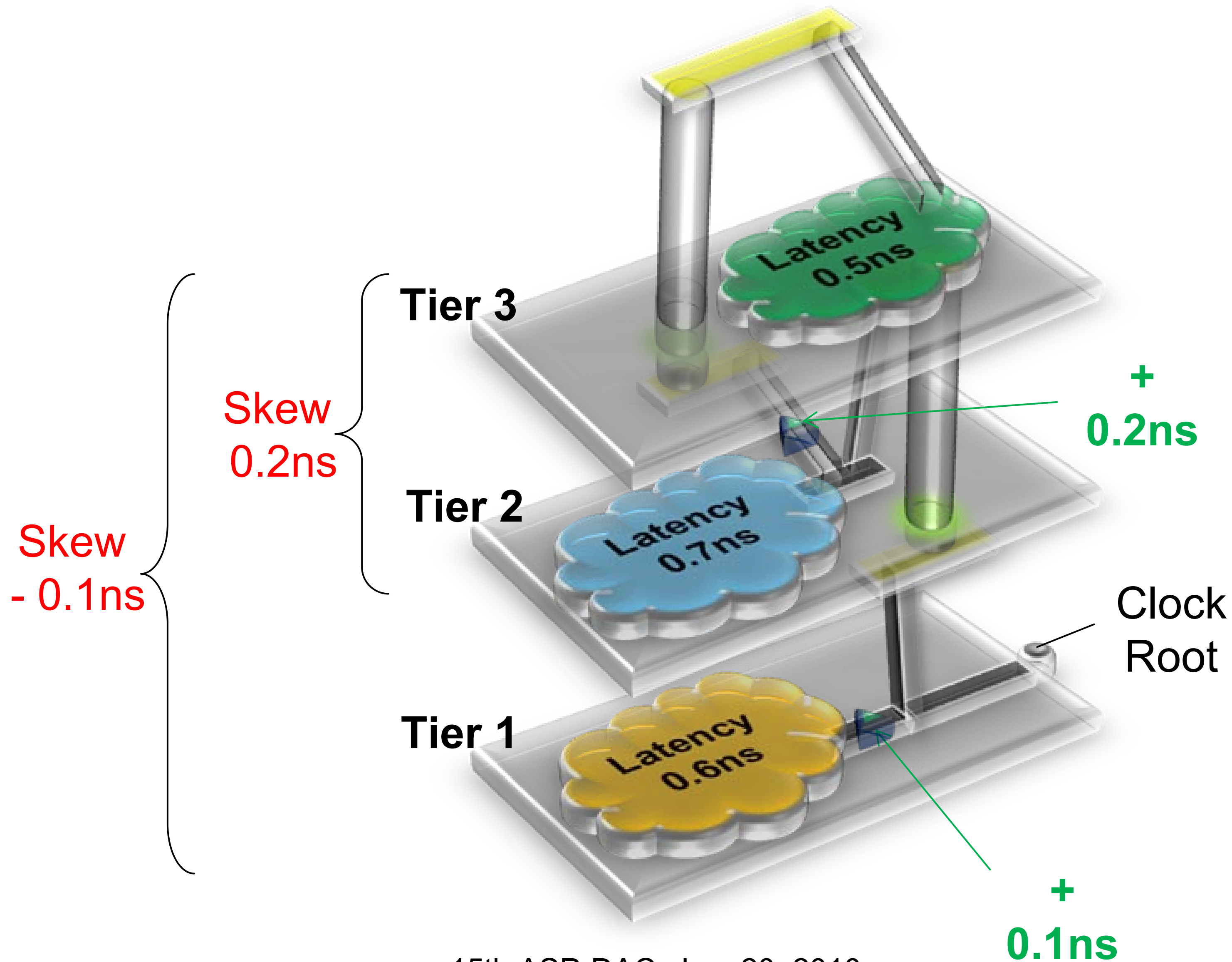
# TSV-aware Placement with Via-alignment Constraints

- Property 1: On the same tier, no cell and block, except for the FP, can overlap with the STC, and no metal line can be routed over.
- Property 2: On the same tier, any cell or block, except for the FP, can overlap with the FP, and any metal line can be routed over.

- Theorem 1: The alignment constraints can always be satisfied, if the placement of FP and STC is performed from the topmost tier to the bottommost tier.

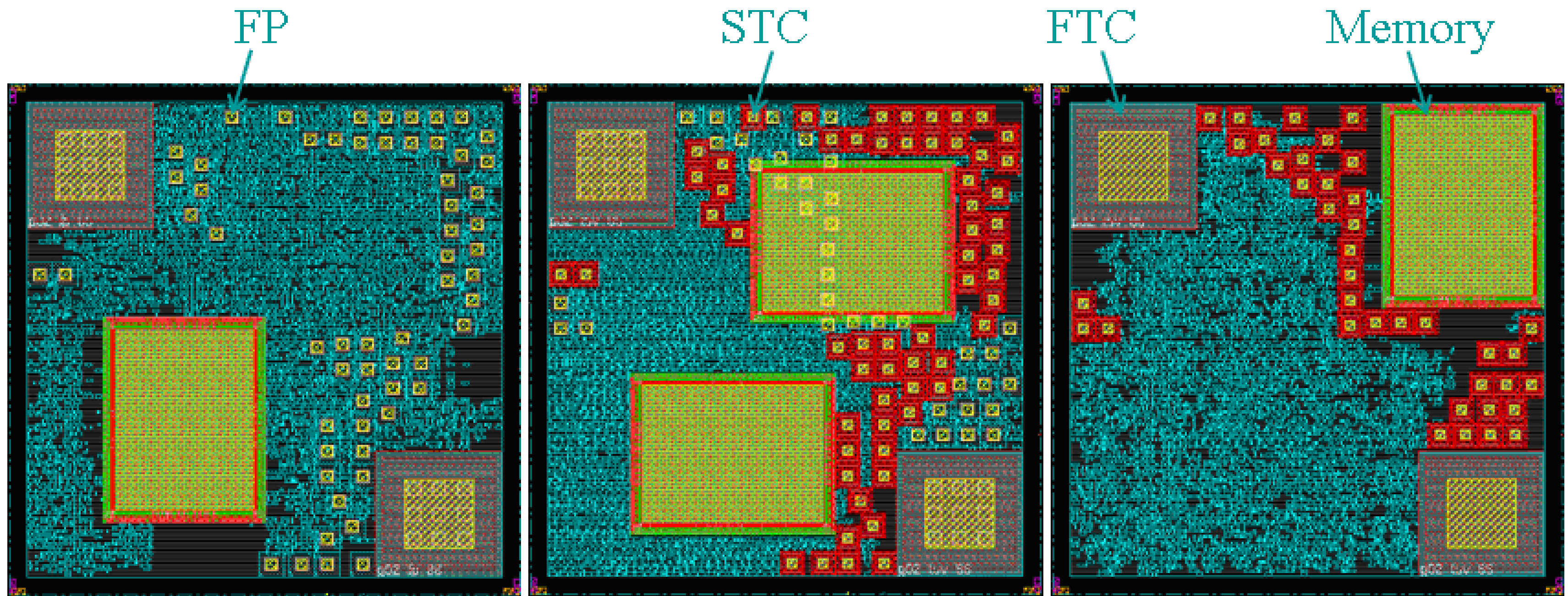


# Multi-Tier Balanced CTS



# 3-Tier Case with Power TSV

- Support 2 kinds of TSV diameters
  - 5um Signal , 50um Power/Ground




(a) Bottom Tier (b) Middle Tier (c) Top Tier

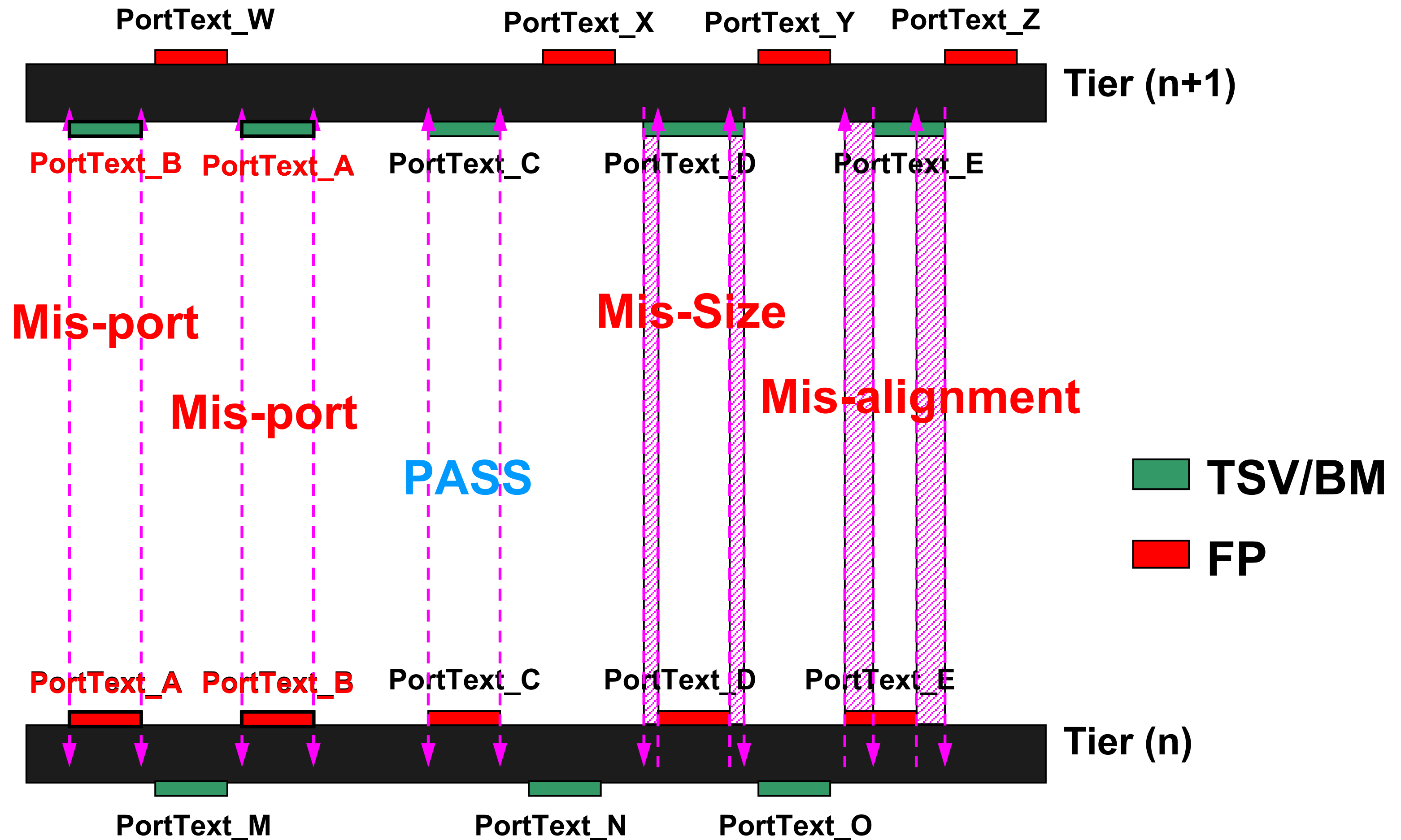
# Clock Tree Synthesis Results

| Unit: ns | Tier | CTS Max Latency | CTS Min Latency | CTS Inter-Tier Skew | Multi-Tier Balanced CTS Max Latency | Multi-Tier Balanced CTS Min Latency | Multi-Tier Balanced CTS Inter-Tier Skew | ΔSkew |
|---|---|---|---|---|---|---|---|---|
| 2 Tiers | 2 | 0.252 | 0.252 | 0.296 | 0.252 | 0.252 | 0.008 | -0.288 |
| | 1 | 0.111 | 0.104 | | 0.351 | 0.344 | | |
| 3 Tiers | 3 | 0.401 | 0.386 | 0.608 | 0.369 | 0.35 | 0.05 | -0.558 |
| | 2 | 0.395 | 0.381 | | 0.545 | 0.531 | | |
| | 1 | 0.323 | 0.298 | | 0.68 | 0.657 | | |
| 4 Tiers | 4 | 0.635 | 0.624 | 1.546 | 0.627 | 0.614 | 0.245 | -1.301 |
| | 3 | 0.54 | 0.518 | | 0.999 | 0.985 | | |
| | 2 | 0.651 | 0.625 | | 1.343 | 1.314 | | |
| | 1 | 0.268 | 0.256 | | 1.282 | 1.27 | | |

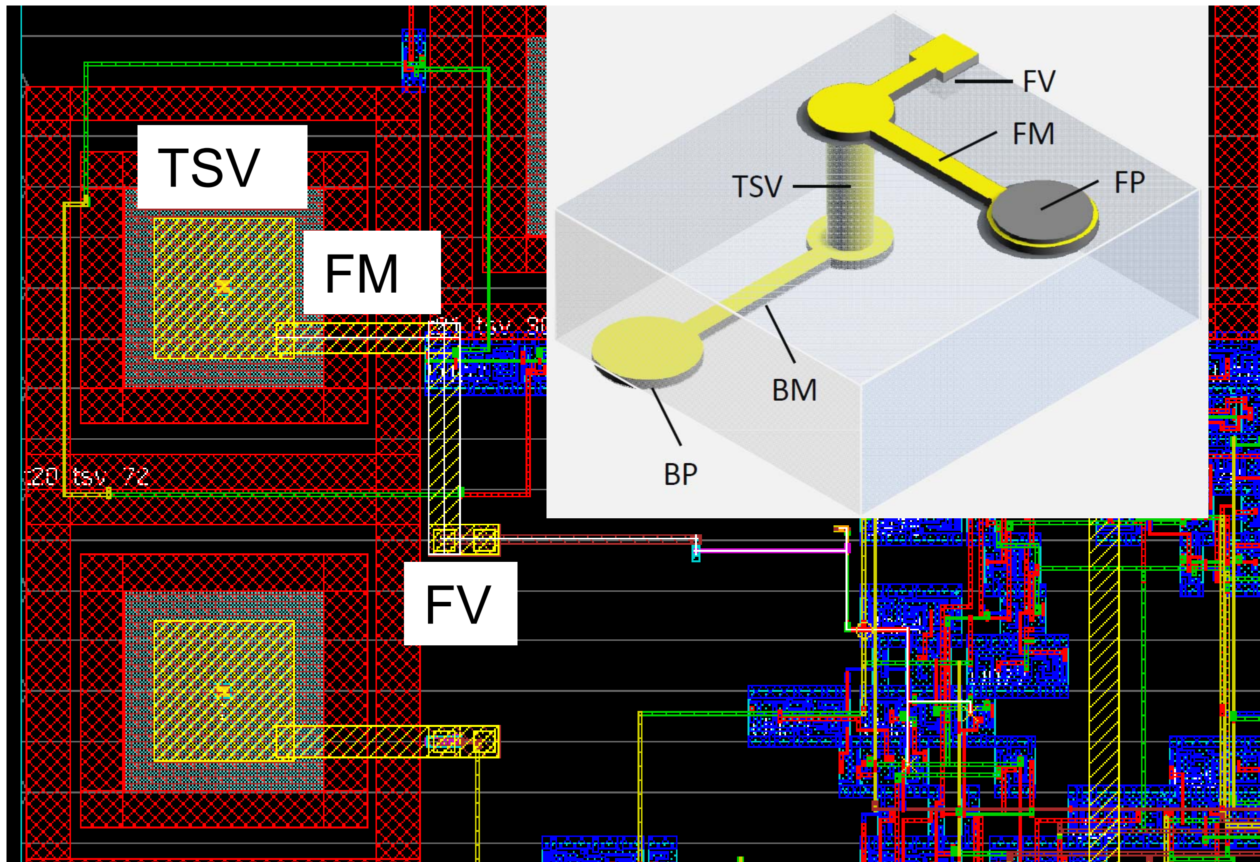
# Routing – DRC/LVS

- Design rules are provided for the five extra mask layers
- 3D LVS need to evolve to tackle the vertical interconnect issues across tiers

# Different LVS Checking Types



# BEOL & FM Routing



# Outline

- Introduction to 3D Integration
- 3D CAD Reference Flow in ITRI
- Conclusions

# Conclusions

- Multi-Tier P&R Methodology
  - TSV co-placement
  - Via alignment constraints
  - Balanced CTS
  - DRC/LVS
- Future works on 3D Integration
  - Thermal
  - Mechanical

# THANKS FOR YOUR ATTENTION

# 謝謝您的聆聽