4B-2

Symmetry-Aware TCG-Based Placement Design under Complex Multi-Group Constraints for Analog Circuit Layouts

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Outline

- *Introduction*
- Prior Work
- Symmetric-feasible TCG
- Symmetric Packing
- Symmetric-feasible TCG perturbation
- Experimental Results
- Conclusions

Analog Placement

- Placement problem
  (1) Problem definition
  (2) Goal
- Symmetric constraint
  (1) Sensitive cells placed on opposite sides
  (2) Reduce the effect of parasitic mismatches
  (3) Reduce the circuit sensitivity

Symmetric Constraints

- Symmetric types
  - Symmetric pair cell
  - Self symmetric
  - Symmetric group
- Flow
  - Perturb
  - Packing
  - Simulate annealing
- Comparison
  - performance
  - time complexity of perturbation
  - time complexity of packing

Our Contributions

Our Contributions

- (1)introduce conditions to verify the symmetric feasibility of TCG enclosing multiple groups;
- (2) propose an efficient contour-based packing scheme;
- (3) a set of random perturbation operations with time complexity of O(n) is defined.

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Prior Work

- Previous placement applications

  -SP

  -Transitive closure graph (TCG)

  -TCG-S

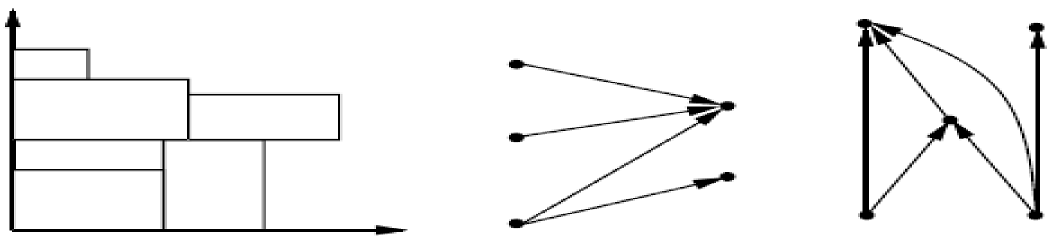
  -O-tree

  -B-tree

  -HB*-tree

Prior Work

- TCG



- SP

  Uses an ordered pair of sequence which is α- and β-sequence to encode the placement .The topological relationship between two cells *a* and *b* can be derived from an SP:

•if $\alpha_a^{-1} < \alpha_b^{-1}$ and $\beta_a^{-1} < \beta_b^{-1}$, then cell *a* is to the left of cell *b*;

•if $\alpha_a^{-1} < \alpha_b^{-1}$ and $\beta_b^{-1} < \beta_a^{-1}$, then cell *a* is on the top of cell *b*,

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Symmetric feasible conditions

Let (G_h, G_v) be the TCG representation of a placement containing two symmetry groups Γ and Φ. For the multi-group situation, we can define the following conditions.

Definition 1: For $(a, a') \in \Gamma$, $(b, b') \in \Gamma$, $(c, c') \in \Phi$, and $(d, d') \in \Phi$, a TCG representation is symmetric-feasible if the following four conditions are satisfied. For intra-group of Γ (the same for Φ)

in G_h : $a \vdash b \langle\neq\rangle a' \vdash b'$; (1)

in G_v : $a \perp b \langle\neq\rangle b' \perp a'$; (2)

For inter-group between Γ and Φ

in G_h : $a \vdash c$ and $a' \vdash c' \langle\neq\rangle d \vdash b$ and $d' \vdash b'$; (3)

in G_v : $a \perp c \langle\neq\rangle c' \perp a'$; (4)

where ‹≠› denotes the two cases before and after this symbol cannot simultaneously appear in the same TCG.

Symmetric feasible conditions

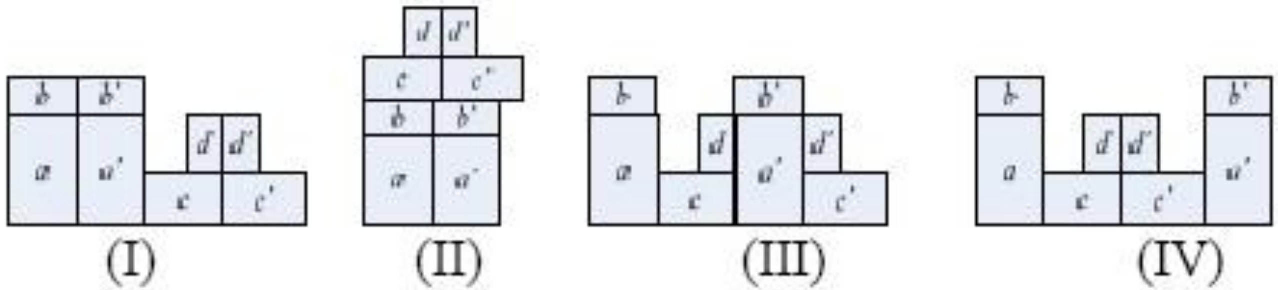

Fig. 1. (I) group Γ is placed at the left of group Φ; (II) Γ is placed below Φ; (III) Γ and Φ are intermingled; (IV) Φ is placed within Γ

- **Lemma**: Any placement containing multiple symmetry groups can be represented with a symmetric-feasible TCG.

Symmetric TCG

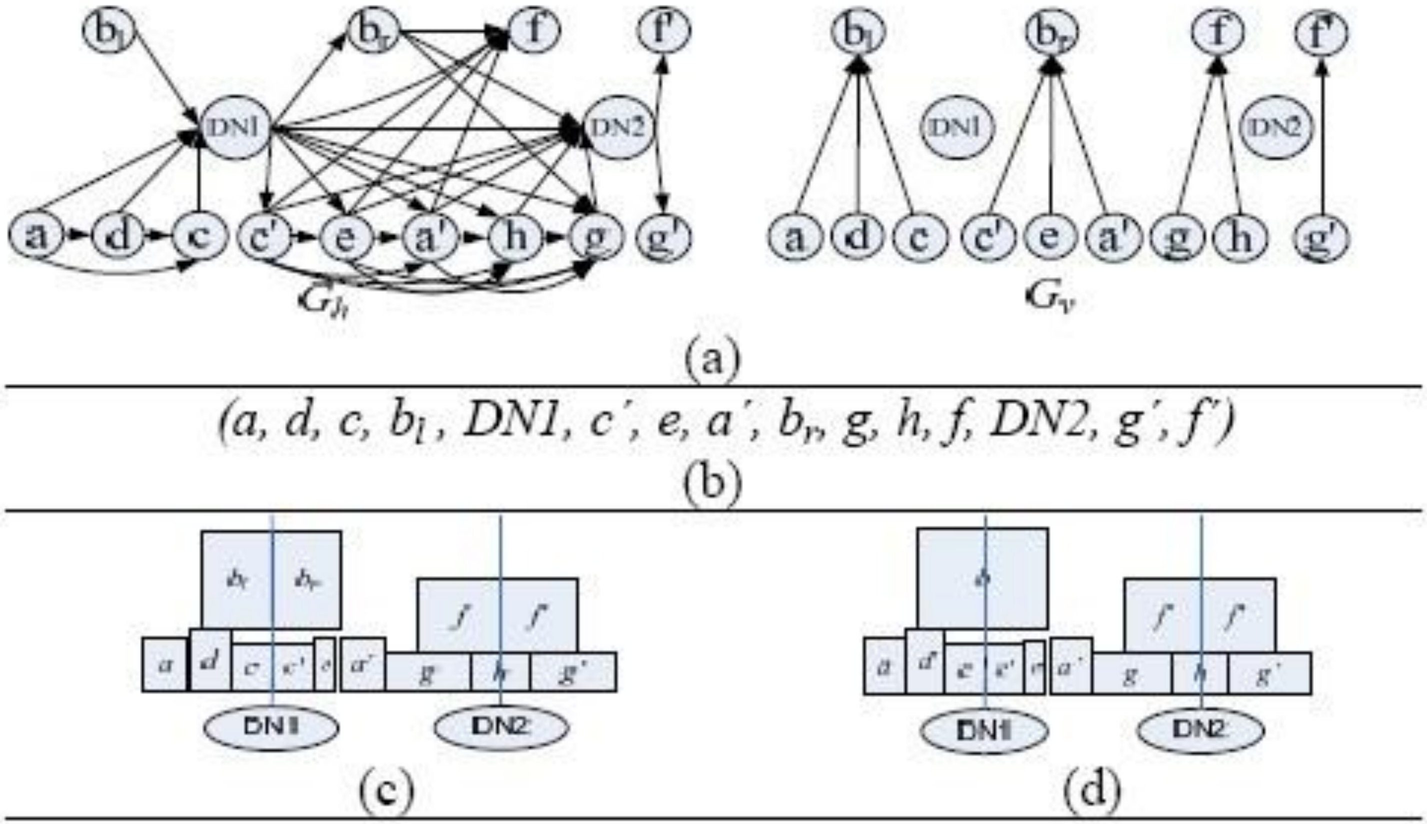

Fig. 2. (a) TCG; (b) topological order; (c) symmetric placement with separate self-symmetric halves; (d) final symmetric placement

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Symmetric Packing Flow

Begin

1 Construct the topological order of the TCG;

2 Generate *packSeq*, which contains only the symmetric cells;

3 Use the dummy axis cells to separate *packSeq* into sub-sequences;

4 Create a *list* made up of the sub-sequences;

5 Do *initial packing* for the first sub-sequence, update the axis position X_{axis};

6 **For** (the *list* is not empty)

7   Do *initial packing* for the second sub-sequence;

8   Follow *packSeq* one by one. Compare the Y coordinates of each two cells in one symmetric pair such as (a, a'), and make $Y_a = Y_{a'} = max(Y_a, Y_{a'})$ and shift the packing symmetric cells that have vertical relationship with the shifted cells;

9   Follow *packSeq* one by one, for every two cells in one symmetric pair such as (a, a'); calculate $\Delta X_a=|X_a-X_{axis}|$ and $\Delta X_{a'} =|X_{a'}-X_{axis}|$. Then shift one symmetric cell to make $\Delta X_a= \Delta X_{a'} = max\ (\Delta X_a, \Delta X_{a'})$. Also tune-up the corresponding cells with the same ΔX_a;

10   Do final packing for the first and second sub-sequences;

11   Remove the first sub-sequence from the sub-sequence *list*;

12 **End for**

13 Consider all symmetric cells as preplaced cells and final-pack the whole sequence;

14 Post-process self-symmetric cells to merge two split parts to one unit;

End

Fig. 3. Symmetric packing flow

Symmetric Packing

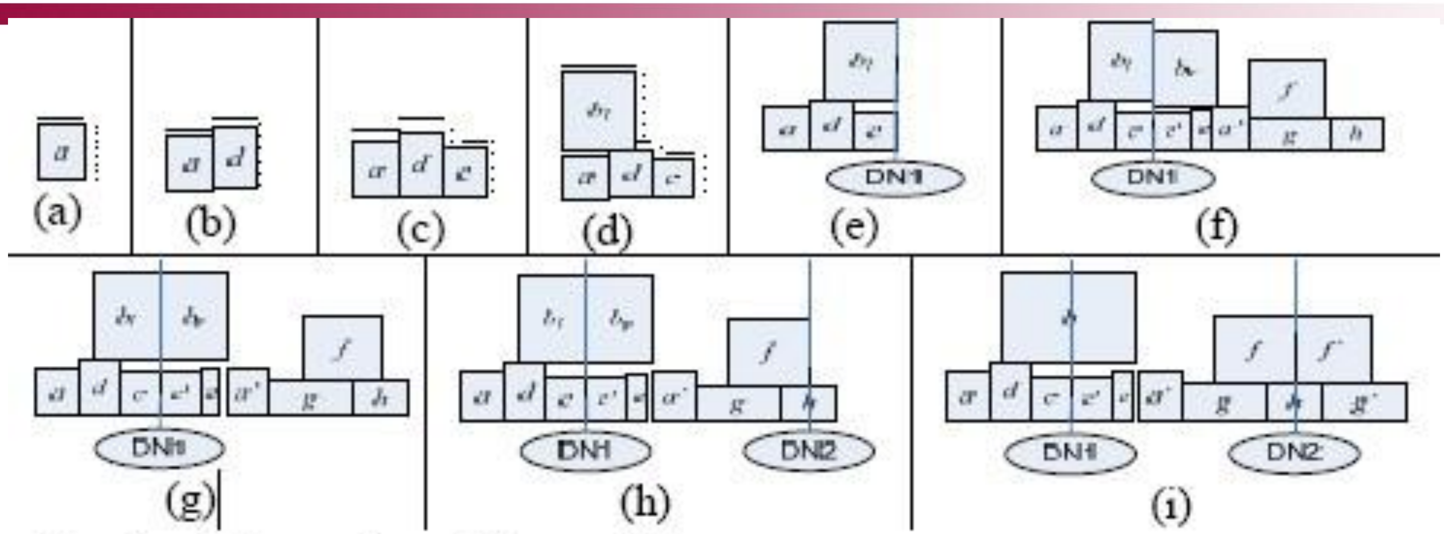

Fig. 4. Examples of the packing

- Step 1:packing preparation; Step 2:initial packing (a-d); Step 3:tune-up operation on symmetric cells (f-h); Step 4:final packing (i)
- Two Schemes : (1)general flow (2) simplified flow
- Complexity is $O(g \cdot m \cdot lgm)$.
- **Lemma**: Any symmetric-feasible TCG containing multiple symmetry groups can be packed to a symmetric placement in polynomial time.

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Symmetric TCG Perturbation

A. Cluster Edge Move-Reverse and Edge Move Operations

- in-in (in-out) degree
- in-in (or in-out) cluster
- Cluster edge move-reverse (or cluster edge move) operation

- All the operations in part B can be done with Cluster edge move-reverse (or cluster edge move) operation.

- **Lemma**: Without losing TCG transitive-closure property, the topological relationship between any two vertices in a TCG can be modified by a cluster edge move or cluster edge move-reverse operation, which takes $O(n)$ time.

Symmetric TCG Perturbation

B. Five Perturbation Operations

- Vertex Rotation
- Symmetric Swap

  This operation is that one vertex in a symmetric pair swaps position with its symmetric counterpart.
- Symmetric-Cell Move

  This operation is to change the horizontal or vertical relationship between symmetric vertices within one symmetry group or from different symmetry groups.
- Asymmetric-Cell Move

  This operation is to perturb the topology relationship between an asymmetric vertex and other vertices.
- Symmetry-Group Move

Symmetric TCG Perturbation

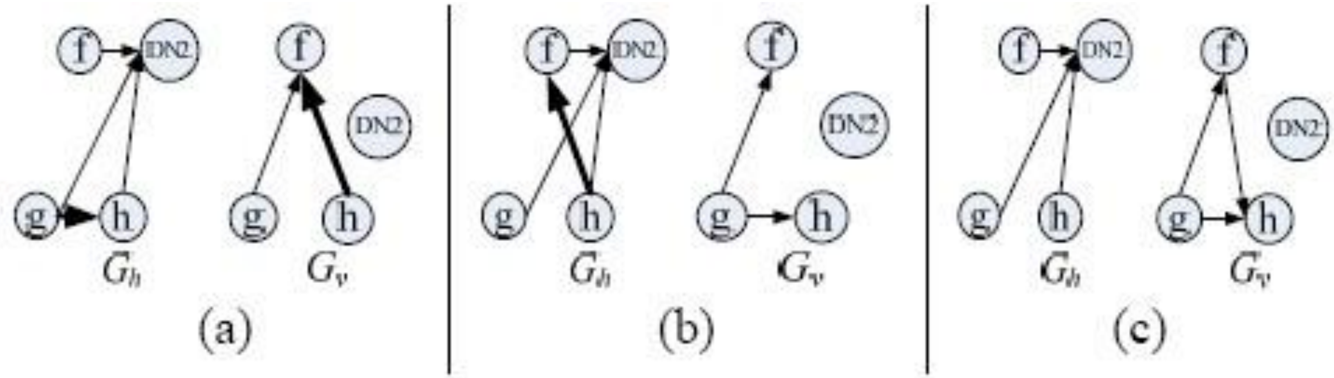

Fig. 6. Example of asymmetric move

Theorem 1: Using operations above, the solution space of the symmetric-feasible TCGs can be fully explored. Each operation takes at almost *O(n)* time, where *n* is the number of cells.

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Experimental Results

- We implement this symmetry TCG scheme based on a simulated annealing algorithm. The program was coded in C++ under Linux operating system and tested on a 2.1 GHz PC with several benchmarks.
- Our cost function for evaluation is obtained from the following equation:

$$Cost = \alpha_{area} \cdot Area + \sum_i \beta_i \; WireLength_i$$

- Test Cases

(1) MCNC benchmarks

(2) biasynth_2p4g of 65 cells and lnamixbias_2p4g of 110 cells

(3) modified 65 cells and 110 cells, OTA

Experimental Results

I.MCNC BENCHMARKS

Circuit	cells	groups		*Abs*	*SP*	*SPWD*	*SP+LP*	*HB*-tree*	*S-TCG-1*	*S-TCG-2*
apte	9	2	Cost	120.7%	112.2%	107.7%	106.4%	101.2%	100.0%	50.74
			Time	1000%	767%	466.7%	400.0%	100%	119%	3
ami33	33	2	Cost	118.9%	109.3%	108.5%	107.4%	103.7%	99.0%	1.33
			Time	1670%	1190%	243.4%	354.8%	83.8%	121%	62
ami49	49	2	Cost	129.1%	107.9%	108.7%	107.1%	102.5%	99.2%	42.21
			Time	2250%	1360%	201.0%	228.0%	90.4%	118%	107

II.CIRCUIT TEST

Circuit	cells	groups		*Abs*	*SP*	*SPWD*	*SP+LP*	*HB*-tree*	*S-TCG-2*
biasynth _2p	65	3	Cost	127%	109.8%	107.4%	104%	102.1%	5.42
			Time	2150%	611%	154%	221%	89.3%	131
lnamixbias _ 2p	110	5	Cost	119%	114.6%	109%	109%	103.2%	51.41
			Time	2430%	1130%	543%	920%	82.5%	287
mod_ biasynth	65	3	Cost	123%	107.8%	107.1%	106%	104.2%	5.53
			Time	2137%	621%	153%	224%	88.5%	144
mod_lnami xbias_	110	5	Cost	120%	114.1%	111%	110%	105.1%	52.23
			Time	2440%	1110%	572%	934%	86.3%	294
OTA	69	5	Cost	119%	114.9%	107.2%	105%	105.5%	27.53
			Time	2084%	724%	167%	207%	90.4%	263

Experimental Results

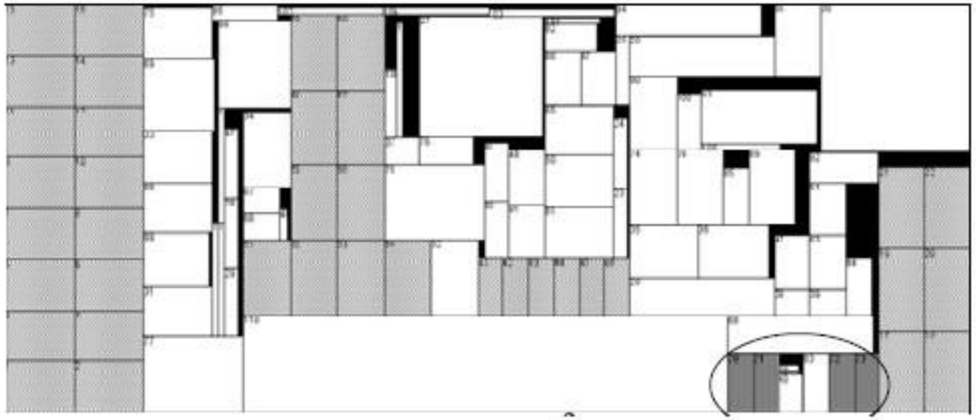

Fig. 7. Final placement of circuit lnamixbias_2p4g

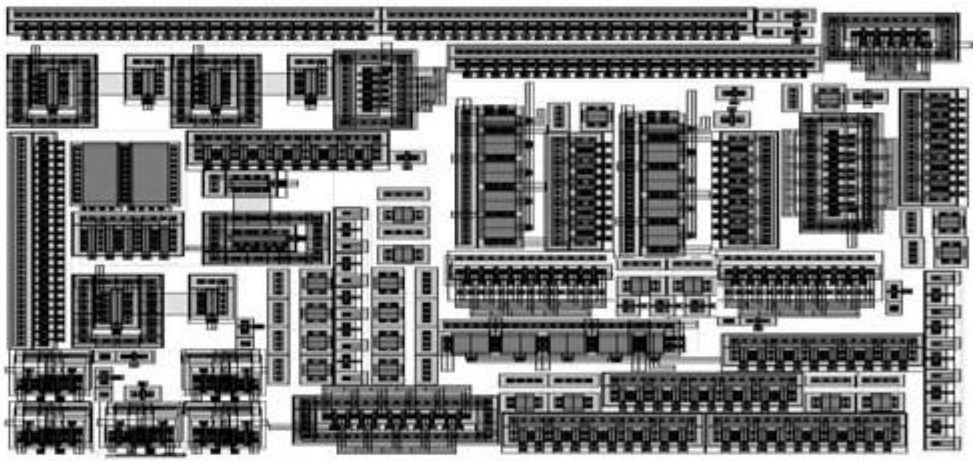

Fig. 8. Final placement of circuit OTA

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Conclusions

- In this paper, we introduce a scheme to handle the symmetric constraints in the analog layout placement.
  - An efficient perturbation strategy was proposed to achieve random state conversion in *O(n)* time without losing TCG symmetric-feasibility and validity.
  - Although the HB*-tree scheme slightly outperforms our approach in terms of area in some larger circuits, our proposed approach is able to cover any placement configurations.

Thank you

and

Questions?