Technology Mapping with Crosstalk Noise Avoidance

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Outline

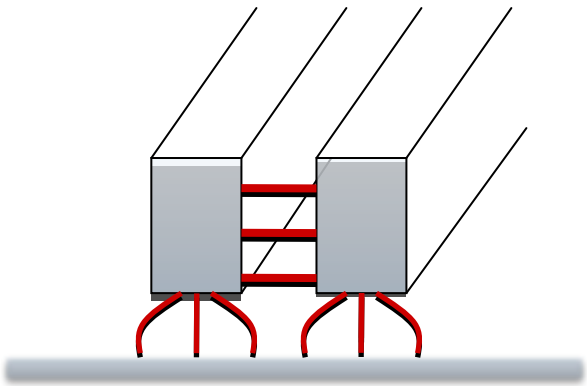
- Introduction
- Preliminaries
- Proposed algorithm
- Experimental results
- Conclusions

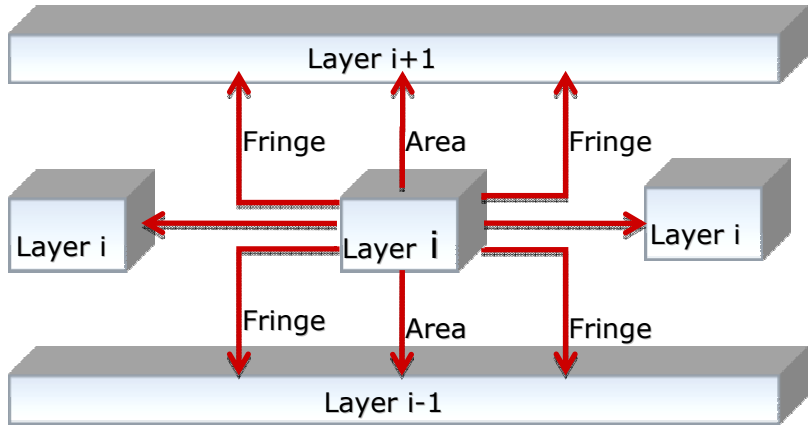
Introduction

- Advanced technology scaling

  → wires become taller and thinner with smaller spacing and higher sidewalls

- Crosstalk effects between interconnection wires become more significant

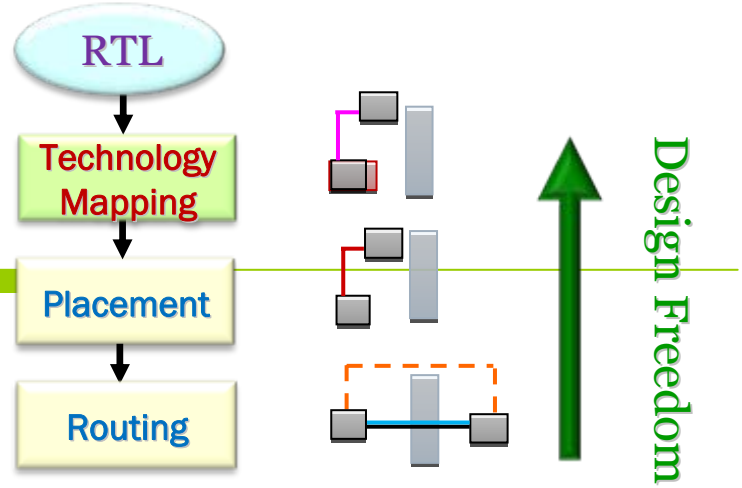




Previous efforts in crosstalk minimization

- Crosstalk avoidance in different design stages
  - At post routing
    - Uses gate sizing, transistor sizing and wire sizing
  - At global routing
    - A global router with crosstalk model by Lagrangian relaxation — Hai Zhou, TCAD 1999
    - Introduces an estimated, congestion-based pre-routing noise analysis — Murat R. Becer et al., ISQED'02
  - At placement
    - A crosstalk- aware placement — Jinan Lou et al., IEEE Design & Test2004

Motivation



- Considering crosstalk in technology mapping stage
  - Challenges : fidelity of routing estimation
  - A simple crosstalk model with predictive layout information
- Design Freedom
  - Supplying freedom to circuits
  - Technology mapping decides cells and routing
- Recent works in technology mapping
  - Targeting routing congestion
  - A congestion map with probabilistic method

Our contributions

- From the predictive information of pre-placement and pre-routing, we construct a reliable crosstalk model in technology mapping.
- According to our results, the crosstalk in post-routing analysis is indeed decreased by our crosstalk-aware technology mapping.
  - A matching procedure with two-dimensional coupling capacitance map.
  - The cost function sensitive to congestion and crosstalk is easy to extend other objectives, like area and power.

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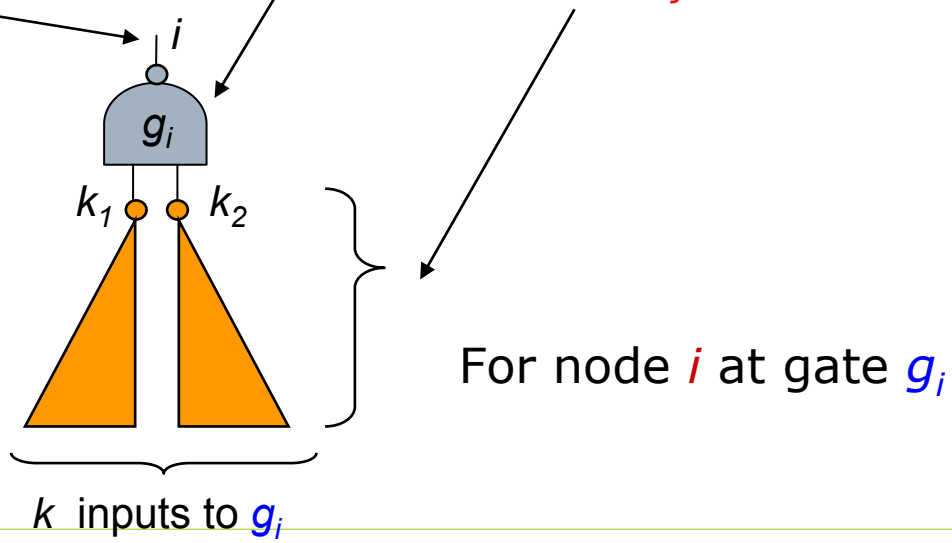
Traditional technology mapping(1/2)

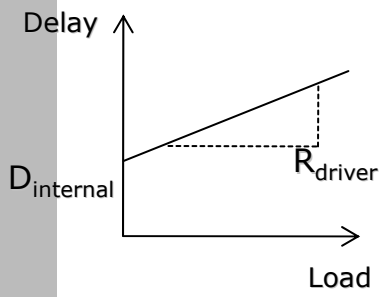
- Minimize area
- Cover each tree optimally using *dynamic programming*

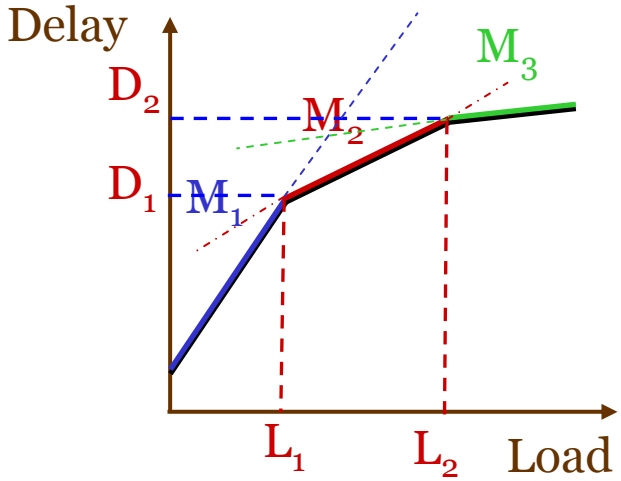
$$cost(i) = min_k\{cost(g_i) + \sum_k cost(k_j)\}$$

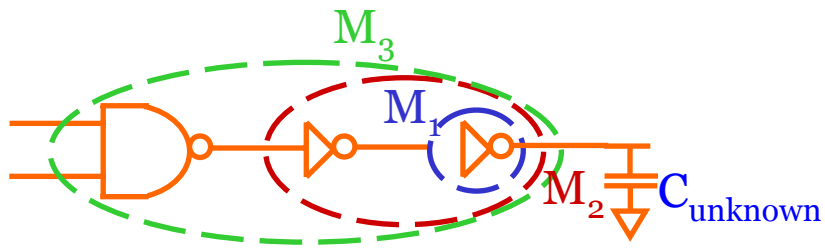


Traditional technology mapping(2/2)

- Generates delay-optimal match solutions
- Unknown output load in matching phase
- Stores the *load-delay curve* containing delay-optimal matches in each range of load, called non-inferior matches





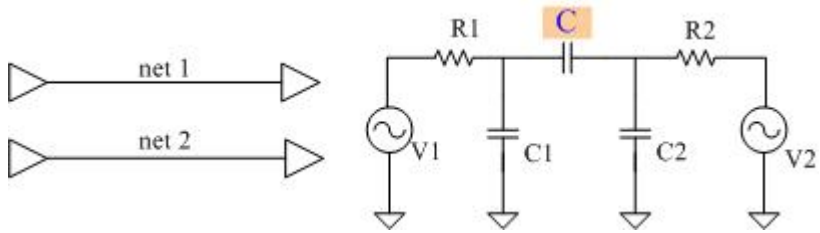


E. M. Sentovich et al., "SIS: A system for sequential circuit synthesis", May 1992

Crosstalk model(1/2)

- Assumes that only the coupling capacitance is controllable in layout design
- Models all parameters except coupling capacitance by a *crosstalk coefficient* e_{ij} for each net *i* from net *j*
- The total crosstalk on one net *i*

$$Xtalk_i = \sum_{j \neq i} e_{ij} C_{ij}$$



Hai Zhou and D.F. Wong, "Global routing with crosstalk constraints" IEEE Transactions on Computer-Aided Design, pp. 1683-1688, Nov. 1999

Crosstalk model(2/2)

- Assuming coupling capacitance only exists between neighboring parallel wires by the following form:

$$C = \alpha \frac{length}{distance^{\beta}} \qquad \beta \approx 2$$

  - *distance* – the distance of two adjacent net
  - *length* – the parallel length of two adjacent net

Problem formulation

- Given a subject graph of a network and a library of gates, generate a mapped netlist which could minimize crosstalk noise effects based on a reliable crosstalk model under specified delay constraints

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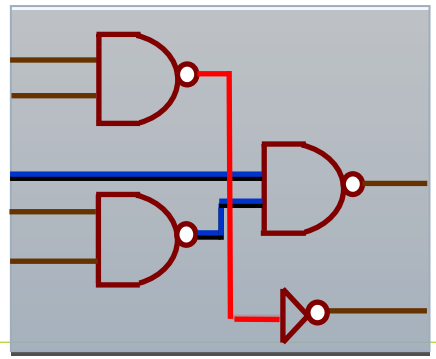
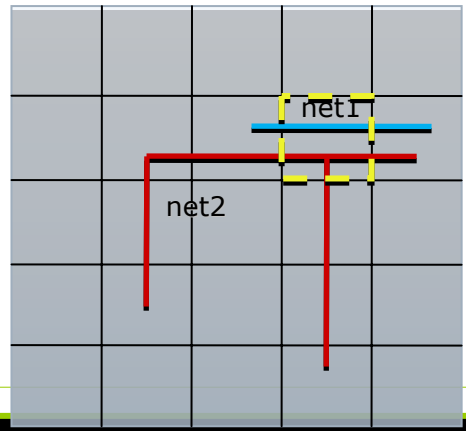
Algorithm overview(1/3)

- Challenges in estimating crosstalk in technology mapping
  - Coupling capacitance requires routing of interconnections
  - Unlike delay, crosstalk cannot be computed by incrementally





Algorithm overview(2/3)

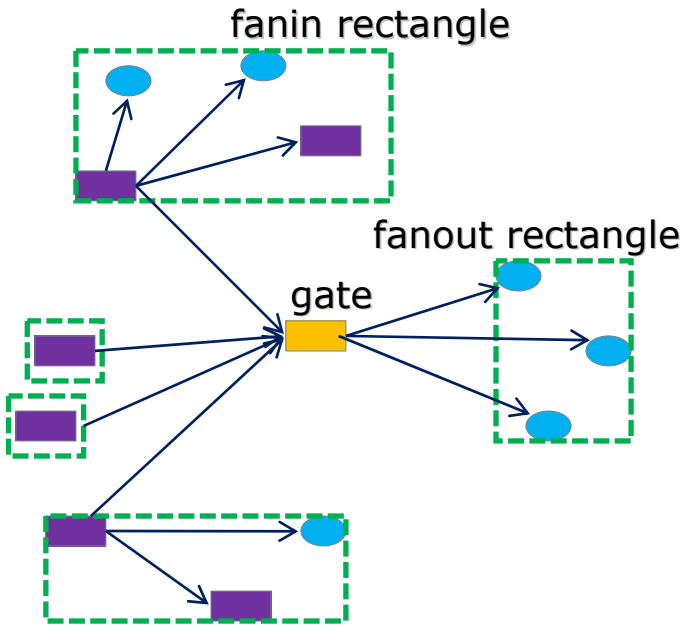
- Solutions overview
  - A quick pattern-based global router to estimate routing topology
  - Defers crosstalk computation to covering phase
  - Requires virtual routing map to capture all wires in mapping solutions

Our approach

- Technology mapping with structural approach
  - Contains load–delay curve for delay model
- The matching phase
  - Employs a companion placement
  - Determines routing net for each match
- The covering phase
  - Generates connection information of whole map
  - Estimates crosstalk

The matching phase — A companion placement

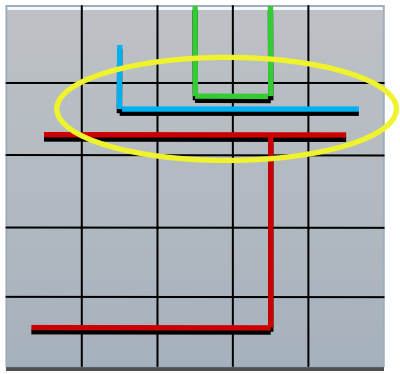
- A placer integrated in technology mapping
- Places the base functions on a layout image
- Updates the new position for the mapped gate by a easy estimated option
- Computes the center point of its fanin /fanout rectangles' points

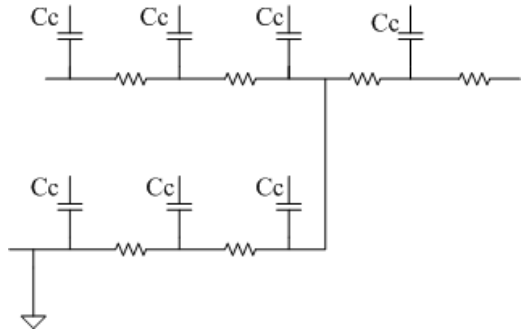


M. Pedram and N. Bhat. "Layout driven technology mapping" DAC, 1991

The covering phase — Crosstalk map

- After placement and routing by a point model, construct crosstalk map for each fanin net on a match
  - a point model– a center point (x,y) represents the location of gate pins and its position





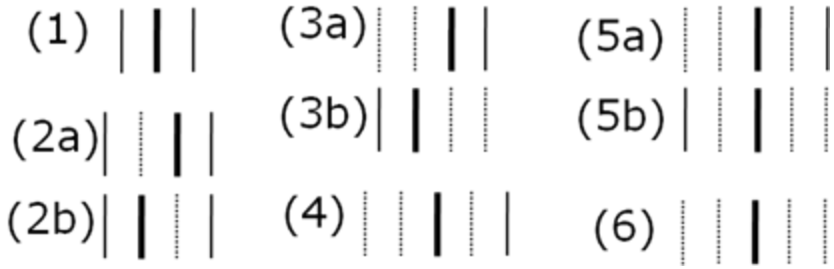
Coupling capacitance model in vertical direction on a net

Probabilistic extraction(1/2)

- In order to predict track utilization, use probabilistic extraction method
- Assumptions:
  - Capacitance values of a net only by the location of the nearest neighboring nets.
  - Ignore the coupling effect of a neighboring net more than two tracks.

M.Becer et al. "Pre-route Noise Estimation in Deep Submicron Integrated Circuits, " ISQED'02, 2002

Six configurations



Probabilistic extraction(2/2)

- Weight the capacitance values of each configuration by the probability of the configuration

$$total\_configurations = \binom{n}{k} k!$$

$$coupling\_cap_{total(i)} = coupling\_cap_{(i)} \times \frac{conf_{(i)}}{total\_configurations}$$

- Sum the weighted contributions for all configurations and scale the per unit length values with the length of the net segment.

Cost function

- The complete virtual routing map
  - The delay optimal matches of primary outputs
  - Update the transitive fanin cone of each match
- Cost function

$$cost = \alpha \cdot crosstalk + \beta \cdot overflow$$

  - Coupling capacitance of each match's fanin net
  - Total track overflow: a global view

$$OF = \sum_{\forall T^{bin} > 0} T^{bin}$$

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Experimental setup(1/2)

- Mapping algorithm incorporated in SIS
  - Technology files in UMC 90 nm process
  - Library: enhanced lib2.genlib with up to 4 strengths for each gate
- ISCAS'85 benchmarks
- Capo for pre-placement
- Placement and routing in Cadence's SoC Encounter
- Timing and noise analysis in *CeltIC* of Encounter

Experimental setup(2/2)

- SIS is modified to use pre-placement to compute wire delay and wire load
- Constraints setting
  - Timing constraints: from delay mode in SIS, extend 15% of the timing constraints
  - Set core utilization as 0.8 at placement in SoC Encounter

Experimental results(1/3)

- SIS: original SIS with companion placement
- Ours: crosstalk-aware technology mapping

	Area (um^2)			number of cells		Delay (ps)		
	SIS	Ours	increase	SIS	Ours	SIS	Ours	Increase
C432	616 .56	650.92	5.6%	178	212	1126	1252	11.2%
C499	1418.26	1572.67	10.9%	371	430	856	914	6.8%
C880	1145.78	1331.82	16.2%	295	366	1162	1321	13.7%
C1355	1447.36	1536.57	6.1%	381	420	888	958	7.8%
C1908	1380.33	1425.31	3.3%	371	475	1271	1311	3.1%
C2670	1924.59	1967.85	2.2%	472	493	863	903	4.6%
C3540	3545.70	4174.23	17.7%	911	1154	1610	1797	11.6%
C5315	4211.55	4161.46	-1.2%	1003	985	1055	1162	10.1%
C6288	8353.50	9404.11	12.5%	2161	2590	4653	4689	0.7%
C7552	6389.44	6424.59	0.6%	1668	2023	1965	1629	-17.1%
average			7.39%					5.25%

Experimental results(2/3)

	Total net		Receiver peak		Xtalk_Ratio(%)		Improve–ment(%)	Run_time (s)	
	SIS	Ours	SIS	Ours	SIS	Ours		SIS	Ours
C432	218	229	37	27	16.97	11.79	43.95	6	7
C499	416	485	93	72	22.36	14.85	50.59	12	13
C880	359	431	71	62	19.78	14.39	37.48	28	30
C1355	426	465	73	72	17.14	15.48	10.67	23	26
C1908	408	526	107	92	26.23	21.6	21.44	21	26
C2670	709	730	135	117	19.05	16.02	18.80	22	26
C3540	965	1208	131	122	13.58	10.10	34.42	33	45
C5315	1185	1167	159	147	13.42	12.59	6.52	47	52
C6288	2197	2626	130	110	5.92	4.18	41.26	78	163
C7552	1879	1880	154	135	8.20	7.18	14.13	64	72
average	--	--			16.26	12.82	27.93	--	--

Experimental results(3/3)

- Summary of results
  - Crosstalk performance: 28% improvement
  - Delay : 5% worse
  - Area : 7% worse
  - Run-time : 1.4x worse, but still practical

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Conclusions

- We propose a new method estimating the crosstalk information in the technology mapping
- Crosstalk can be reduced in technology mapping with affordable increase in area and delay
- From our framework, it can easily be extended to other objectives, such as power or temperature

Thank you for your attention