Technology Mapping with Crosstalk Noise Avoidance

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Outline

- Introduction
- Preliminaries
- Proposed algorithm
- Experimental results
- Conclusions
Introduction

- Advanced technology scaling
  - wires become taller and thinner with smaller spacing and higher sidewalls
- Crosstalk effects between interconnection wires become more significant
Previous efforts in crosstalk minimization

- Crosstalk avoidance in different design stages
  - At post routing
    - Uses gate sizing, transistor sizing and wire sizing
  - At global routing
    - A global router with crosstalk model by Lagrangian relaxation
      - Hai Zhou, TCAD 1999
    - Introduces an estimated, congestion-based pre-routing noise analysis
      - Murat R. Becer et al., ISQED’02
  - At placement
    - A crosstalk-aware placement
      - Jinan Lou et al., IEEE Design & Test2004
Motivation

- Considering crosstalk in technology mapping stage
  - Challenges: fidelity of routing estimation
  - A simple crosstalk model with predictive layout information
- Design Freedom
  - Supplying freedom to circuits
  - Technology mapping decides cells and routing
- Recent works in technology mapping
  - Targeting routing congestion
  - A congestion map with probabilistic method
Our contributions

- From the predictive information of pre-placement and pre-routing, we construct a reliable crosstalk model in technology mapping.

- According to our results, the crosstalk in post-routing analysis is indeed decreased by our crosstalk-aware technology mapping.
  - A matching procedure with two-dimensional coupling capacitance map.
  - The cost function sensitive to congestion and crosstalk is easy to extend other objectives, like area and power.
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- Introduction
- **Preliminaries**
- Proposed Algorithm
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Traditional technology mapping (1/2)

- Minimize area
- Cover each tree optimally using *dynamic programming*

\[
\text{cost}(i) = \min_k \{ \text{cost}(g_i) + \sum_k \text{cost}(k_j) \}
\]

For node \(i\) at gate \(g_i\)

- \(k\) inputs to \(g_i\)
Generates delay-optimal match solutions
- Unknown output load in matching phase
- Stores the *load-delay curve* containing delay-optimal matches in each range of load, called non-inferior matches

Crosstalk model (1/2)

- Assumes that only the coupling capacitance is controllable in layout design
- Models all parameters except coupling capacitance by a crosstalk coefficient \( e_{ij} \) for each net \( i \) from net \( j \)
- The total crosstalk on one net \( i \)

\[
X_{talk_i} = \sum_{j \neq i} e_{ij} C_{ij}
\]

Crosstalk model (2/2)

- Assuming coupling capacitance only exists between neighboring parallel wires by the following form:

\[ C = \alpha \frac{\text{length}}{\text{distance}^\beta} \quad \beta \approx 2 \]

- \textit{distance} – the distance of two adjacent net
- \textit{length} – the parallel length of two adjacent net
Problem formulation

- Given a subject graph of a network and a library of gates, generate a mapped netlist which could minimize crosstalk noise effects based on a reliable crosstalk model under specified delay constraints
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Algorithm overview (1/3)

- Challenges in estimating crosstalk in technology mapping
  - Coupling capacitance requires routing of interconnections
  - Unlike delay, crosstalk cannot be computed by incrementally
Algorithm overview (2/3)

- Solutions overview
  - A quick pattern-based global router to estimate routing topology
  - Defers crosstalk computation to covering phase
  - Requires virtual routing map to capture all wires in mapping solutions
Our approach

- Technology mapping with structural approach
  - Contains load–delay curve for delay model
- The matching phase
  - Employs a companion placement
  - Determines routing net for each match
- The covering phase
  - Generates connection information of whole map
  - Estimates crosstalk
The matching phase — A companion placement

- A placer integrated in technology mapping
- Places the base functions on a layout image
- Updates the new position for the mapped gate by an easy estimated option
- Computes the center point of its fanin/fanout rectangles’ points

The covering phase — Crosstalk map

- After placement and routing by a point model, construct crosstalk map for each fanin net on a match
  - a point model—an center point (x,y) represents the location of gate pins and its position

Coupling capacitance model in vertical direction on a net
Probabilistic extraction (1/2)

- In order to predict track utilization, use probabilistic extraction method.

- Assumptions:
  - Capacitance values of a net only by the location of the nearest neighboring nets.
  - Ignore the coupling effect of a neighboring net more than two tracks.


Six configurations

1. \( \begin{array}{c|c|c|c|c|c|c} \end{array} \)
2. \( \begin{array}{c|c|c|c|c|c|c} \end{array} \)
3. \( \begin{array}{c|c|c|c|c|c|c} \end{array} \)
4. \( \begin{array}{c|c|c|c|c|c|c} \end{array} \)
5. \( \begin{array}{c|c|c|c|c|c|c} \end{array} \)
6. \( \begin{array}{c|c|c|c|c|c|c} \end{array} \)
Probabilistic extraction (2/2)

- Weight the capacitance values of each configuration by the probability of the configuration

\[
total \_configurations = \binom{n}{k} k!
\]

\[
coupling \_cap_{total(i)} = coupling \_cap_{(i)} \times \frac{conf_{(i)}}{total \_configurations}
\]

- Sum the \textit{weighted contributions} for all configurations and scale the per unit length values with \textit{the length of the net} segment.
Cost function

- The complete virtual routing map
- The delay optimal matches of primary outputs
- Update the transitive fanin cone of each match

Cost function

\[ \text{cost} = \alpha \cdot \text{crosstalk} + \beta \cdot \text{overflow} \]

- Coupling capacitance of each match’s fanin net
- Total track overflow: a global view

\[ \text{OF} = \sum_{T^{bin} > 0} T^{bin} \]
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Experimental setup (1/2)

- Mapping algorithm incorporated in **SIS**
  - Technology files in UMC 90 nm process
  - Library: enhanced *lib2.genlib* with up to 4 strengths for each gate
- ISCAS’85 benchmarks
- Capo for pre-placement
- Placement and routing in Cadence’s SoC Encounter
- Timing and noise analysis in *CeltIC* of Encounter
Experimental setup (2/2)

- SIS is modified to use pre-placement to compute wire delay and wire load

- Constraints setting
  - Timing constraints: from delay mode in SIS, extend 15% of the timing constraints
  - Set core utilization as 0.8 at placement in SoC Encounter
Experimental results (1/3)

- **SIS**: original SIS with companion placement
- **Ours**: crosstalk-aware technology mapping

<table>
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<th>Delay (ps)</th>
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### Experimental results (2/3)

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<th>Receiver peak</th>
<th>Xtalk_Ratio(%)</th>
<th>Improvement(%)</th>
<th>Run_time (s)</th>
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2010/2/1
Experimental results (3/3)

- Summary of results
  - Crosstalk performance: 28% improvement
  - Delay: 5% worse
  - Area: 7% worse
  - Run-time: 1.4x worse, but still practical
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Conclusions

- We propose a new method estimating the crosstalk information in the technology mapping.
- Crosstalk can be reduced in technology mapping with affordable increase in area and delay.
- From our framework, it can easily be extended to other objectives, such as power or temperature.
Thank you for your attention