Adaptive Performance Control with Embedded Timing Error Predictive Sensors for Subthreshold Circuits

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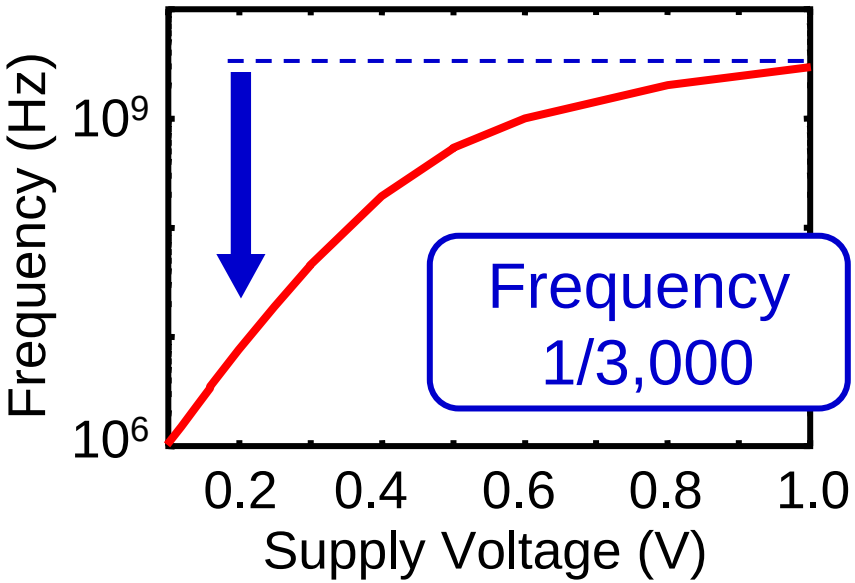
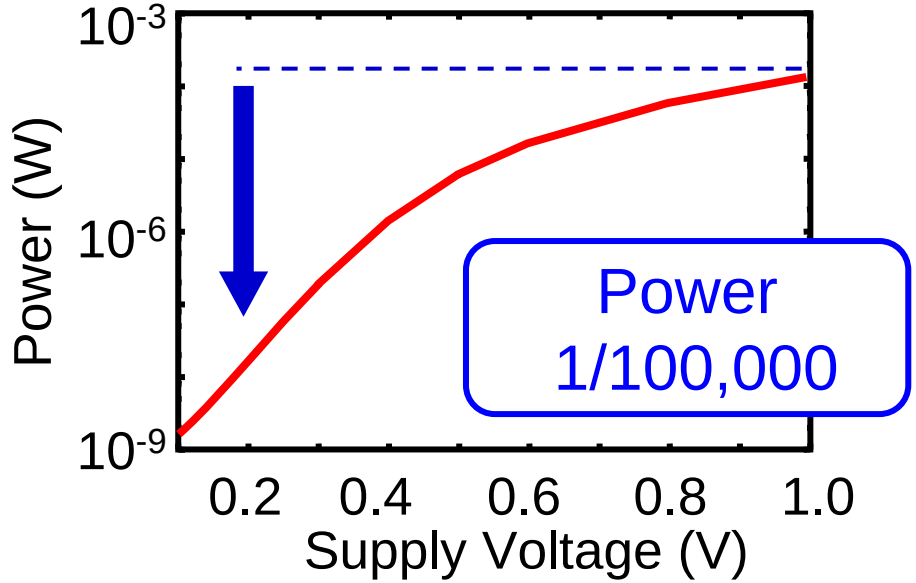
Summary

- Demonstrate an self-adaptive technique for compensating manufacturing and environmental variability using embedded timing error predictive sensor, called "**canary flip-flop**"
  - Test chips were fabricated in 65-nm CMOS process
  - Measurement results show:
    - The power dissipation can be reduced by 46% compared to conventional worst-case design with guardbanding

Background

- Subthreshold Circuits
  - Operate at lower supply voltage than threshold voltage V_{th}
  - **Slow Speed yet Ultra-Low Power**
    - Suitable to energy-constrained devices with low demands for their speeds such as a processor for sensor network





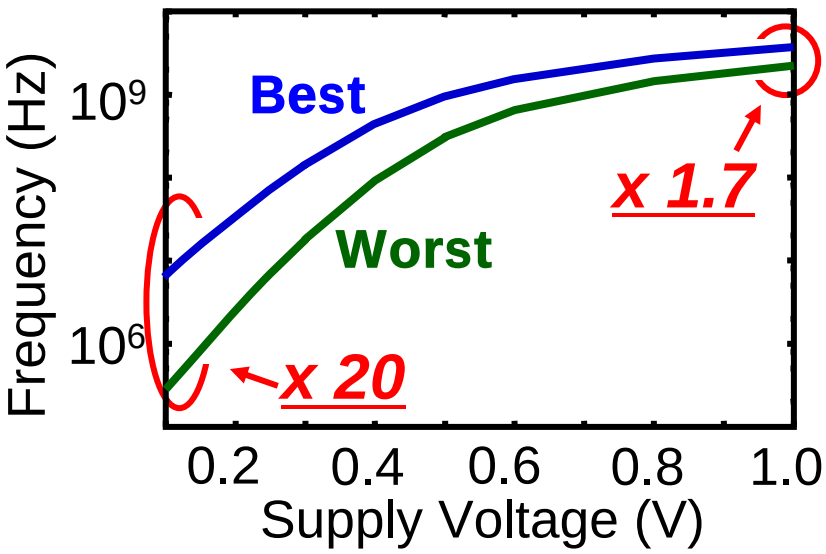
* Simulation of 17-stage ring oscillator (90nm process)

Problem of subthreshold circuits

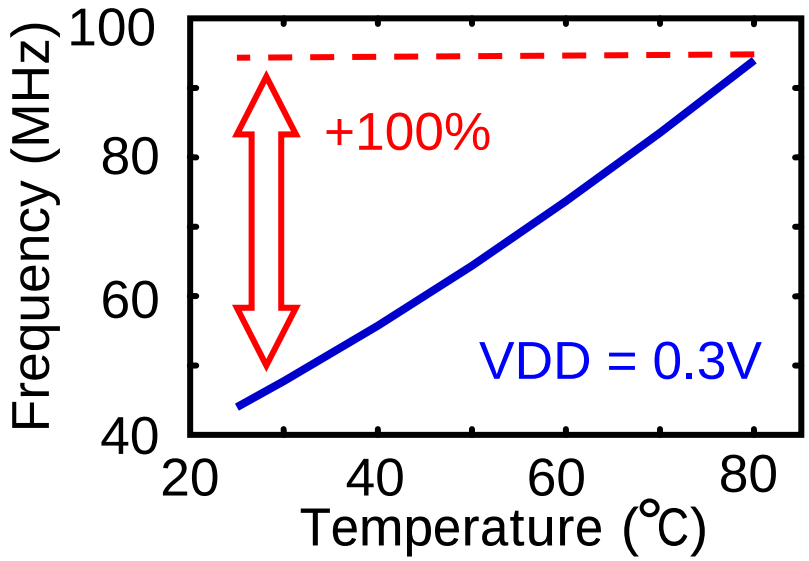
- Extremely sensitive to manufacturing and environmental (PVT) variability
  - Conventional worst-case design is inefficient

    → Run-time adaptive speed control is promising

Manufacturing variability



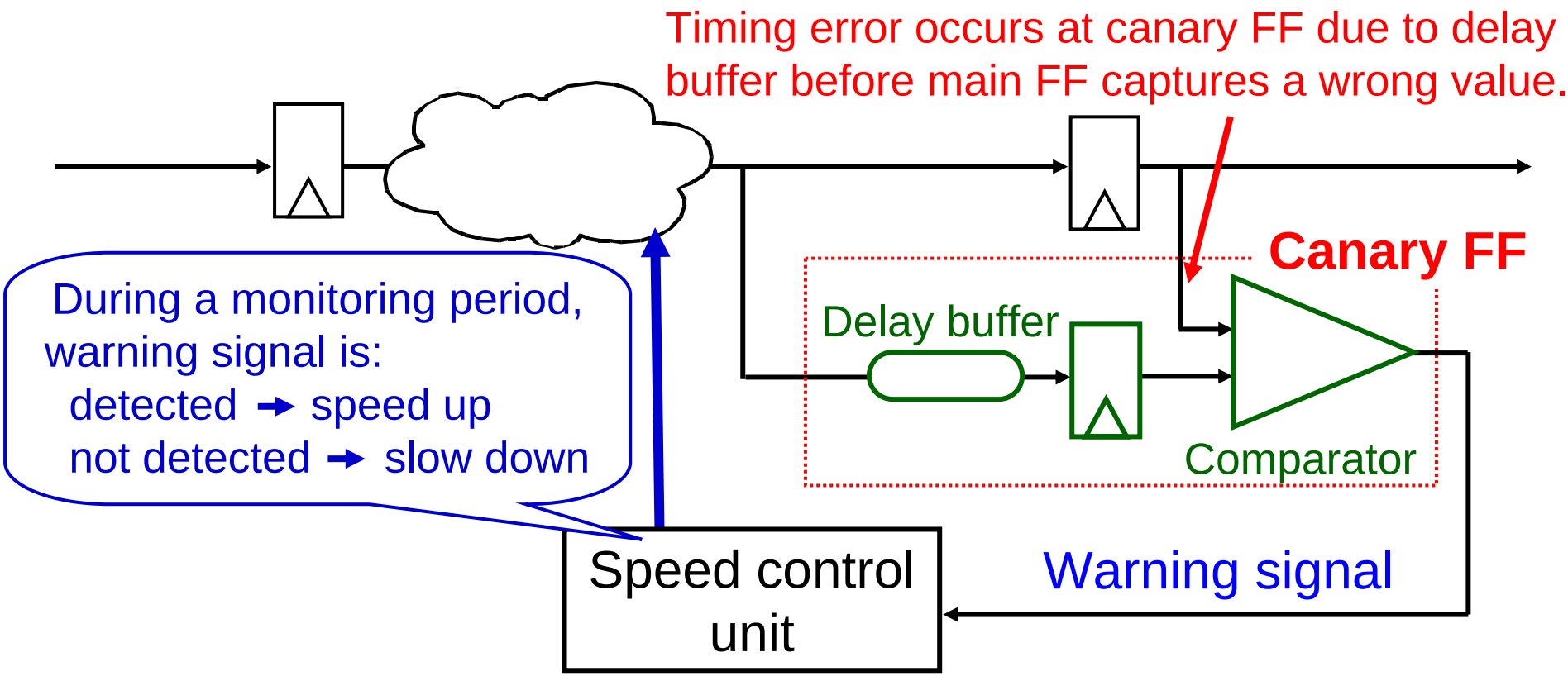
Temperature fluctuation



* Simulation of 17-stage ring oscillator (90nm process)

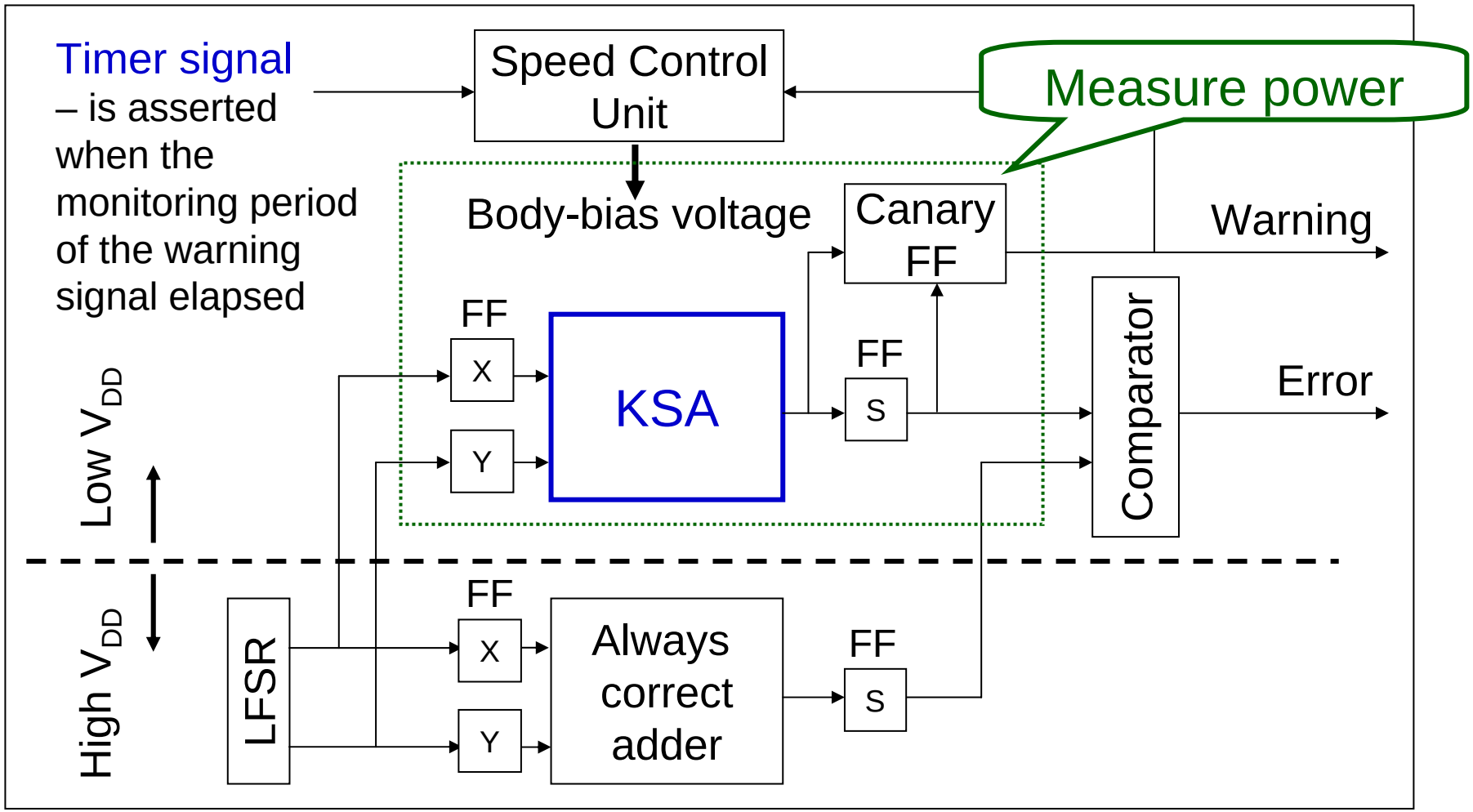
Proposed Technique

- Adaptive speed control with "**canary flip-flop**"
  - Predict the occurrence of timing errors
  - Can be applied to general sequential logics



Circuit structure of test chip

- 32b Kogge-Stone adder（KSA） is controlled adaptively

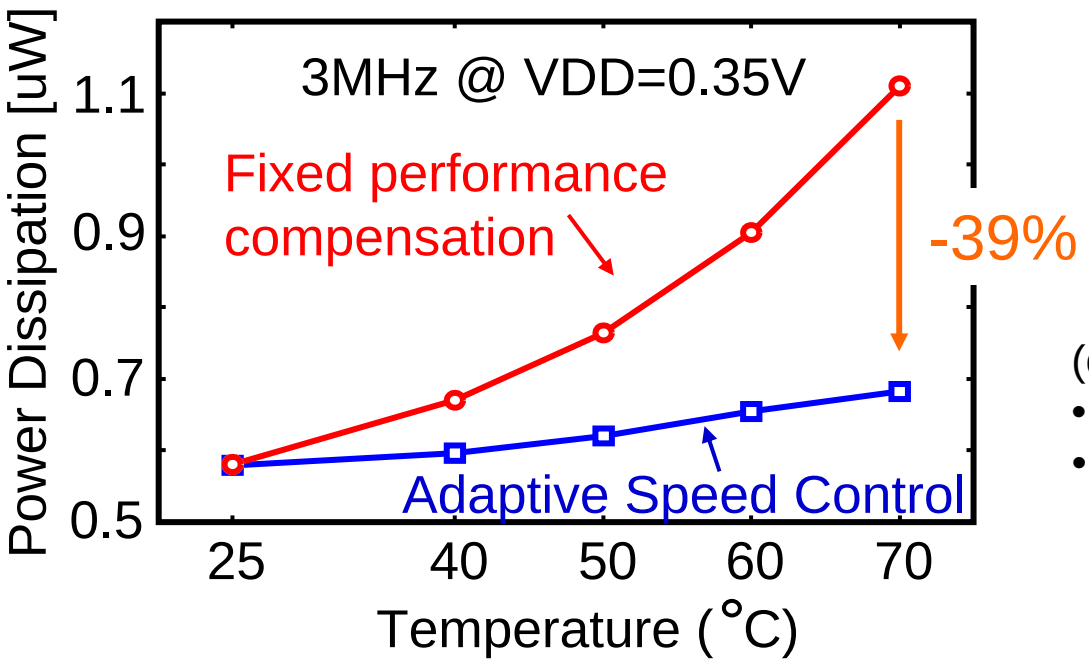


Measurement Result

- Power Dissipation at the various temperature
  - Adaptive speed control with canary FF

v.s. Fixed performance compensation

(Body-bias voltage is fixed)



(operation conditions)
- Monitoring period: 10^7 cycles
- step of body-biasing levels: 30mV

Adaptive speed control is much more energy-efficient