

# Geyser-1: A MIPS R3000 CPU Core with Fine- Grained Run-Time Power Gating

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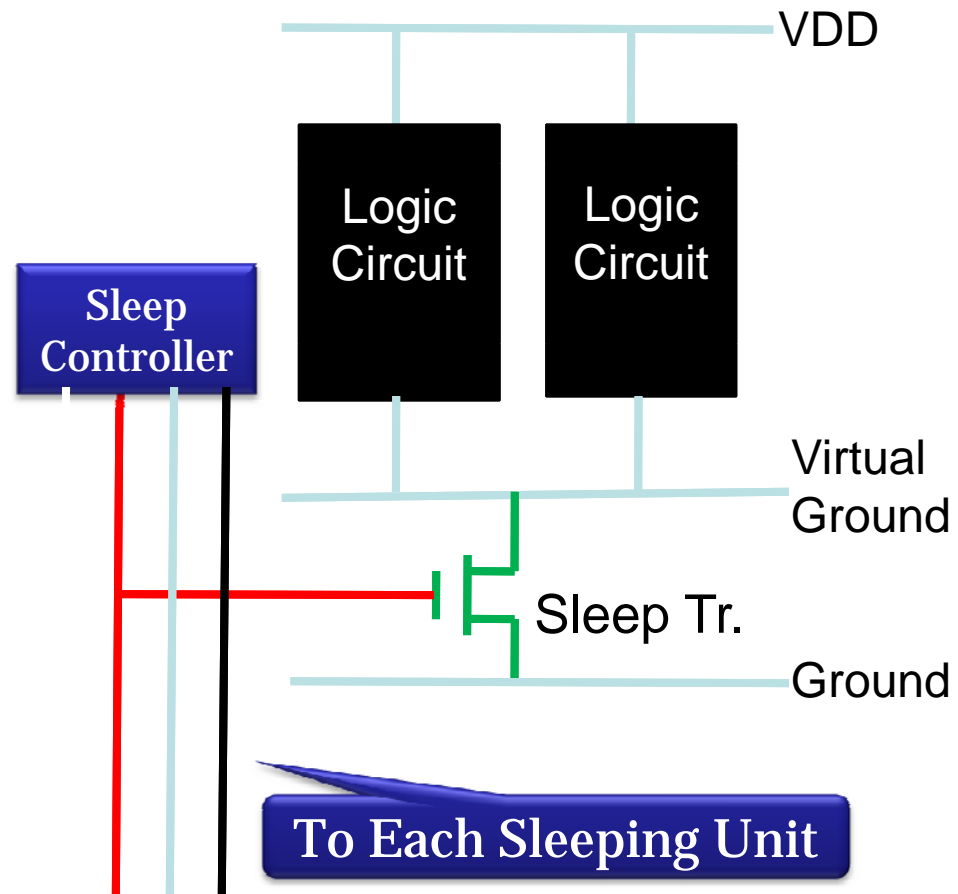
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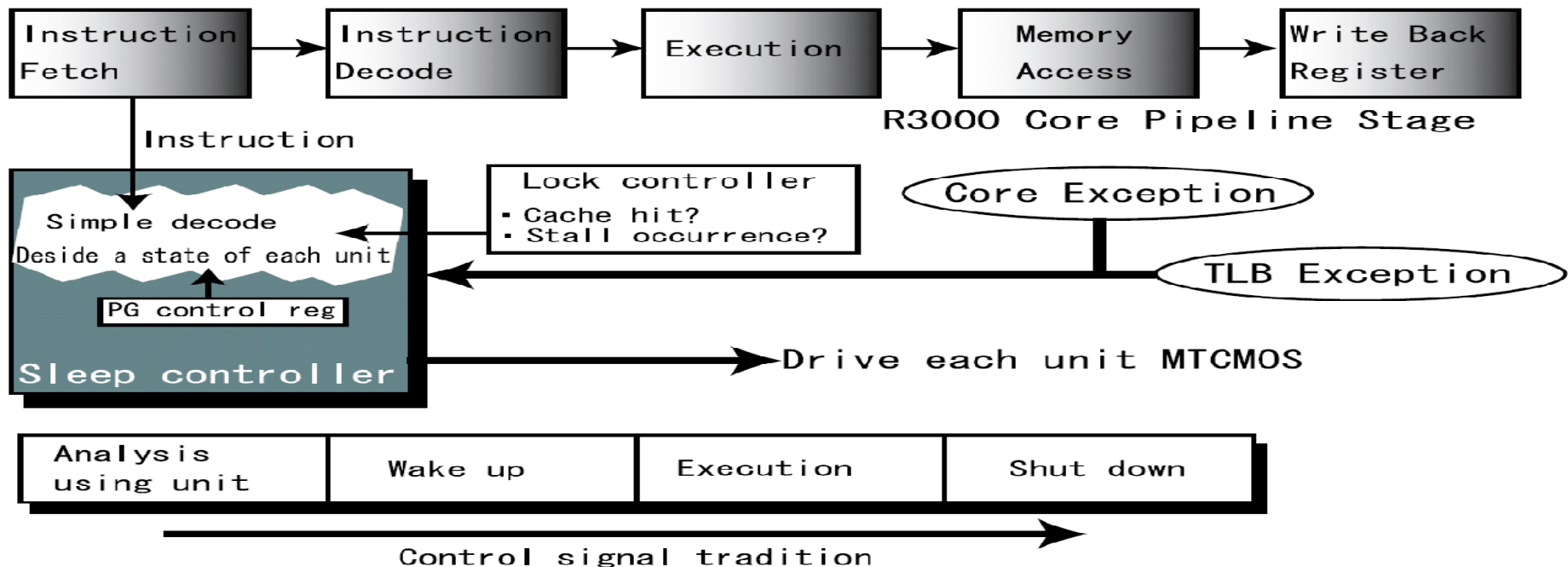
# Power Gating Architecture

- Power Switch (Sleep Tr.) is inserted between logic and Ground  
(or logic and VDD, or both)
- Sleep Tr is high threshold (= low leakage) MTCMOS
  - Sleep Mode: Sleep Tr. cuts off the power
  - Active Mode: Sleep Tr. is power-on and the power is supplied to logic

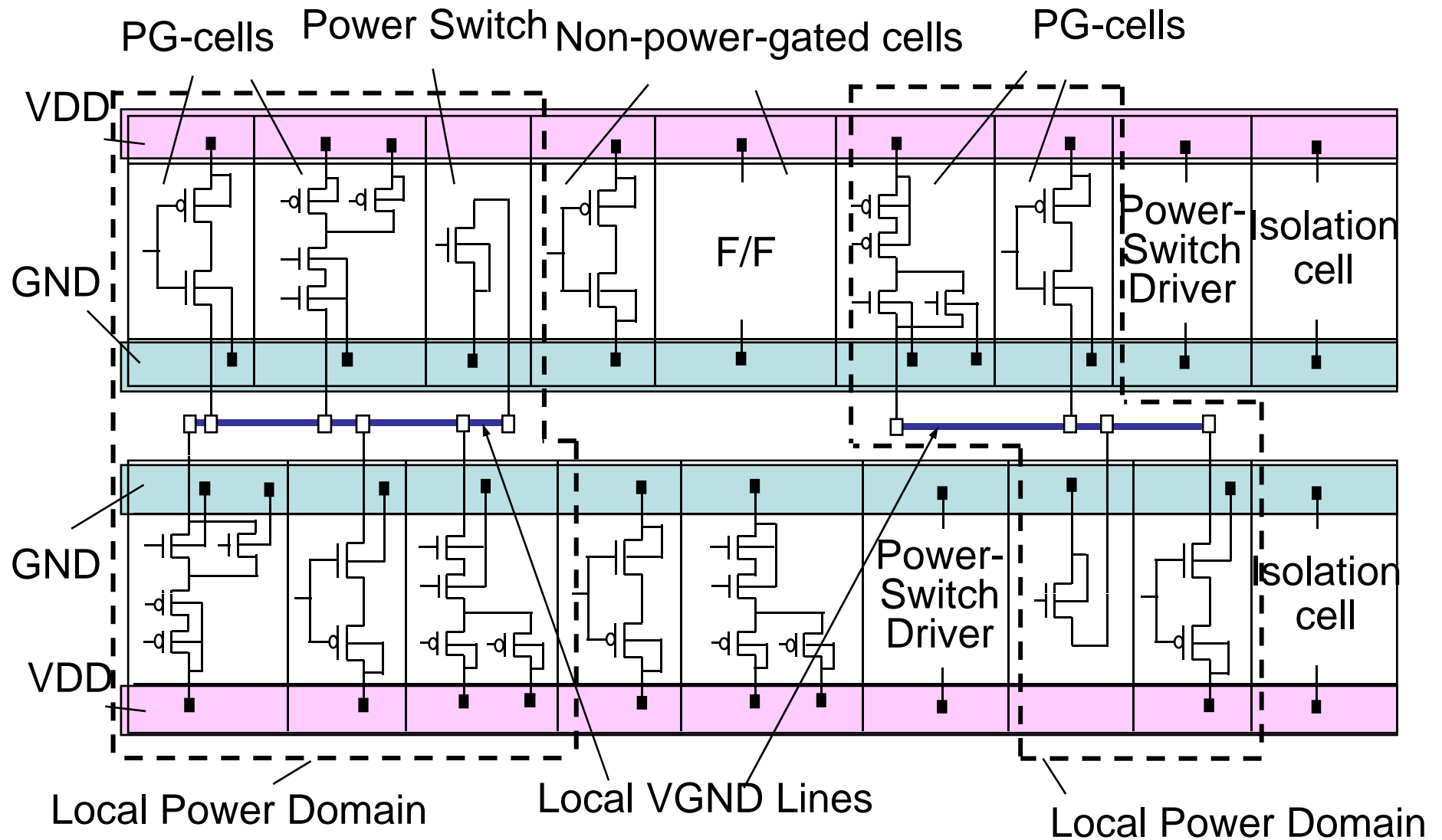


# Run Time Power Gating on Geyser-1

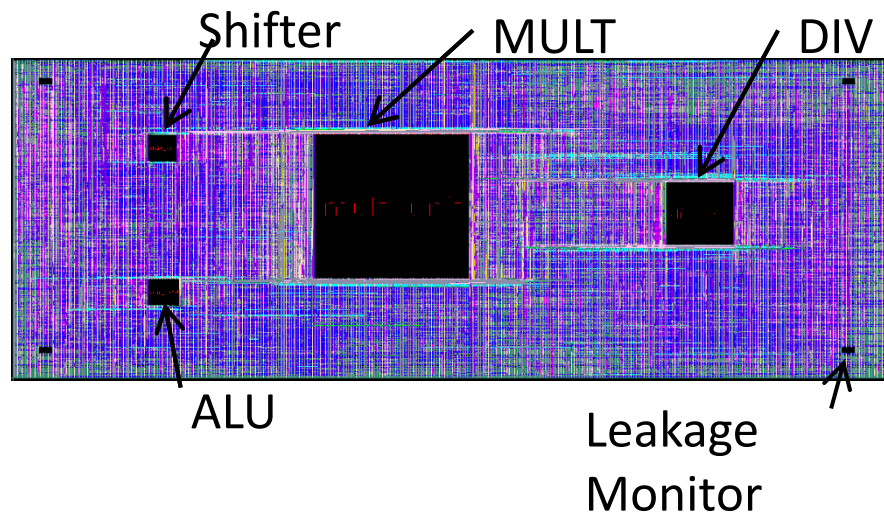
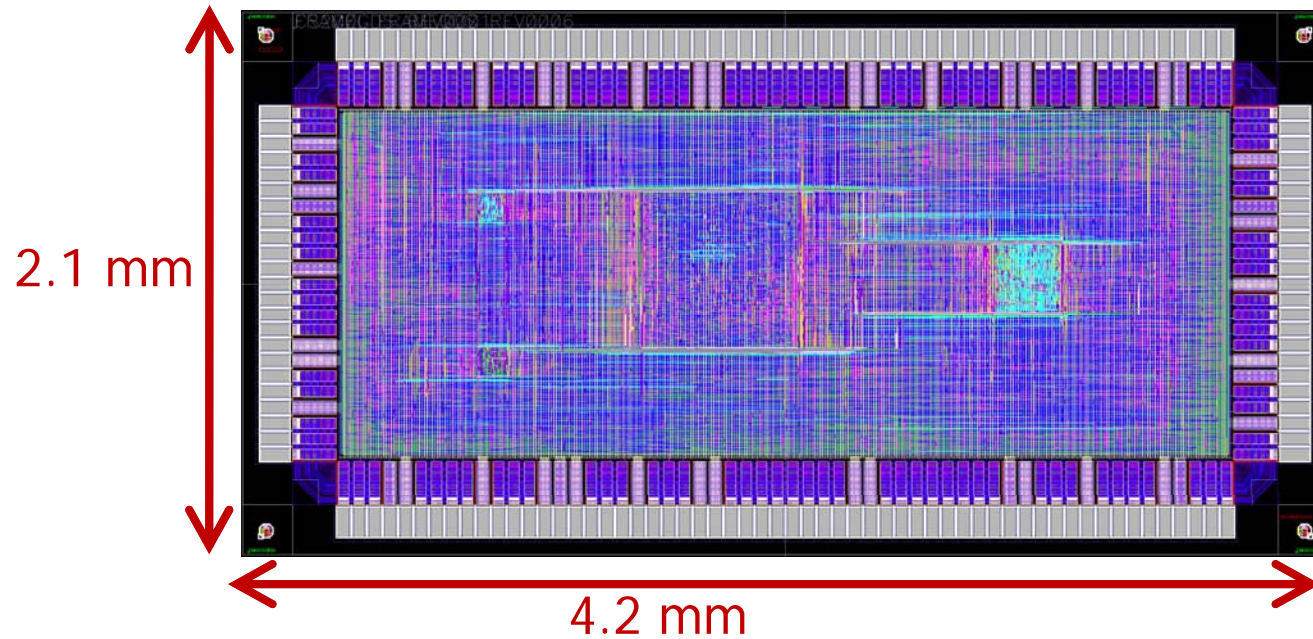
- Geyser is 5-stage standard MIPS R3000 Pipeline
- ALU is split into four units (CLU, Multiplier, Divider, Shifter)
- Each unit is controlled by sleep signal
- The pre-decoder in IF stage creates the wake-up signal
- After the operation, the unit sleeps soon automatically.



# Fine-grain PG [Usami06]



# Geyser-1 Layout



Long wires between I/O pins limit clock at 60MHz

# Simple Conclusion

- Geyser-1 works at 60MHz clock with run-time PG.
- It saves leakage power by 5% to 24%.
- The power in application can be saved by 3% to 28%.
- The area overhead is smaller about 10%.
- Now Geyser-2 with cache/TLB is implemented.

**Please come to the poster**