

MuCCRA-3: A Low Power Dynamically Reconfigurable Processor Array

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MuCCRA-3 Overview

- ▶ Dynamically Reconfigurable Processor Array (DRPA)
- ▶ Flexible offloading engine in various SoCs
 - streaming applications
- ▶ Multi-Context style
 - Datapath changing clock by clock
- ▶ **Instruction-Level Parallelism**
- ▶ Data-Level Parallelism

High flexibility & High performance

- ▶ **MuCCRA-3**
 - Third prototype chip
- ▶ Optimized for low power consumption

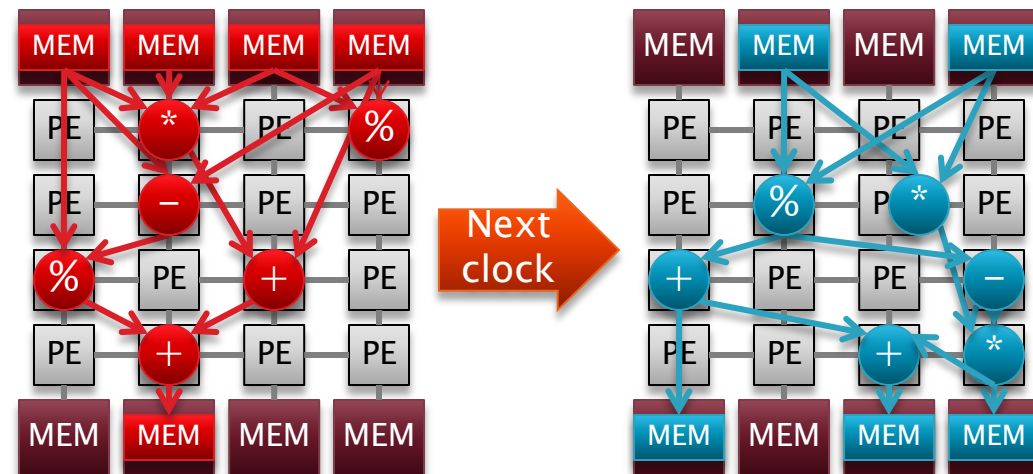


Fig. 1: Datapath changing on DRPA

Structure of MuCCRA-3

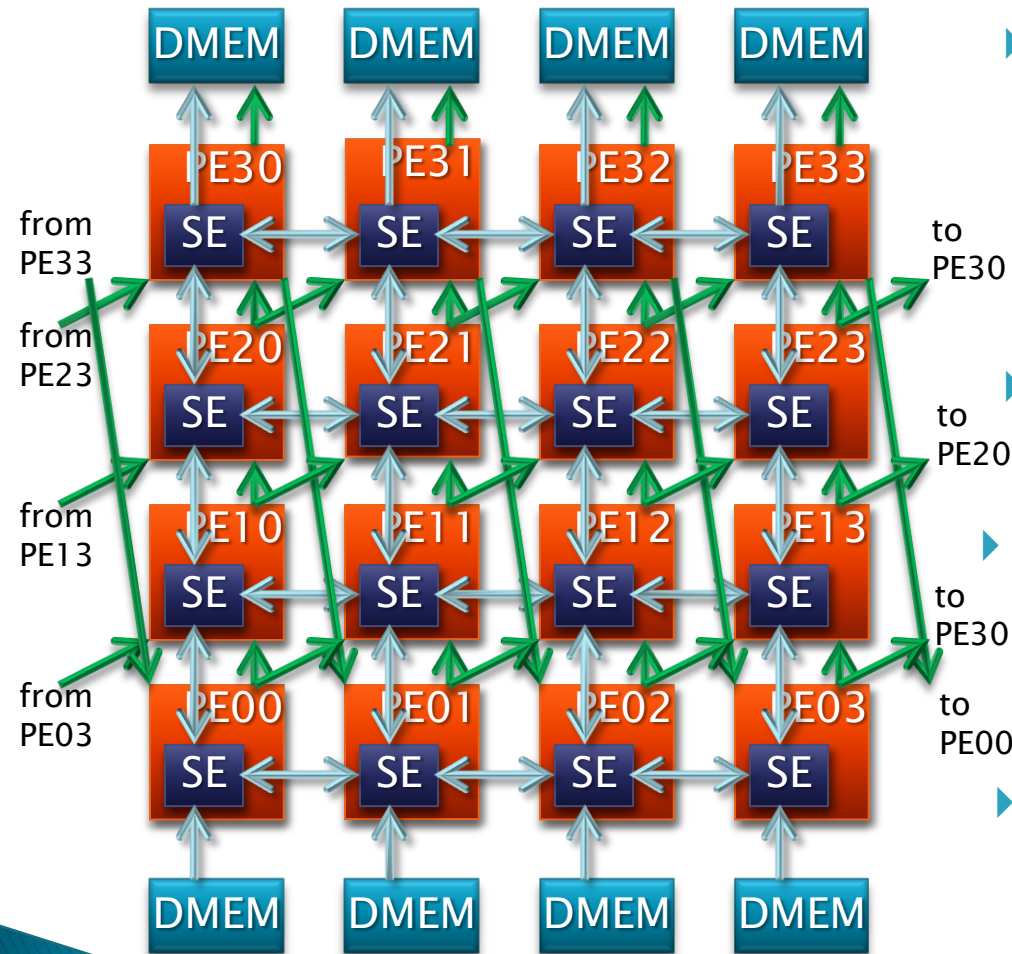
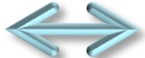



Fig. 2: PE Array of MuCCRA-3

- ▶ PE Array
 - 4x4 PEs
 - Data bit width: 16bit
 - No. of instruction: 14
- ▶ Data Memory (DMEM)
 - 16bits × 128words × 8RAMs
- ▶ Inter PE Network
 - Island-style Links 
 - Direct Links 
- ▶ Multi-Context style
 - 1 clock context switching
 - 32 hardware contexts

PE Structure and Context Switching

- ▶ Dynamically Reconfigurable Modules
 - ALU, Register file, ALU Input SELs, SEs
 - Changes function of each module clock by clock
- ▶ Context Memory
 - Storing Configuration Data
 - Give Conf. Data to each module
 - by Context Pointer from Context Switch Controller (CSC)
 - No. of Entries: 32

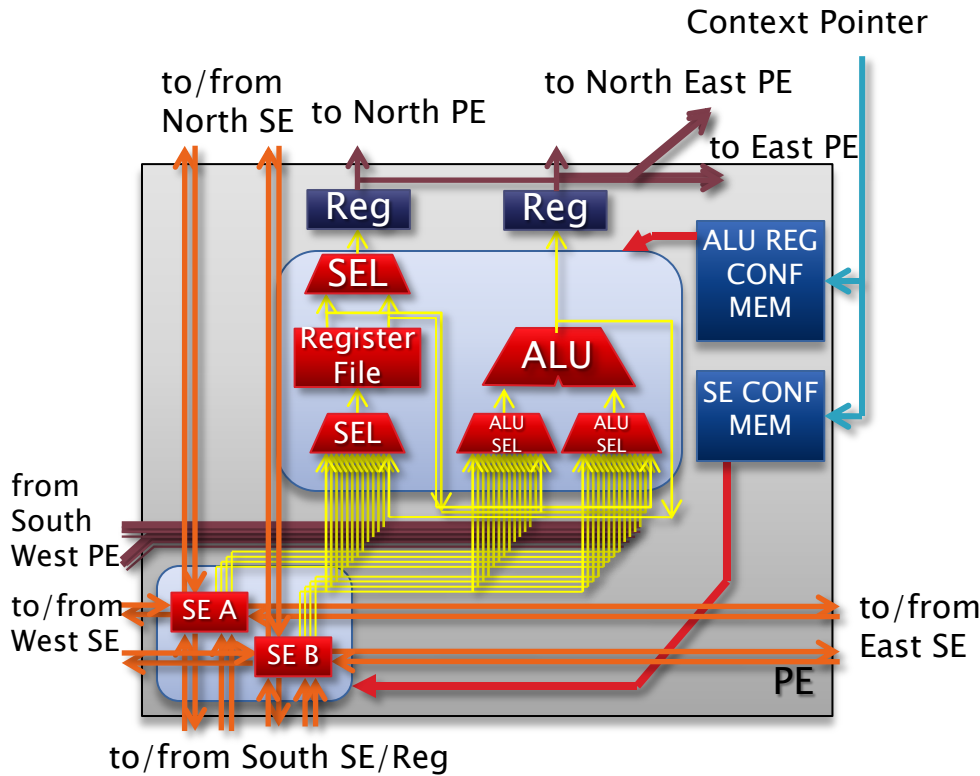


Fig. 3: Structure of PE

Chip Implementation

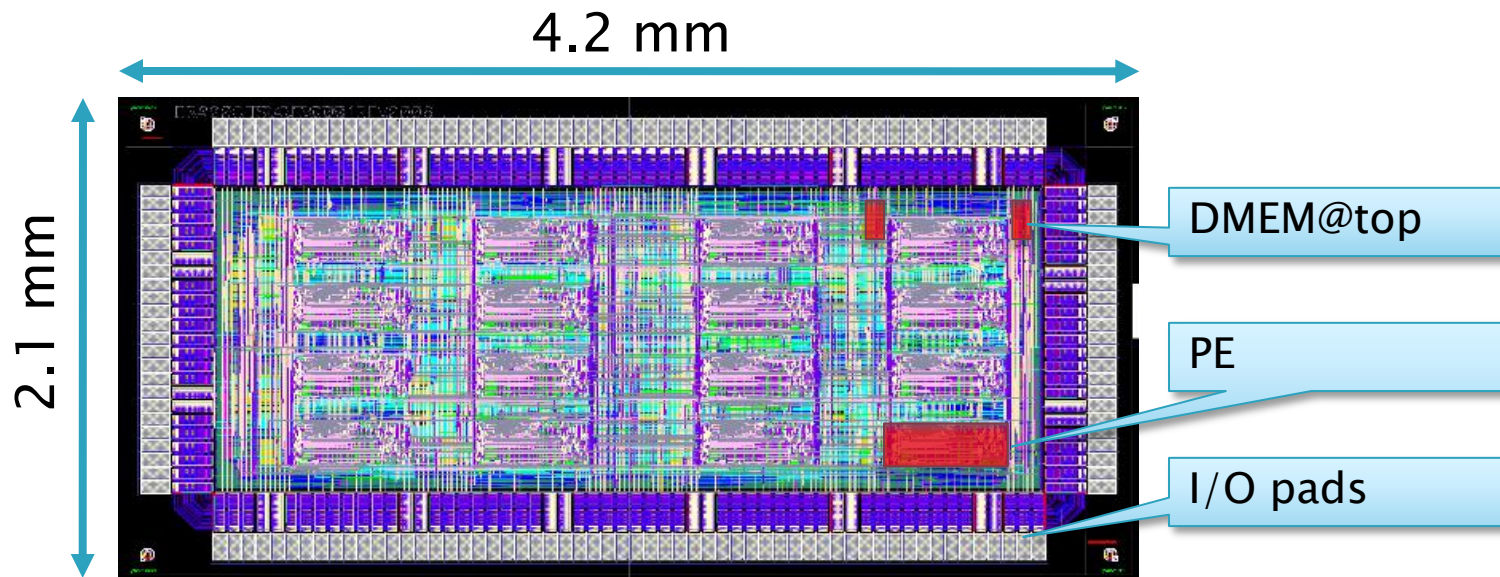


Fig. 4: MuCCRA-3 Floorplan

- Fujitsu e-shuttle 65nm CMOS Process
- Synthesize: Synopsys Design Compiler 2007.12-SP3
- Layout: Cadence's SoC Encounter 7.1
- Target clock frequency: 41.4 MHz

Evaluation Results

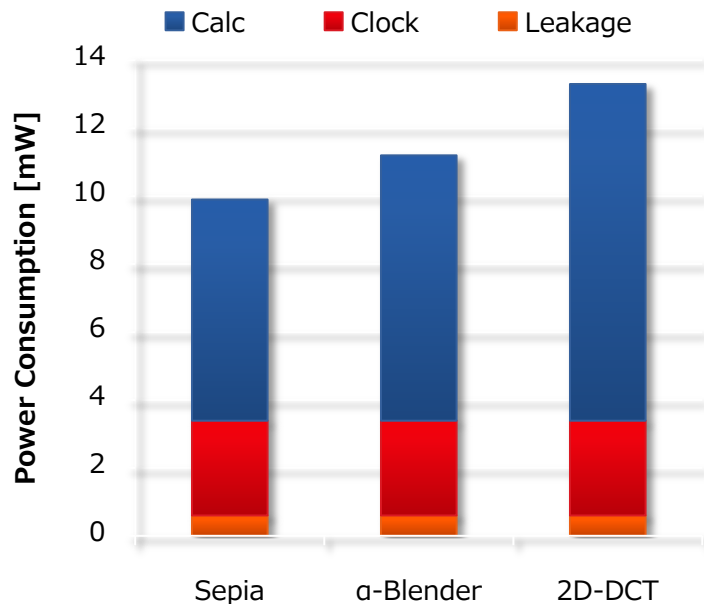


Table 1: Comparing Power Consumption

Device Name (Process Scale [nm])	Clock Freq. [MHz]	Core Supply Voltage [V]	Ave. Power [mW] Energy [nJ]
TI TMS32C6201 (130nm)	167	1.26	684 (310.2) 8412.2 (3815.1)
MuCCRA-1 (ROHM 180nm)	25	1.8	85.1 (13.66) 663.8 (106.54)
MuCCRA-3 (Fujitsu 65nm)	41.4	1.2	11.0 (11.0) 41.8 (41.8)

Fig.5 Power for Executing Applications

▶ Power for Applications

- Power consumption of clock tree: 30% of entire power (Sepia)
- 10–13mW power consumption for each application

▶ Energy consumption

- **Approximately 90 times better than DSP(TI TMS32C6201)**

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