# A Versatile Recognition Processor for Sensor Network Applications

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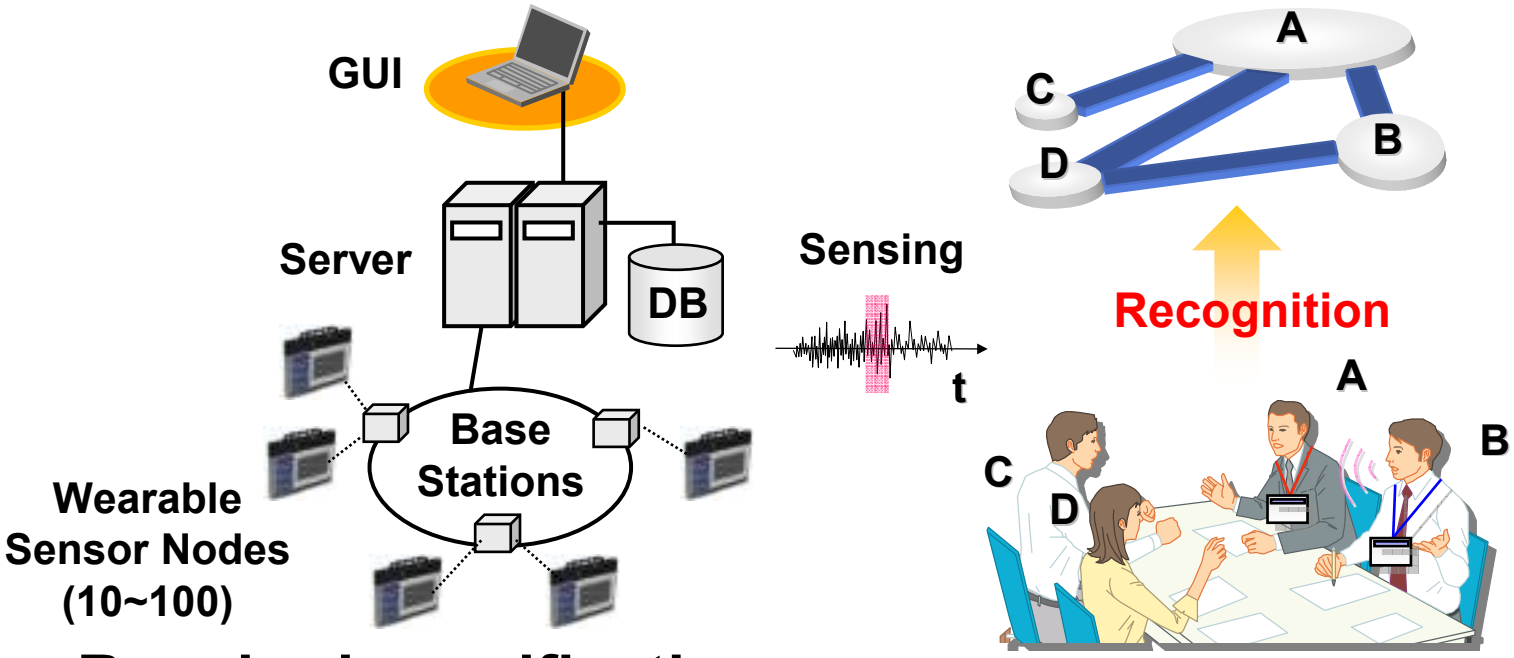
# Background

- Target applications
  - Mobile phone, Digital still camera…
  - Sensor Network Applications: Business Microscope[1]



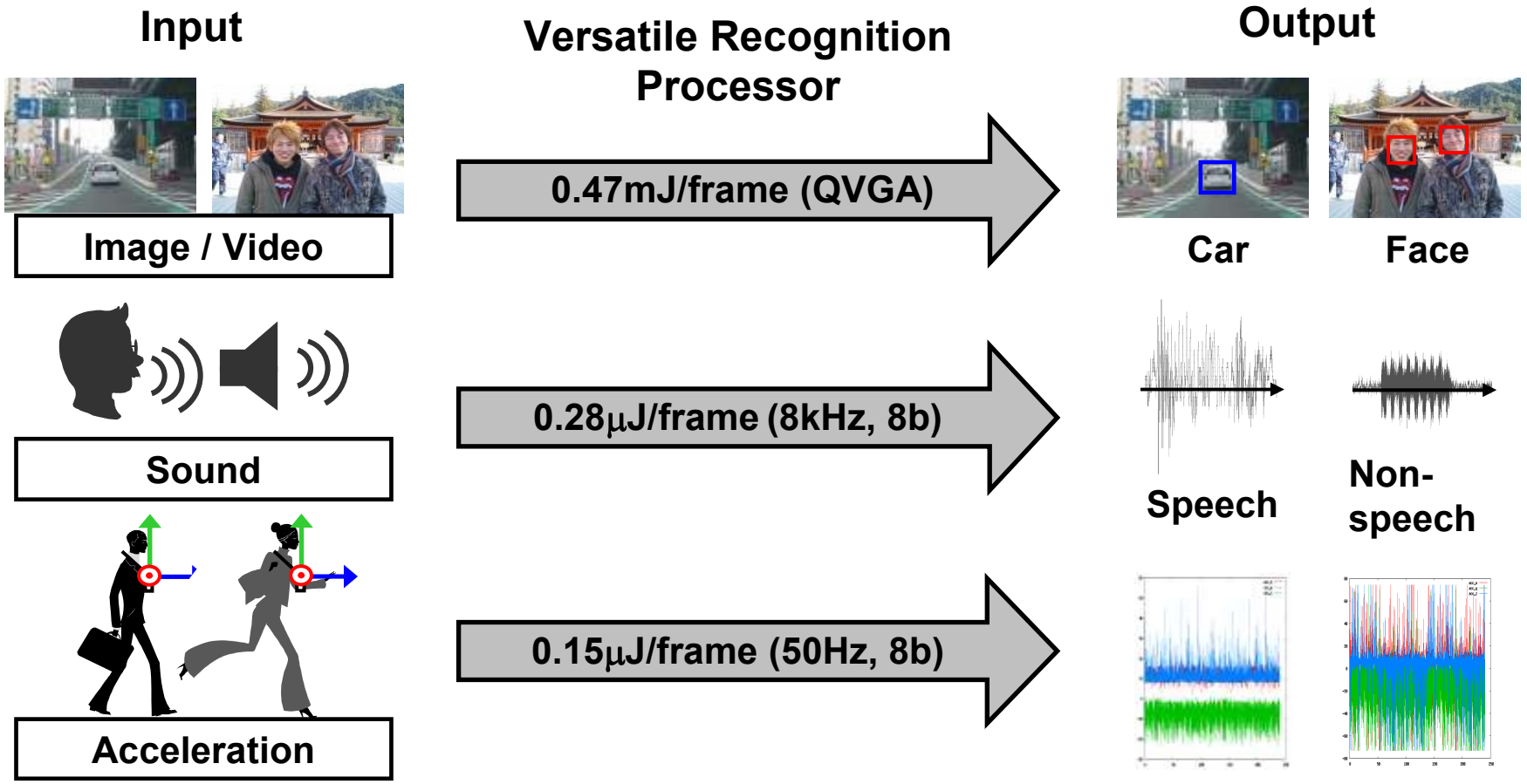

- Required specifications
  - Versatility: input signals (Image, Sound, Acceleration…)
  - Low energy consumption: less than sub-mJ/frame



[1] J. Nishimura, IEEE PerCom'08

# This Work

- 0.47mJ versatile recognition processor
  - ◆ “Algorithm driven” architecture : No parallel PEs
  - ◆ For image, sound, and acceleration



# Overall Optimization Procedure

## 1. Algorithm Development

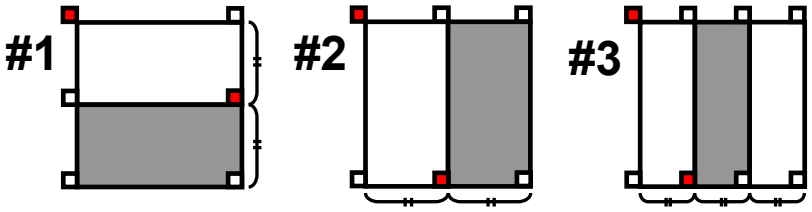
- ◆ Haar-Like Feature (HF)
  - ■ Low computational cost
- ◆ Cascaded Classifier (CC)
  - ■ 98% computational cost reduction

## 2. Architecture Design

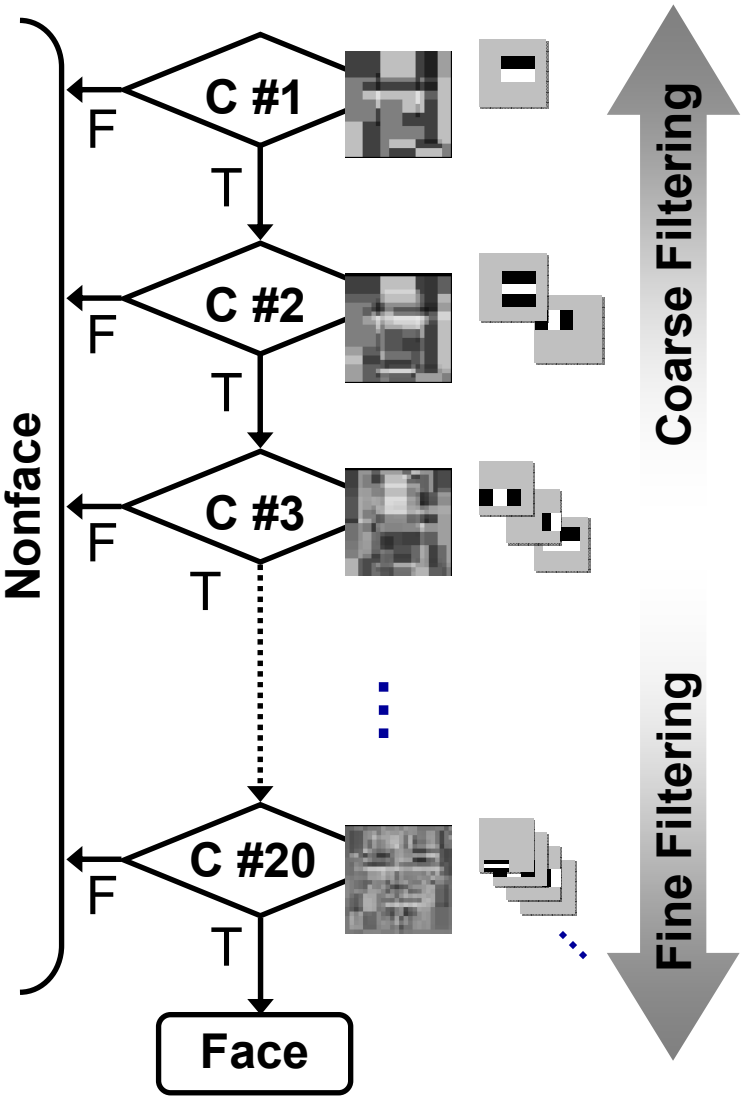
- ◆ Classifier Data Cache

## 3. Circuit Design

- ◆ HF Index Rearrangement
- ◆ HF Coordinates Decoder (HFCD)
- ◆ HF Value Extractor (HFVE)

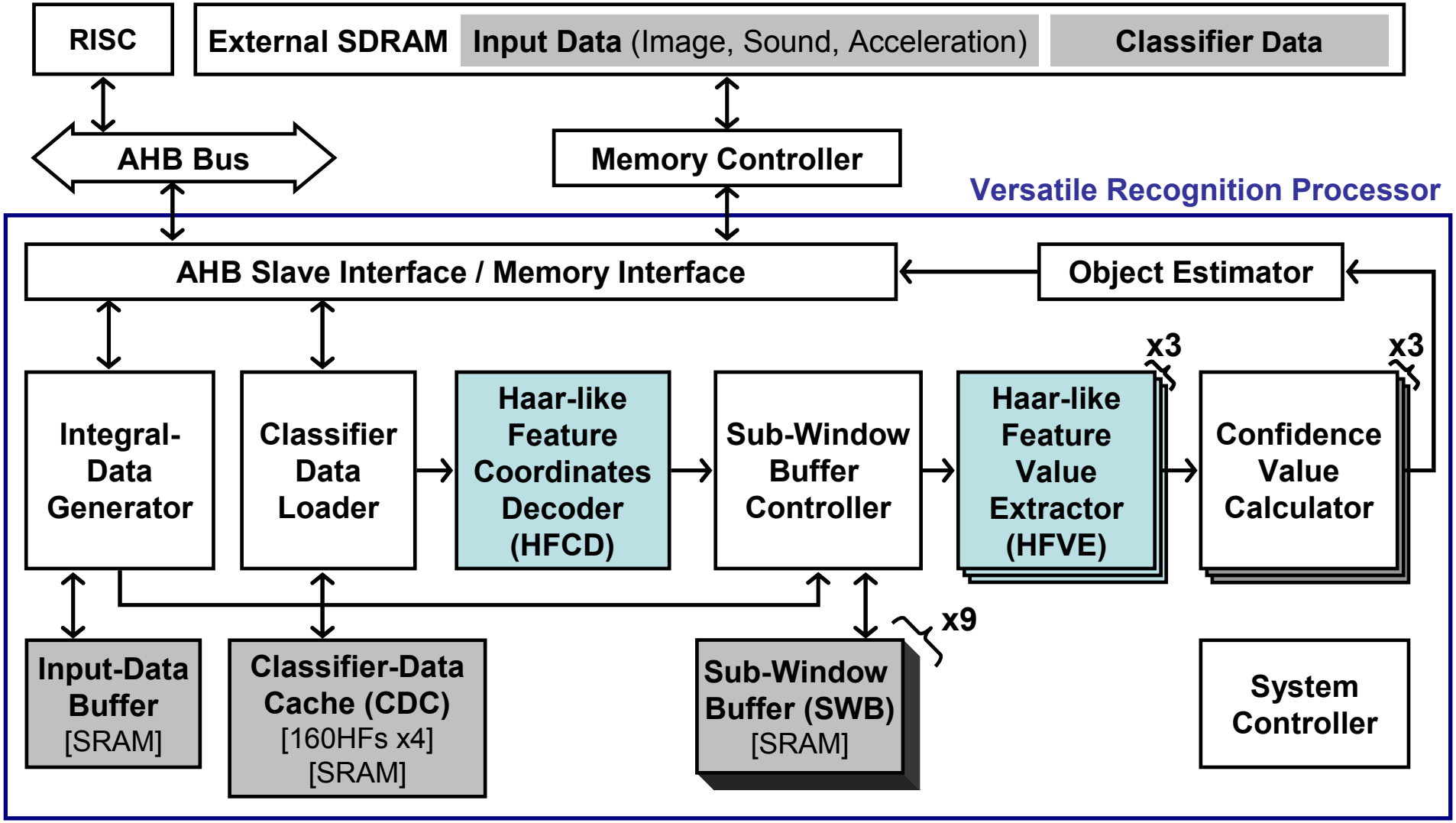



Haar-like Feature

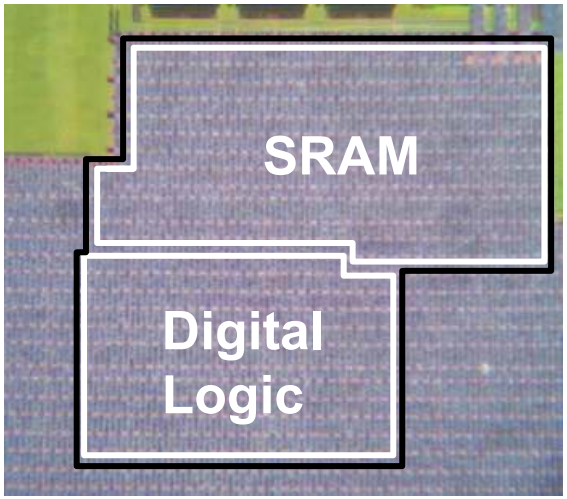


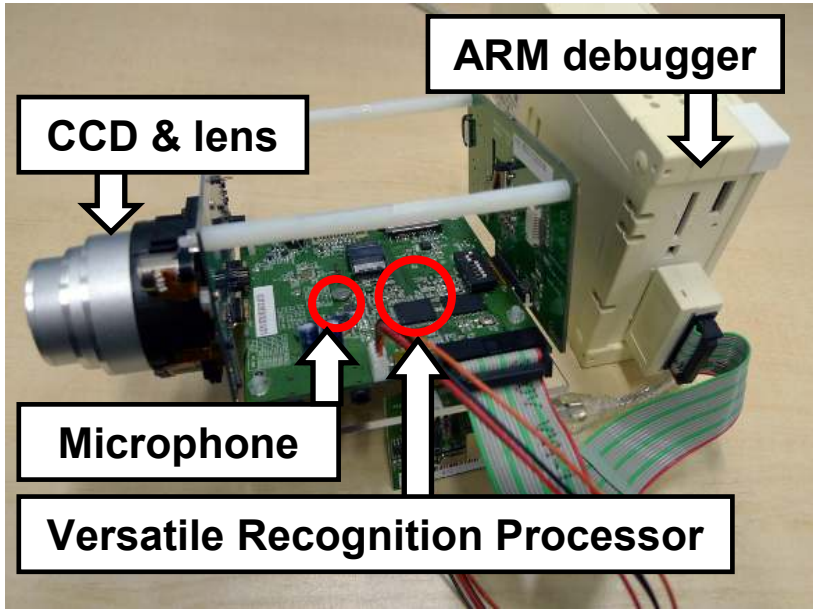

Cascaded Classifier

# Block Diagram



# Micrograph and Performance Summary




| | | |
|---|---|---|
| Technology | | 90nm CMOS |
| Supply Voltage | | 0.9V |
| Layout Area | | 0.89mm$^2$ |
| Number of Transistors | | 2.1M |
| Clock Frequency | | 54MHz |
| Energy Consumption | Image | 0.47mJ/frame |
| | Sound | 0.28μJ/frame |
| | Acceleration | 0.15μJ/frame |

# Conclusion

- 0.47mJ versatile recognition processor is developed using a 90nm CMOS technology
- Overall optimization of processor design contributes to versatility and energy efficiency