TOSHIBA
Leading Innovation

Design and Verification Methods of Toshiba's Wireless LAN Baseband SoC

Masanori Kuwahara

Toshiba Corporation
Japan

January 18-21, 2010

秘

Toshiba WLAN Baseband SoC Series

- **TC90515XBG**
  - Over 30 Mbps on TCP/IP.
  - Build-in DTCP (Digital Transmission Content Protection).
  - Suitable for HD (High-Definition) video transmission.
- **TC90525XBG**
  - 20 Mbps on TCP/IP.
  - Small-sized, low-cost chip.
  - Suitable for various embedded systems like consumer electronics, security cameras, toys and so on.
- **TC90535XBG**
  - 20 Mbps on TCP/IP.
  - Ultra low power.
  - Suitable for various low power mobile devices.

Requirements of WLAN Baseband SoC

- **MAC layer must conform with many specifications, authentication tests, radio laws of each country.**
  - A great deal of verification is needed for MAC hardware.
- **PHY layer is composed of many complicated signal processing circuits.**
- **PHY layer is difficult to evaluate its wireless performance.**
  - Wireless performance is not guaranteed only by clock speed. Packet error rate (PER) is also a crucial metric.
  - But, RTL simulation to evaluate PER takes very long time.
- **Low Power is becoming increasingly necessary for WLAN SoC.**
  - WLAN are getting installed into much more mobile devices.
  - Ever-increasing data rate and multi antennas are pushing up power.
  - Ultra low power design method is needed.

Outline

- Design and Verification method of MAC
- Design and Verification method of PHY
- Design method of Ultra Low Power Wireless BB SoC
- Summary

Outline

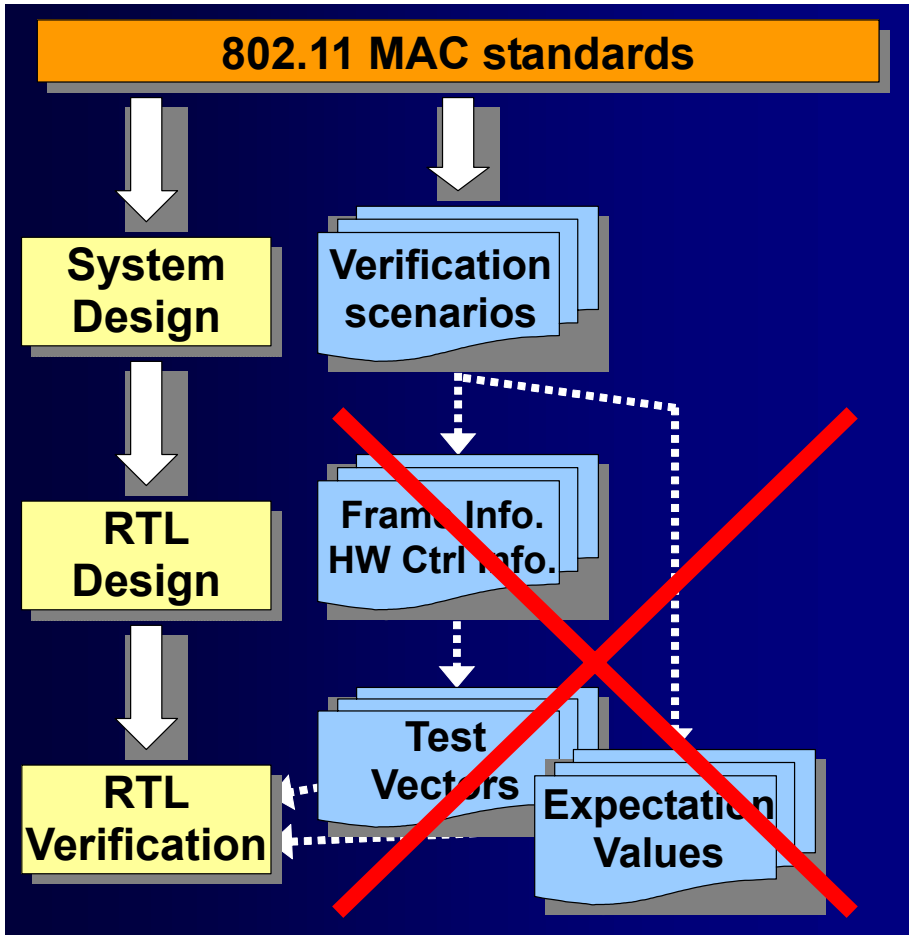
- **Design and Verification method of MAC**
- Design and Verification method of PHY
- Design method of Ultra Low Power Wireless BB SoC
- Summary

MAC Needs Lots of Verification

- **Standards**
  - 802.11a / b / g / n / e / h / i / k, …
    - Each having complicated protocols:
      - CDMA/CA, PCF, DCF, Backoff, Ad Hoc, RTS/CTS, …
- **Authentication tests**
  - Wi-Fi tests
  - Interoperability tests
- **Laws**
  - Radio Law, Technical Regulations Conformity Certification (Japan)
  - Federal Communications Commission (US)

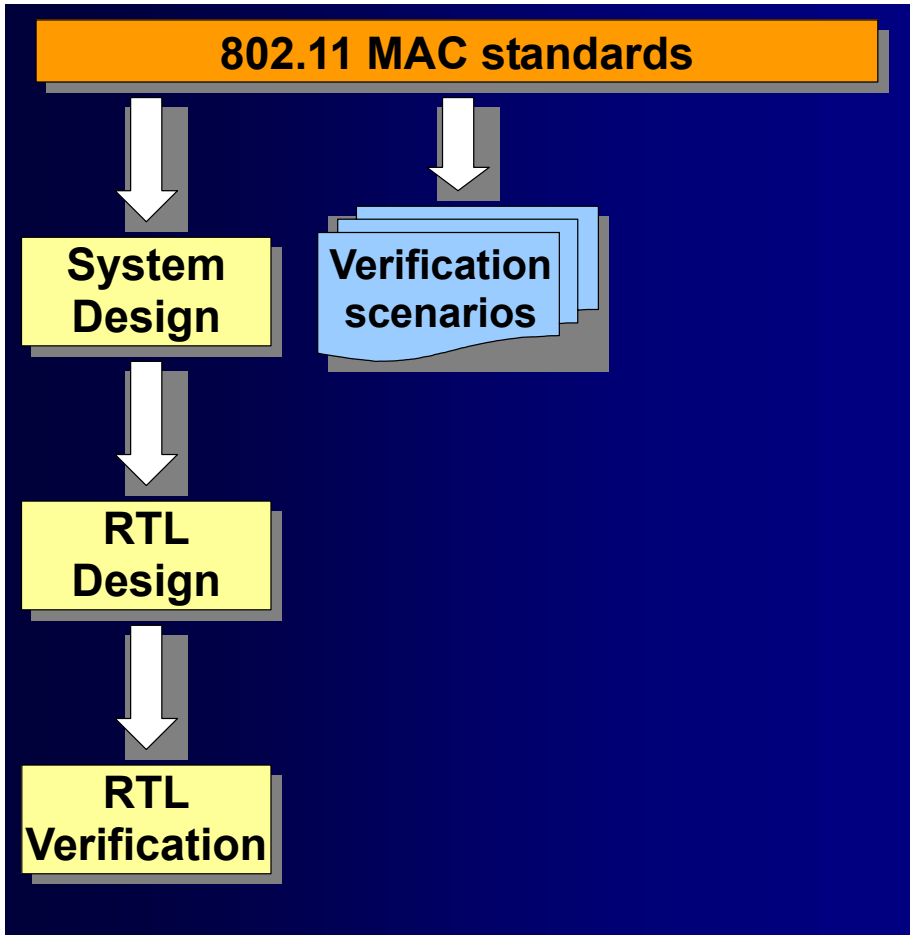
Efficient and Reliable verification method is needed.

Conventional MAC Verification Method



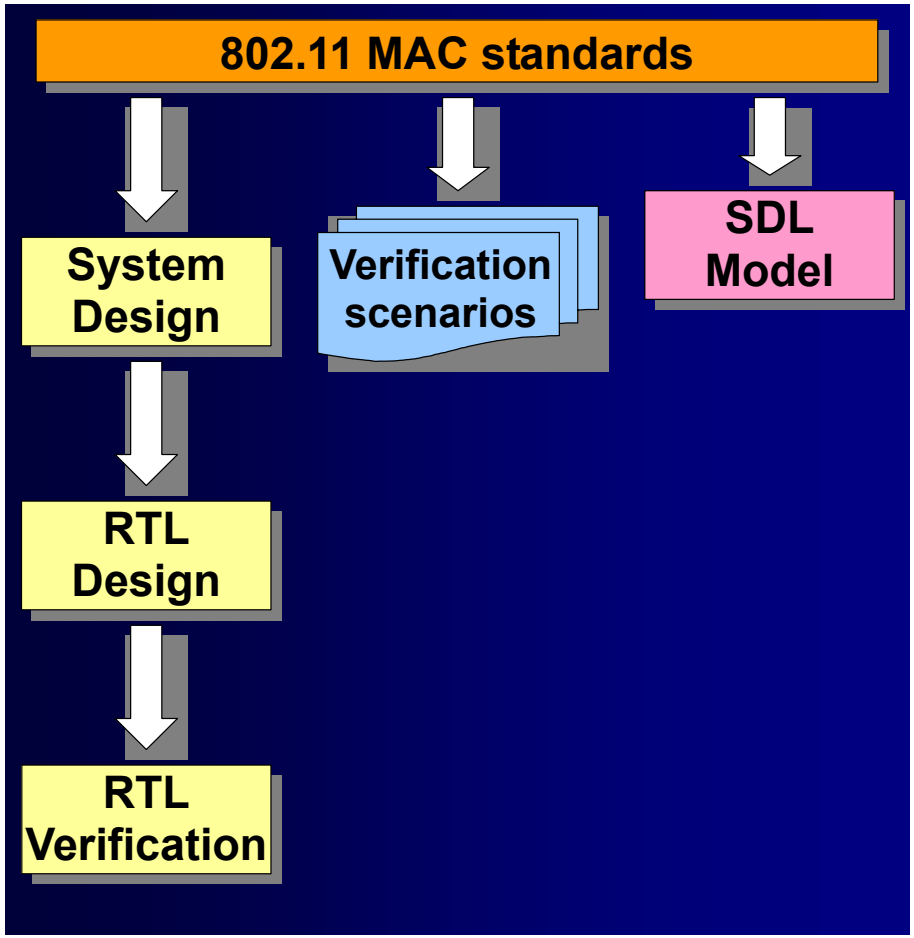
- **Reliability problem**
  - Many complicated MAC protocols.
  - Some scenarios may be wrong or lacking due to human errors.
  - Verification scenarios not validated.
- **Efficiency problem**
  - Many test vectors and expectation values are made by human hand.
  - It's cumbersome and time-consuming.

New MAC Verification Method



- **SDL is introduced.**

New MAC Verification Method



- **SDL is introduced.**
- **MAC is modeled by SDL.**

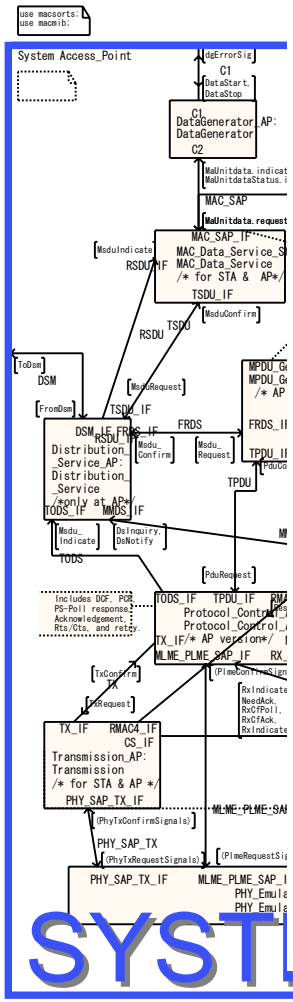
What is SDL?

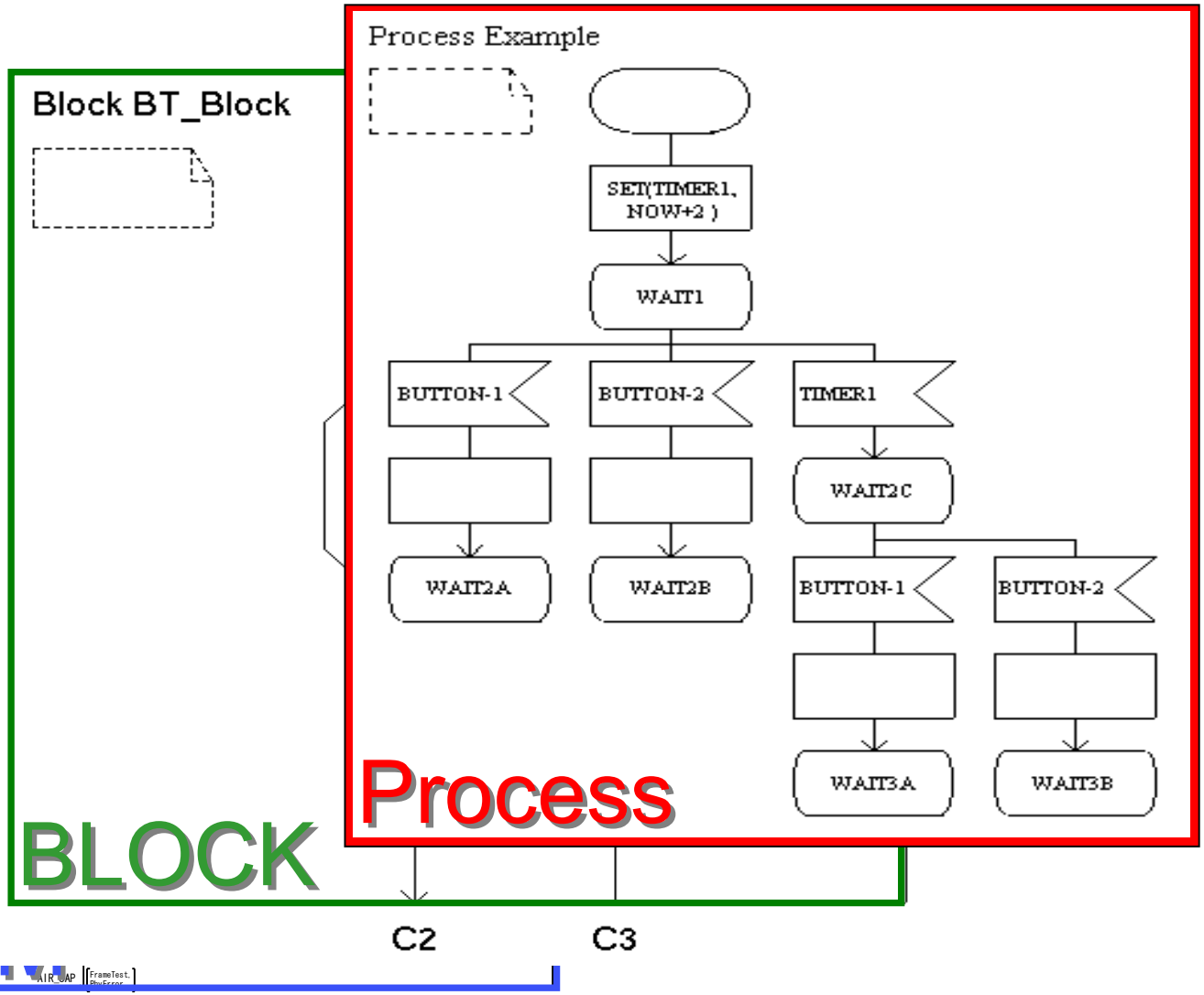
- **Specification and Description Language**
  - Formal language standardized by ITU-T.
  - Describes specification without ambiguity.
  - Its model can be verified by the SDL simulator.
  - It's usually used for software development, but we use it for hardware development.

ITU-T : International Telecommunication Union
Telecommunication Standardization Sector

SDL Model of MAC

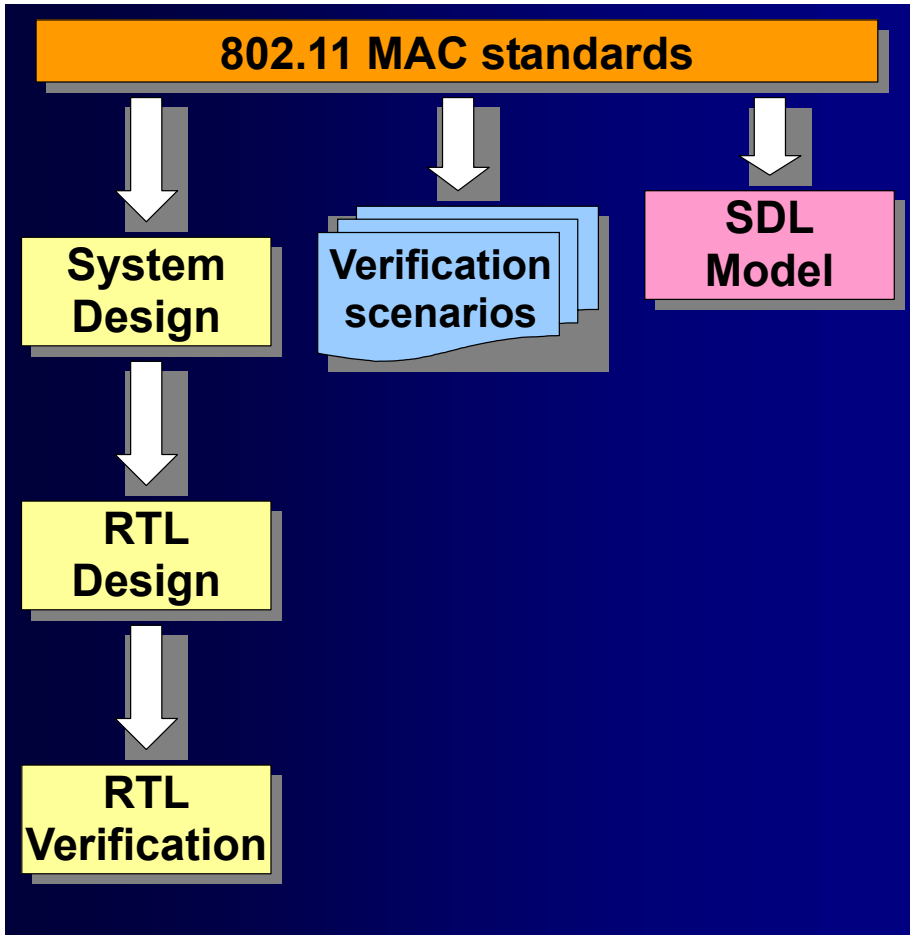
- **Top diag**





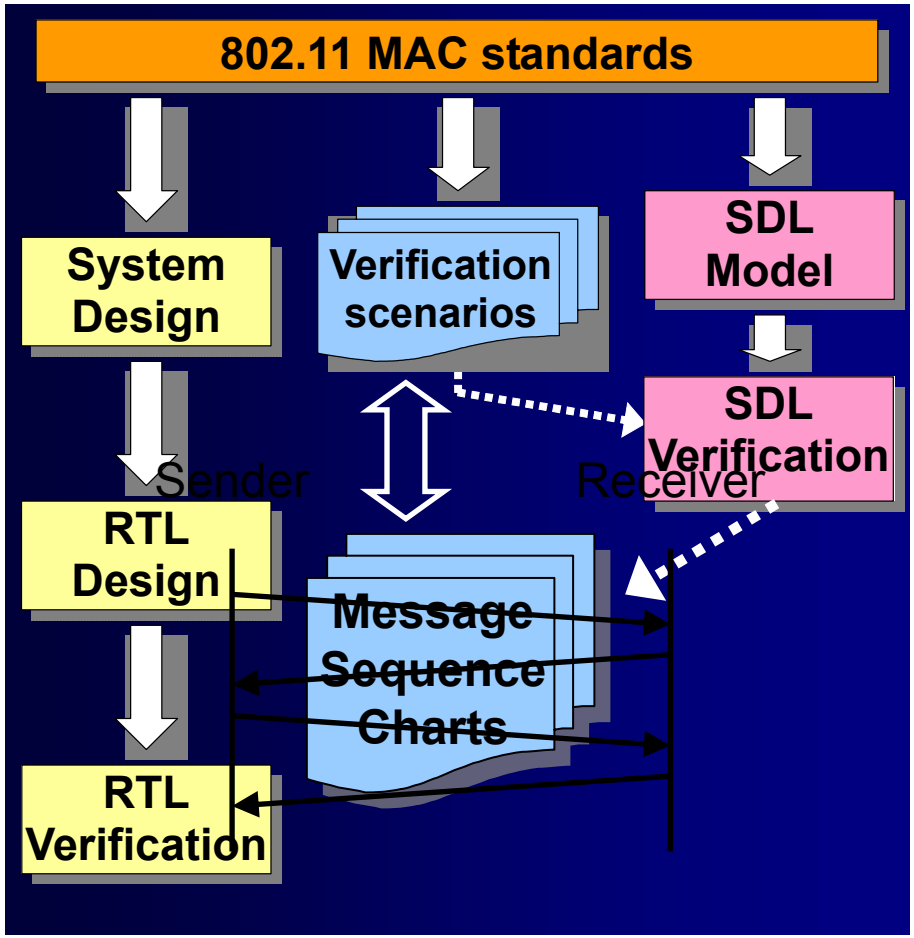
SYSTEM

Scenarios Validation



- **Scenarios are validated with the SDL model by using SDL simulator.**

Scenarios Validation

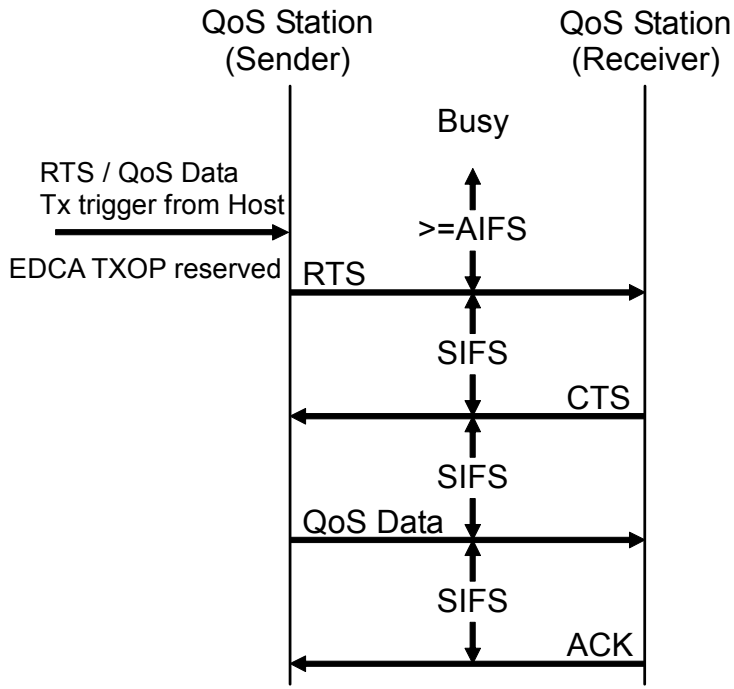


- Scenarios are validated with the SDL model by using SDL simulator.
- The simulator outputs MSC (Message Sequence Chart).

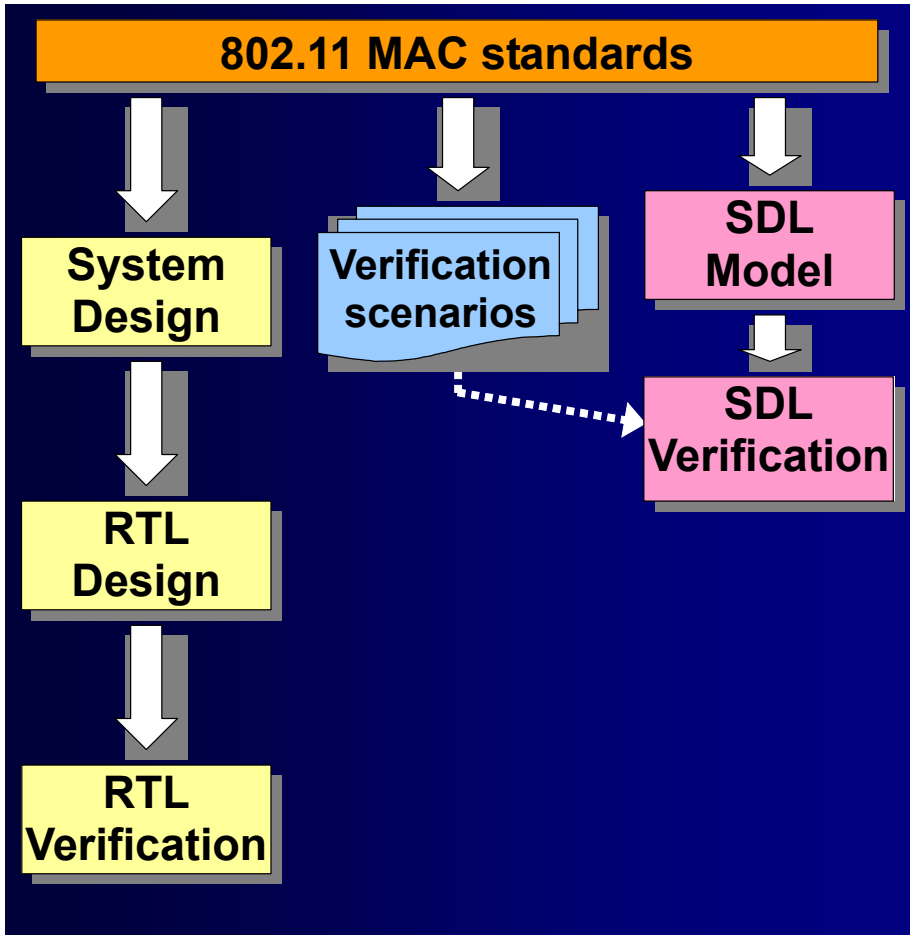
Verification Scenarios

- **196 fundamental scenarios are prepared for 802.11a/e/h**
  - Complicated scenarios can be constructed from the fundamental ones.

Category	Number of scenarios
HCCA	34
EDCA	18
Management	6
802.11h	32
Sequence	23
Illegal input	68
Miscellaneous	15
Total	196

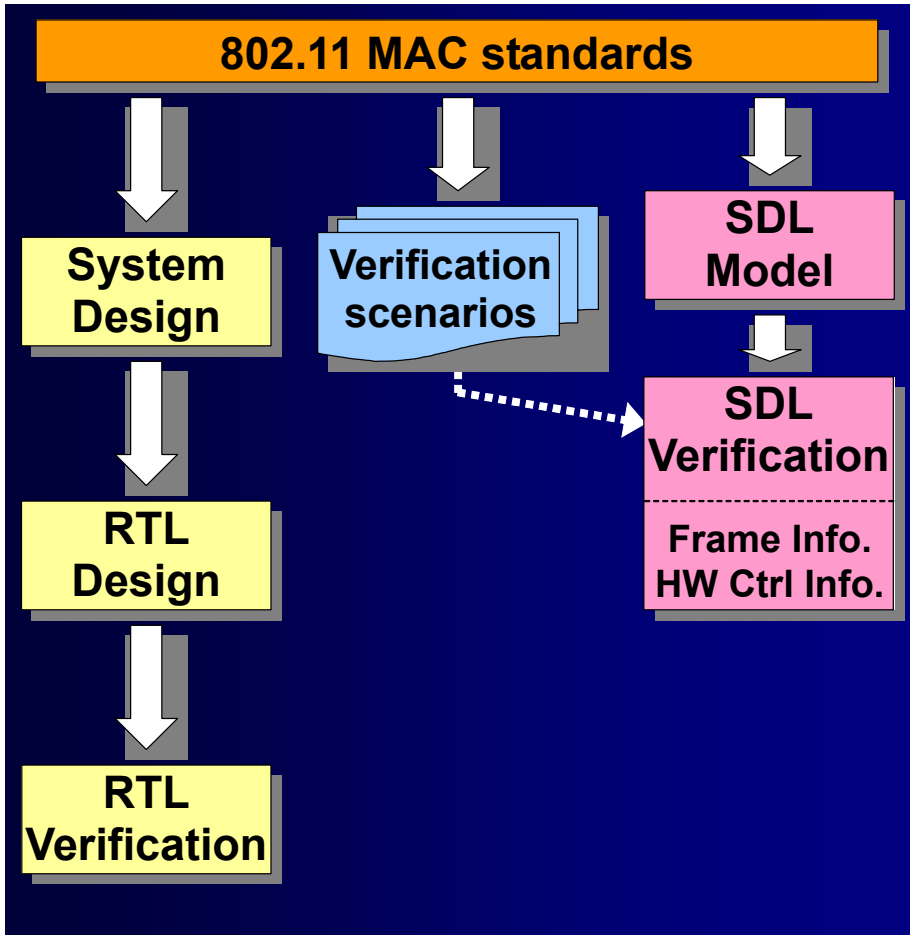


Test Vectors and Expectation Values Automatic Generation



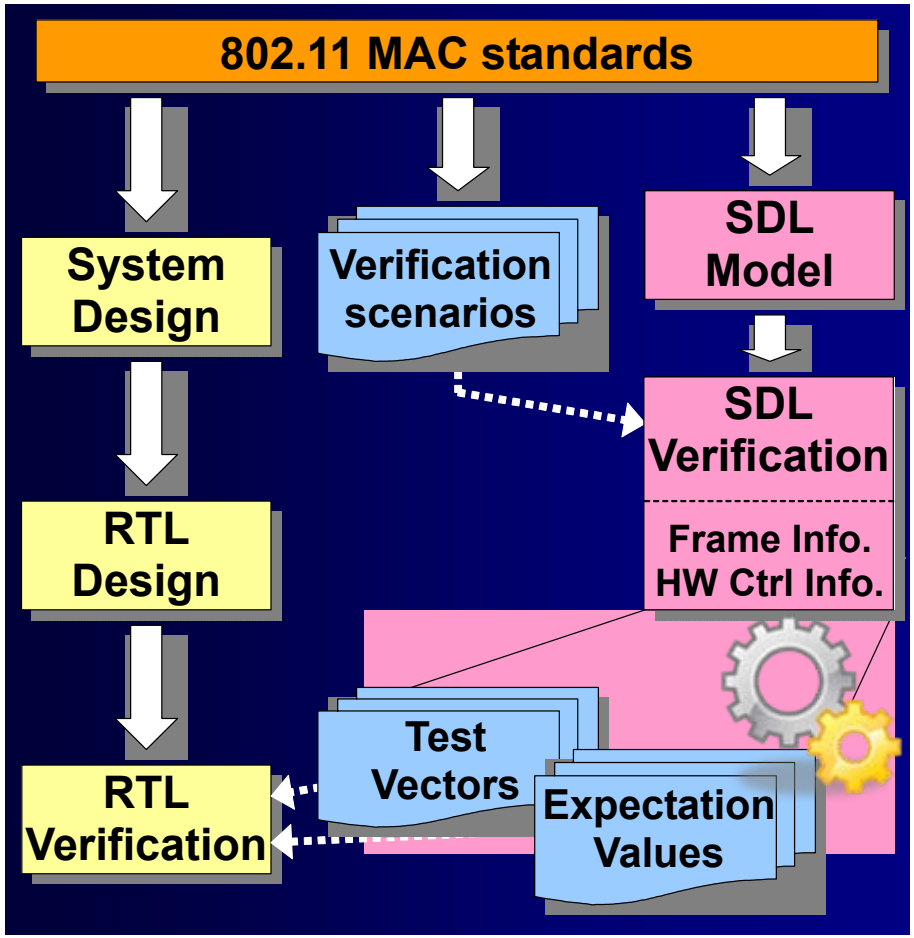
- **Frame information and HW control information are extracted during the SDL simulation.**
  - Frame info : Frame header, frame length.
  - HW control info : Parameters for registers or memories.

Test Vectors and Expectation Values Automatic Generation



- **Frame information and HW control information are extracted during the SDL simulation.**
  - Frame info : Frame header, frame length.
  - HW control info : Parameters for registers or memories.

Test Vectors and Expectation Values Automatic Generation

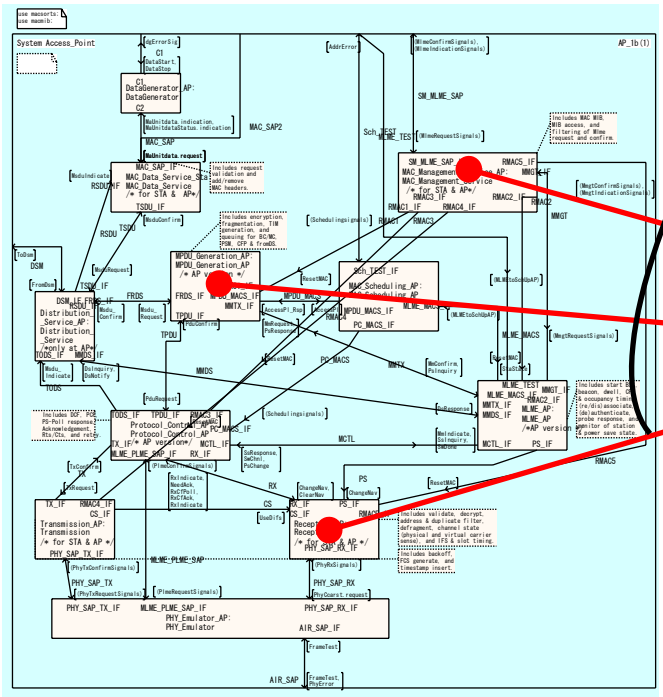


- Frame information and HW control information are extracted during the SDL simulation.
- Test vectors and expectation values are automatically generated.

How Automatic generation works

Verification Scenarios

Simulation



SDL Model of 802.11 MAC

Frame info. and

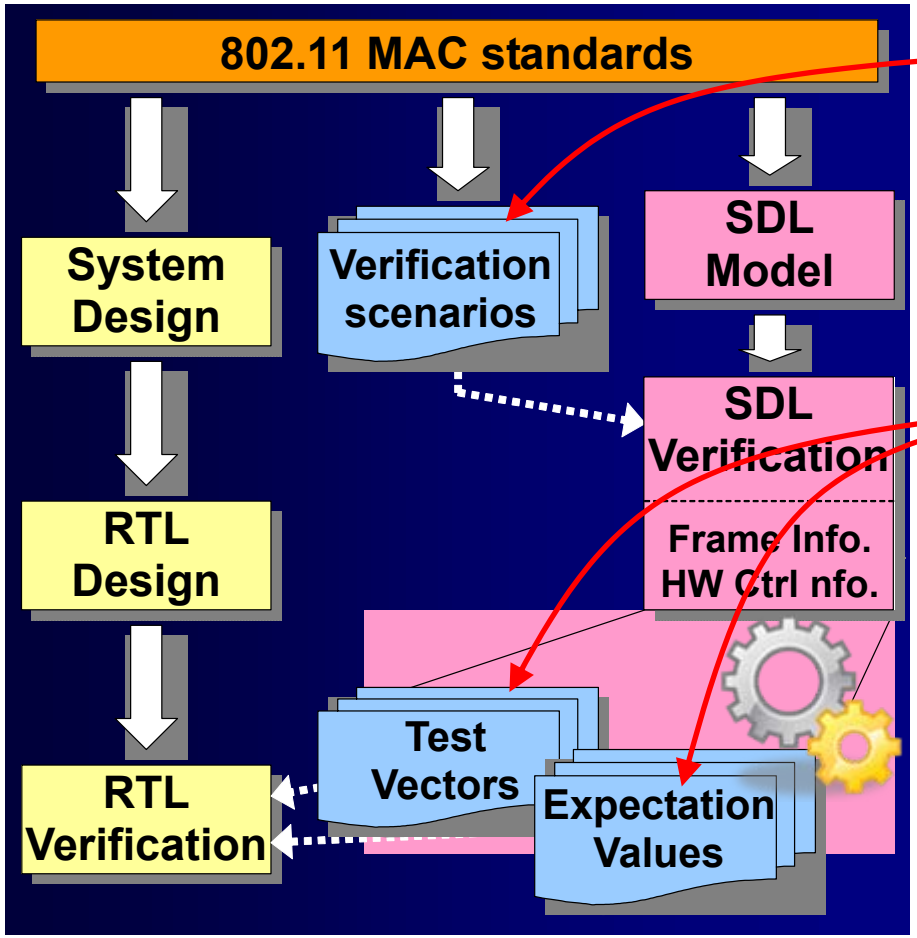
HW control info.

Process

Information Extraction

test vectors and expectation values

Summary of New Method



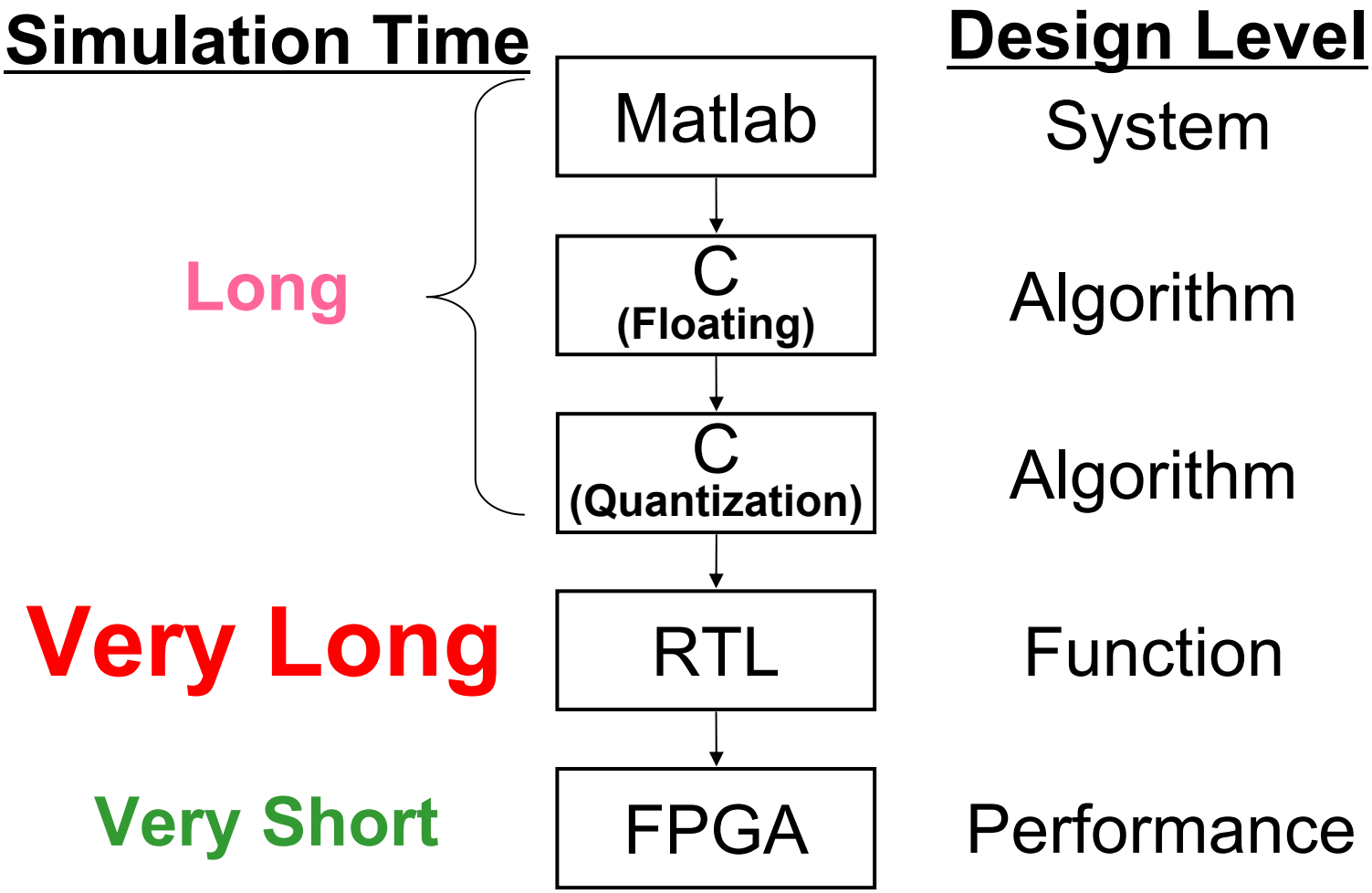
- Verification scenarios are validated, therefore, reliable.
- Test vectors and expectation values are automatically generated.

New method is reliable and efficient.

Outline

- Design and Verification method of MAC
- **Design and Verification method of PHY**
- Design method of Ultra Low Power Wireless BB SoC
- Summary

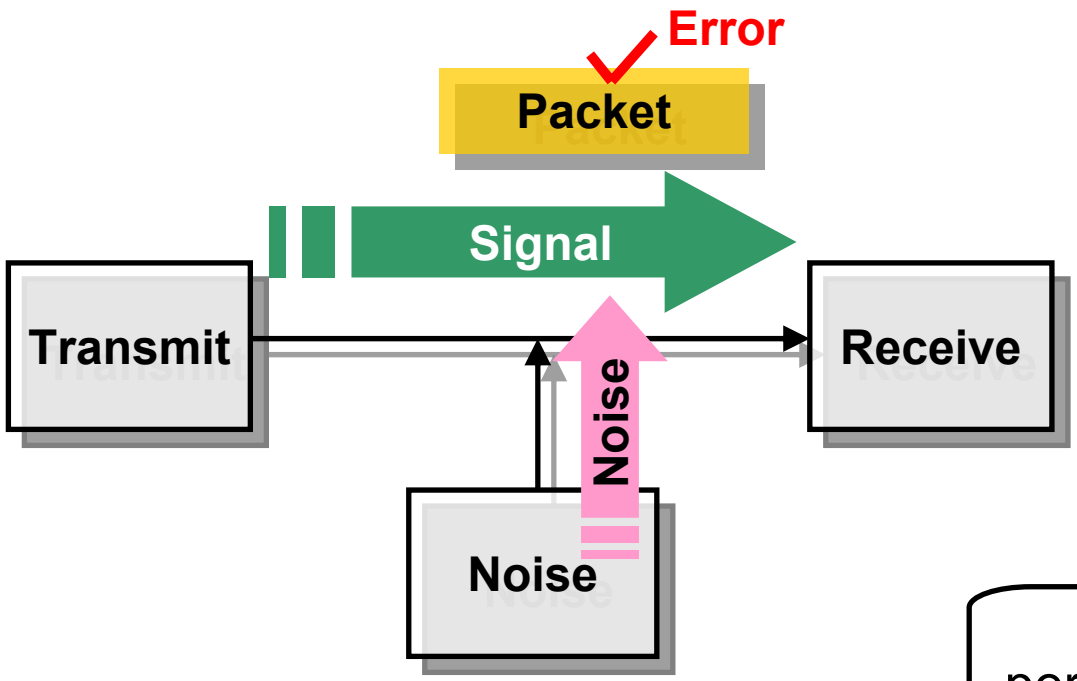
PHY Design Flow

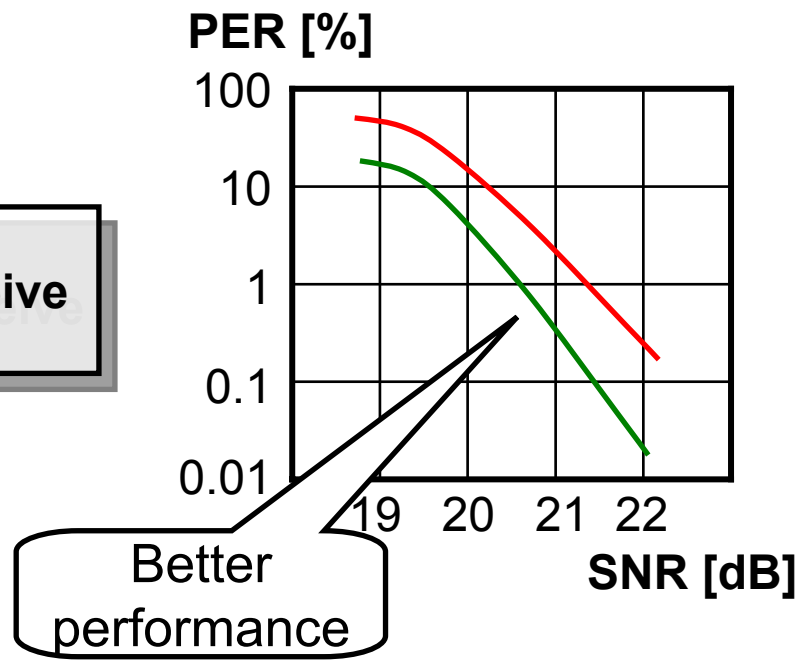


- **In each design step, SNR-PER is evaluated.**

SNR-PER (Signal-to-Noise Ratio to Packet Error Rate)

- **SNR-PER is the key metric to measure PHY performance.**

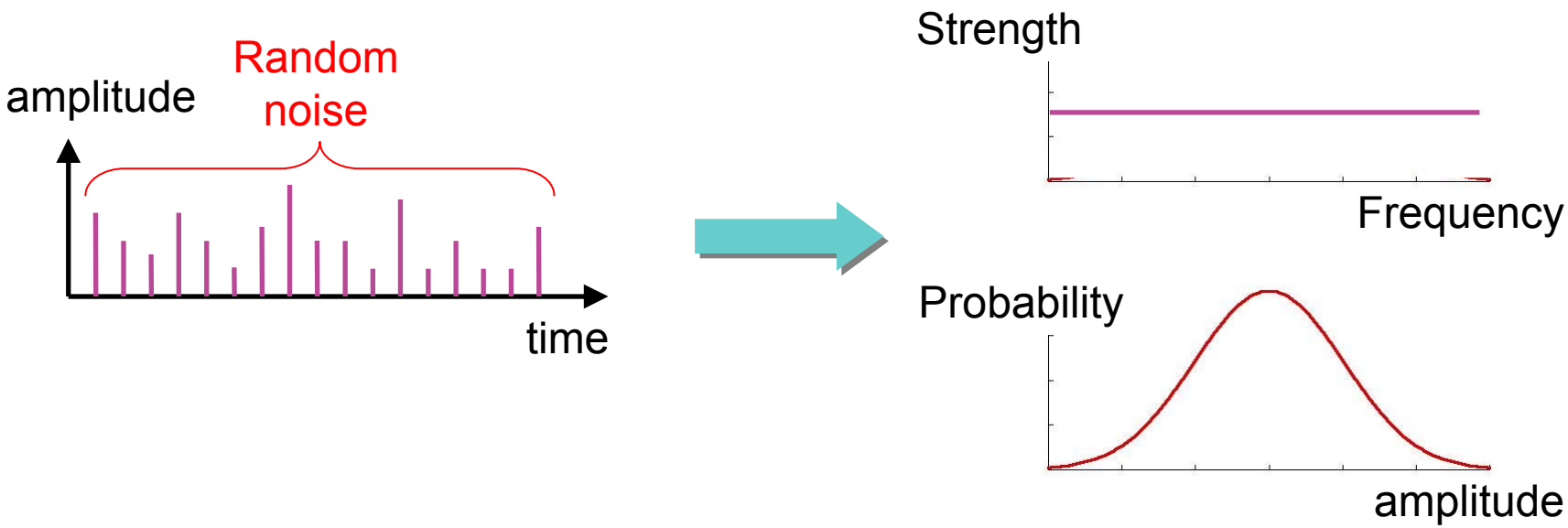




- **SNR-PER depends on the noise model, therefore, accurate noise model is important to evaluate SNR-PER.**
- **AWGN is used as a basic noise model.**

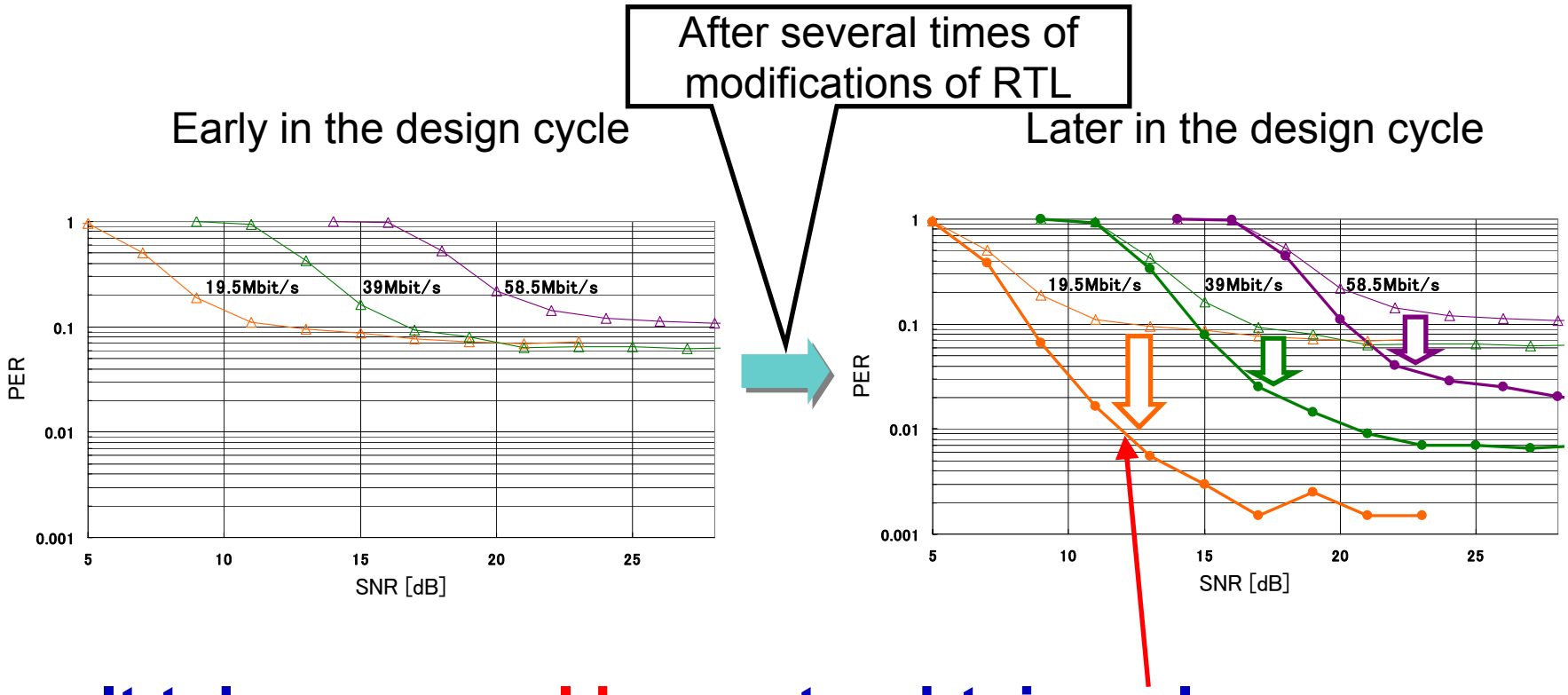
AWGN (Additive White Gaussian Noise)

- **Linear random noise**
  - Constant spectrum density.
  - Its noise amplitude has normal distribution.



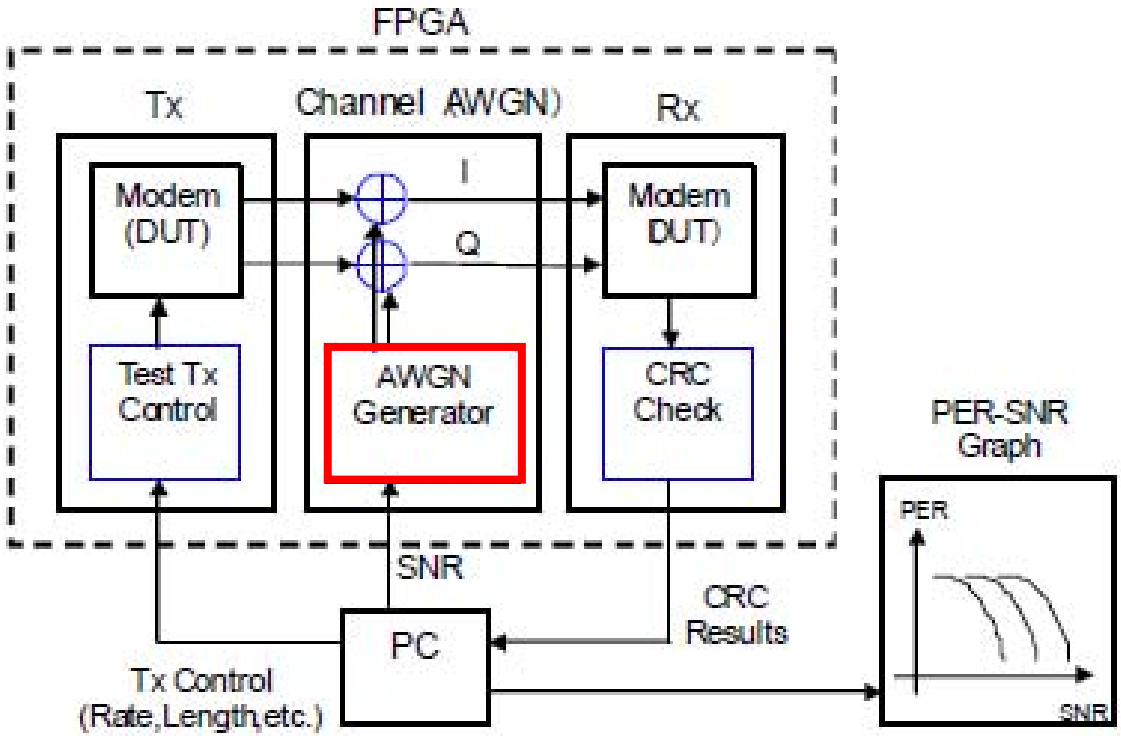
- **In RTL simulation, C function C_RAND() is often used to generate accurate random noise.**
- **RTL simulation is too slow!**

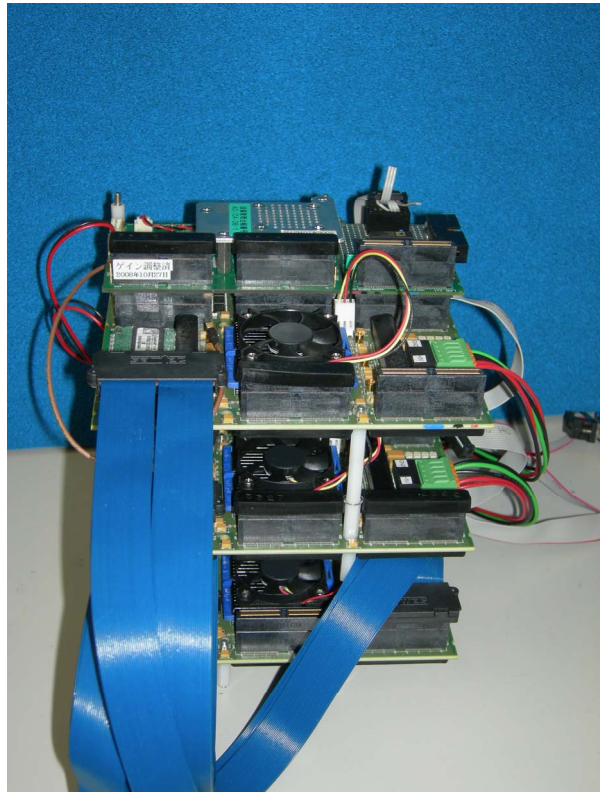
How slow the RTL simulation is



- **It takes several hours to obtain only one curve by RTL simulation.**
- **It takes a full day (sometimes more days) to have only one modification of RTL.**

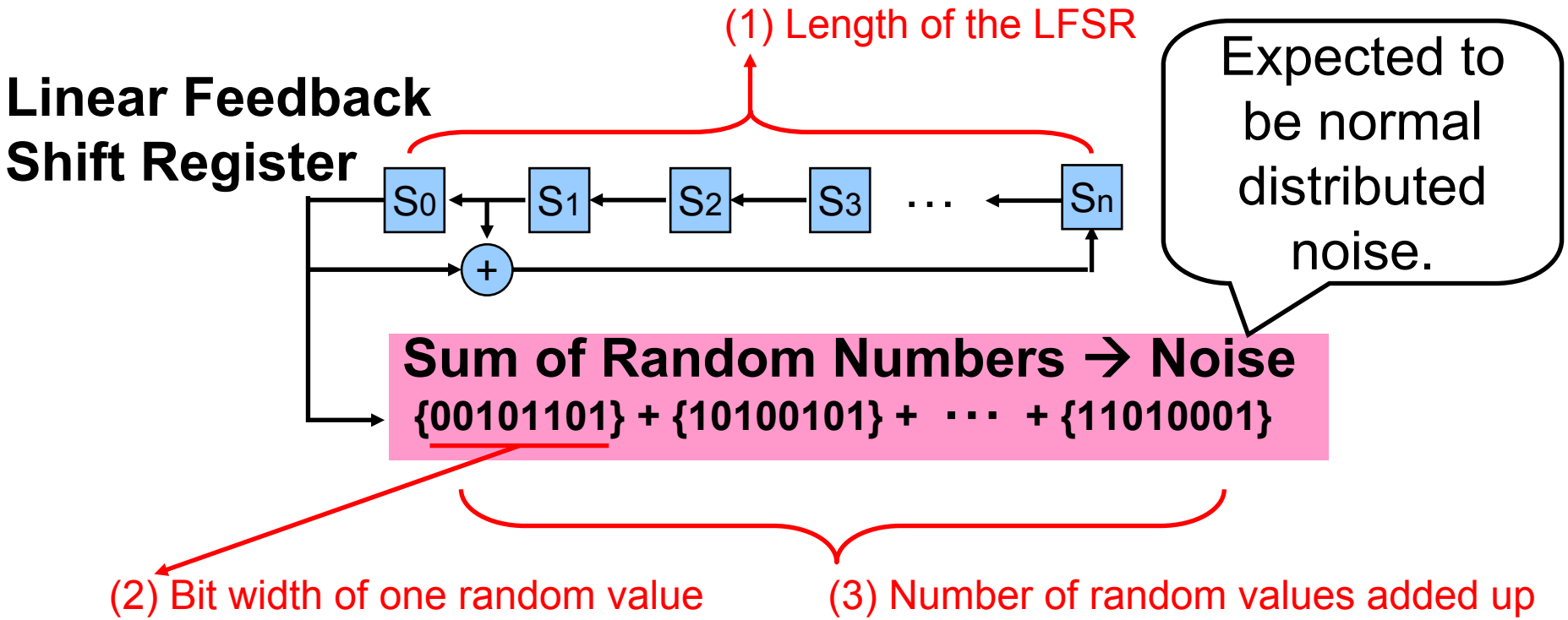
FPGA-based Validation Environment





- **Can FPGA model generate accurate AWGN noise like C model?**

AWGN Generator



- **LFSR generates pseudo-random numbers.**
- **Summation of some pseudo-random numbers becomes normal distribution (Central Limit Theorem).**
- **Three parameters are optimized with Taguchi method.**

Taguchi Method

- **Uses Design of Experiments (DoE) with orthogonal arrays to explore parameter space.**
- **Yields optimized parameters.**
- **Goal to optimize the parameters**
  - Error margin ration of PER between FPGA model and C model is less than 10 %:

$$\frac{|\ PER\ (FPGA) - PER\ (C)\ |}{PER\ (C)} < 10\ \%$$

  - Optimization is done for 3 points of SNR values: 19dB, 20dB and 21dB in 54 Mbps mode of 802.11a.

DoE (Design of Experiments)

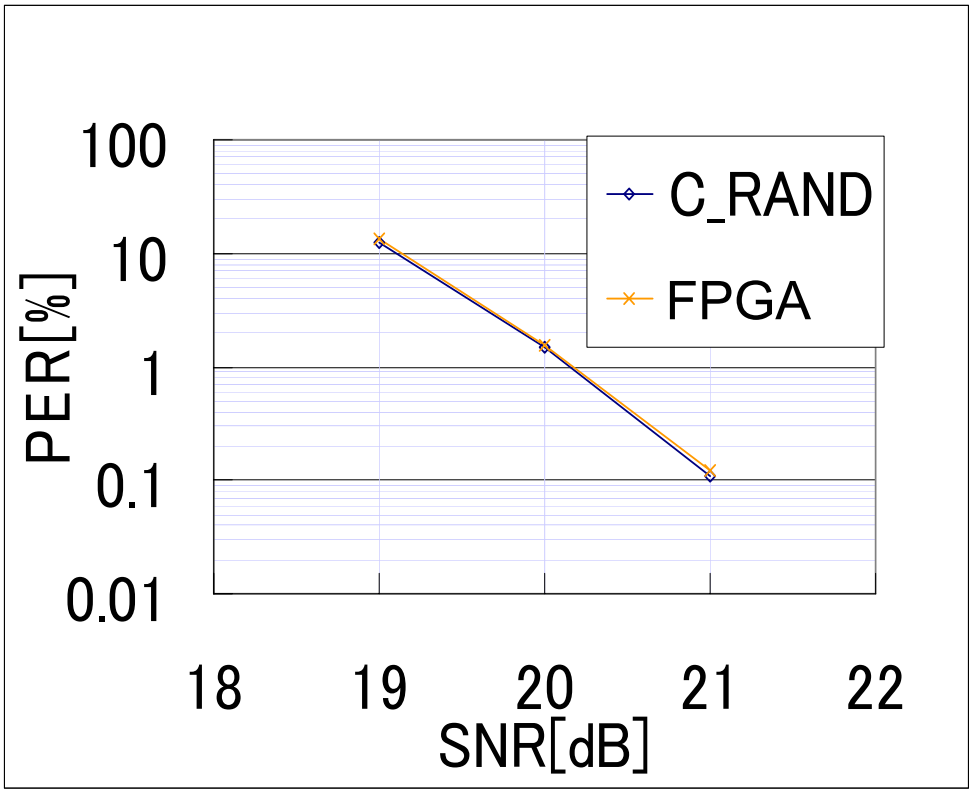
- **DoE is based on a full factorial design with 2 levels (High/Low) for each parameters.**

	Parameter 1	Parameter 2	Parameter 3
FPGA Simulation 1	L	L	L
FPGA Simulation 2	H	L	L
FPGA Simulation 3	L	H	L
FPGA Simulation 4	H	H	L
FPGA Simulation 5	L	L	H
FPGA Simulation 6	H	L	H
FPGA Simulation 7	L	H	H
FPGA Simulation 8	H	H	H

- **Through those experiments, the most effective parameter is found.**
- **With few more experiments, the optimized parameters are determined.**

Result of Comparison with C Model

- **SNR-PER from the FPGA model matches that from the C model very well.**

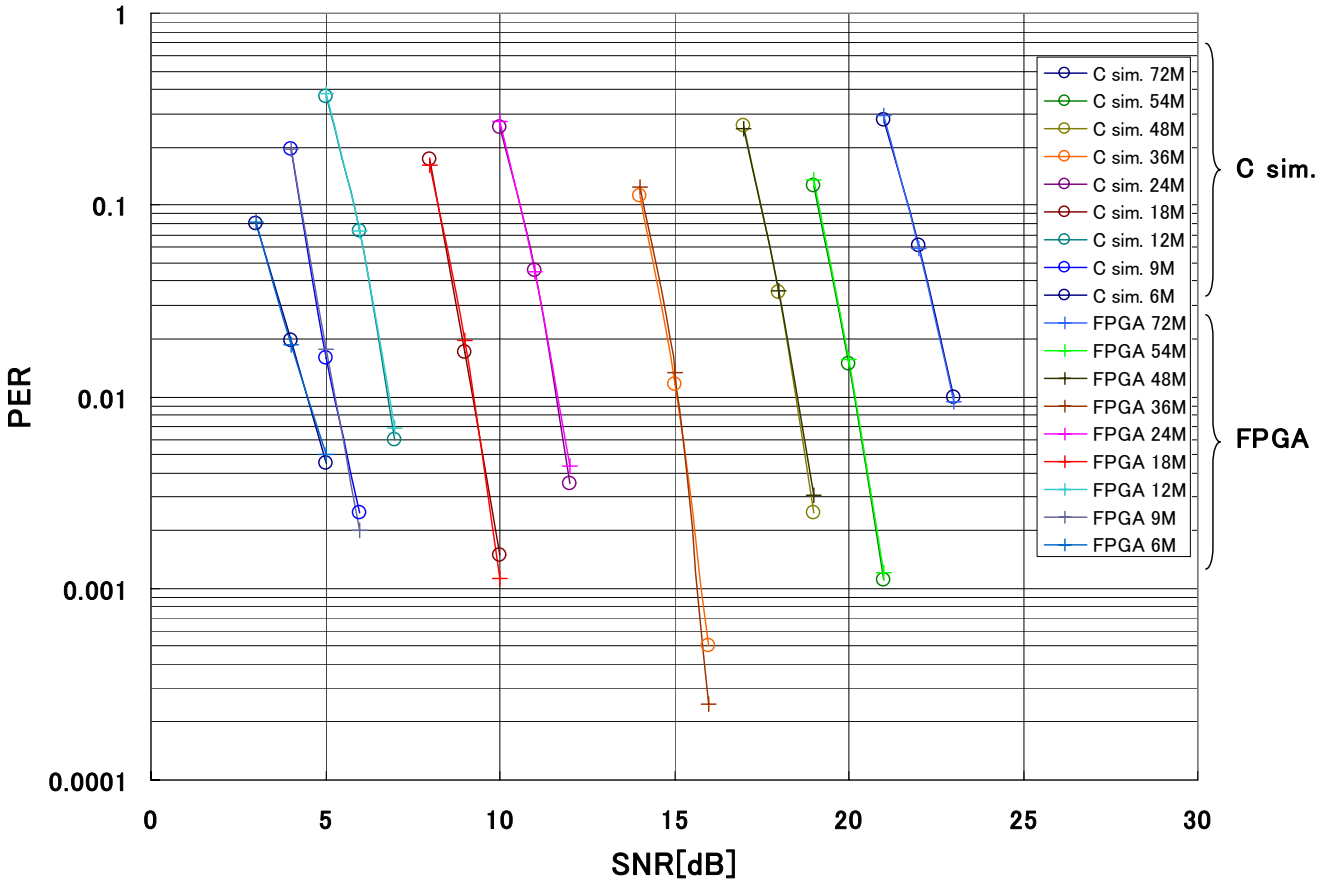


- **This result is obtained with the parameters optimized for 54 Mbps mode of 802.11a.**
- **What about the other modes?**

Error margin ratio of PER between FPGA model and C model is only 7.8%.

Result for Other Data Rates

- **Again, the FPGA model matches the C model very well for all the data rates of 802.11a.**



Summary of New Method for PHY

- New FPGA-based environment gives an accurate and fast method for the evaluation of SNR-PER for all the data rate of 802.11a.
- Using this environment, the total design period of PHY has drastically decreased.

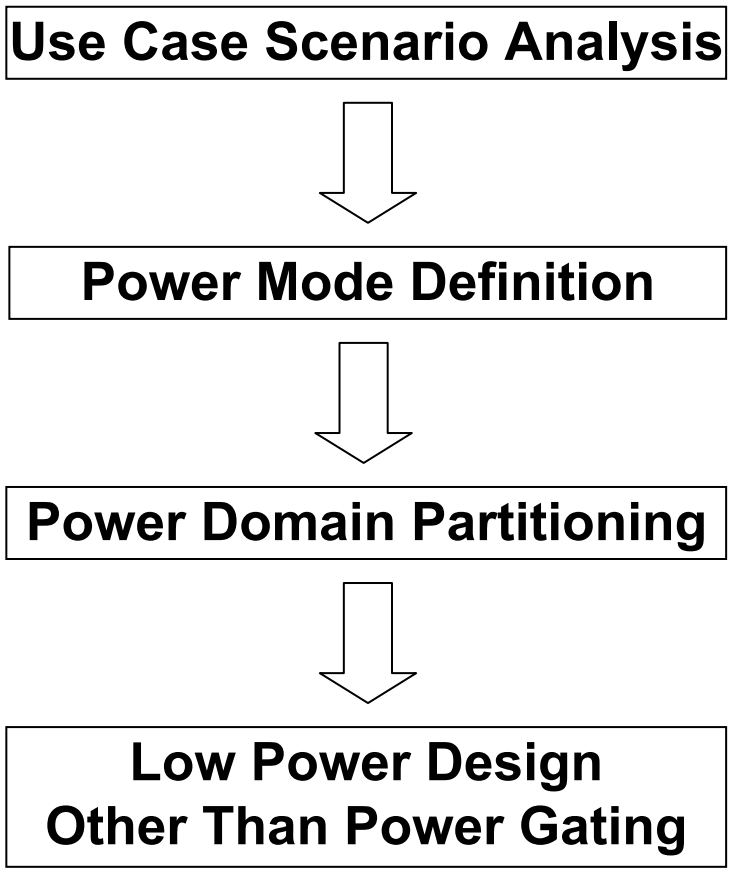
Outline

- Design and Verification method of PHY
- Design and Verification method of MAC
- **Design method of Ultra Low Power Wireless BB SoC**
- Summary

Top-Down Design is the Key

- There are so many low power technologies from the system level to the physical level.
- The higher level of technologies yields the bigger effects of low power.
- Therefore, low power design should take a top-down approach.

Top-Down Design Flow for Low Power



For Power Gating Design

- **The power gating has the biggest impact on low power.**

Use Case Scenario

Use Case Scenario Analysis

↓

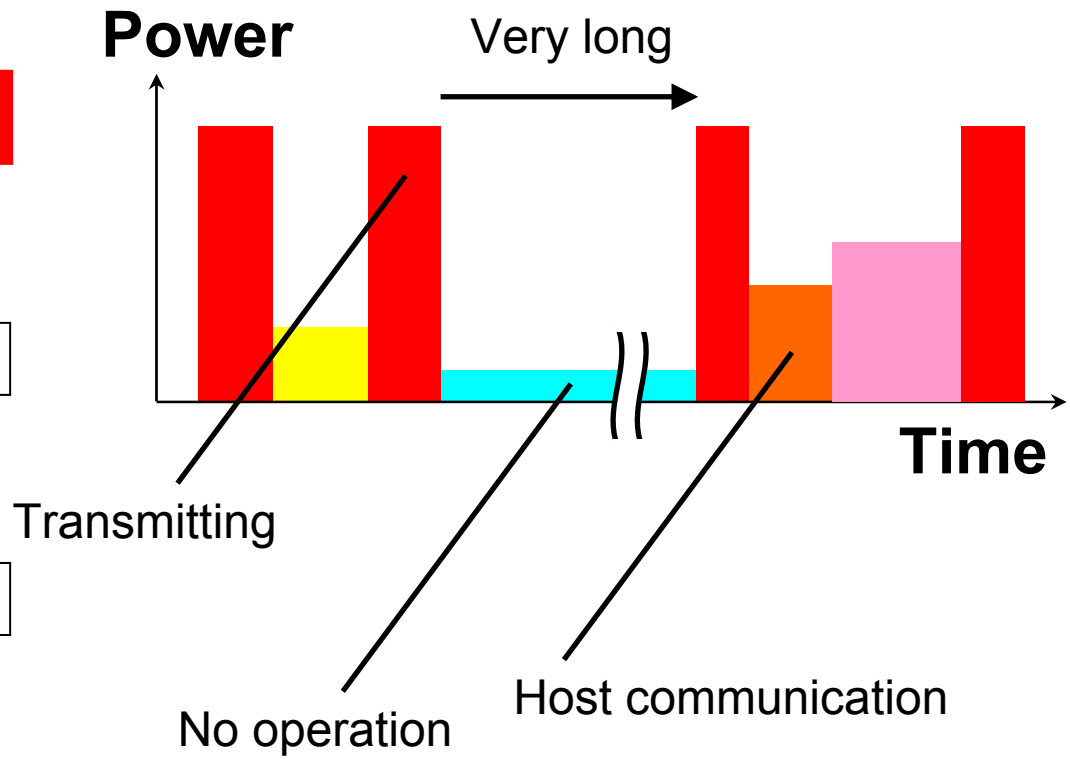
Power Mode Definition

↓

Power Domain Partitioning

↓

Low Power Design
Other Than Power Gating



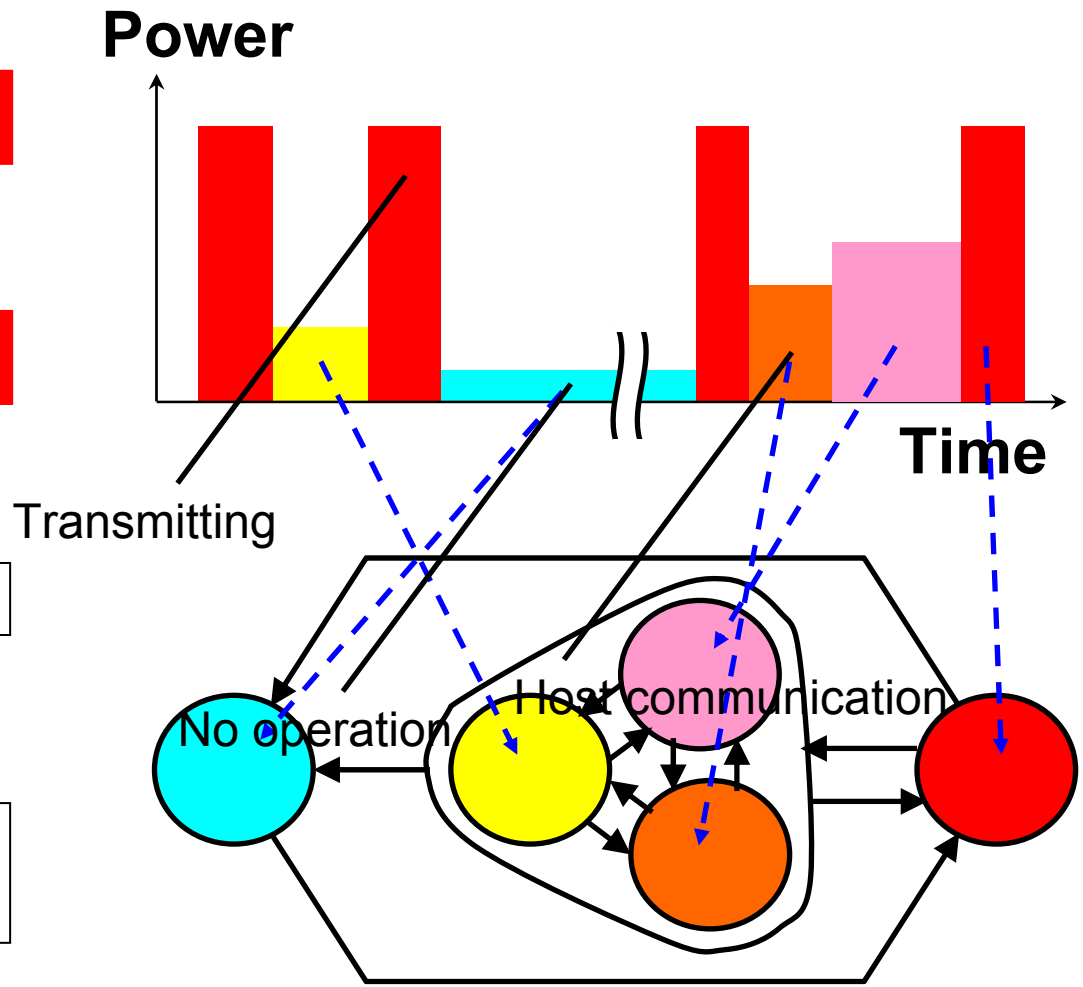
Power Mode Definition

Use Case Scenario Analysis

Power Mode Definition

Power Domain Partitioning

- Full Operation
- Receive Standby
- Host Communication
- Sleep
- Deep-Sleep



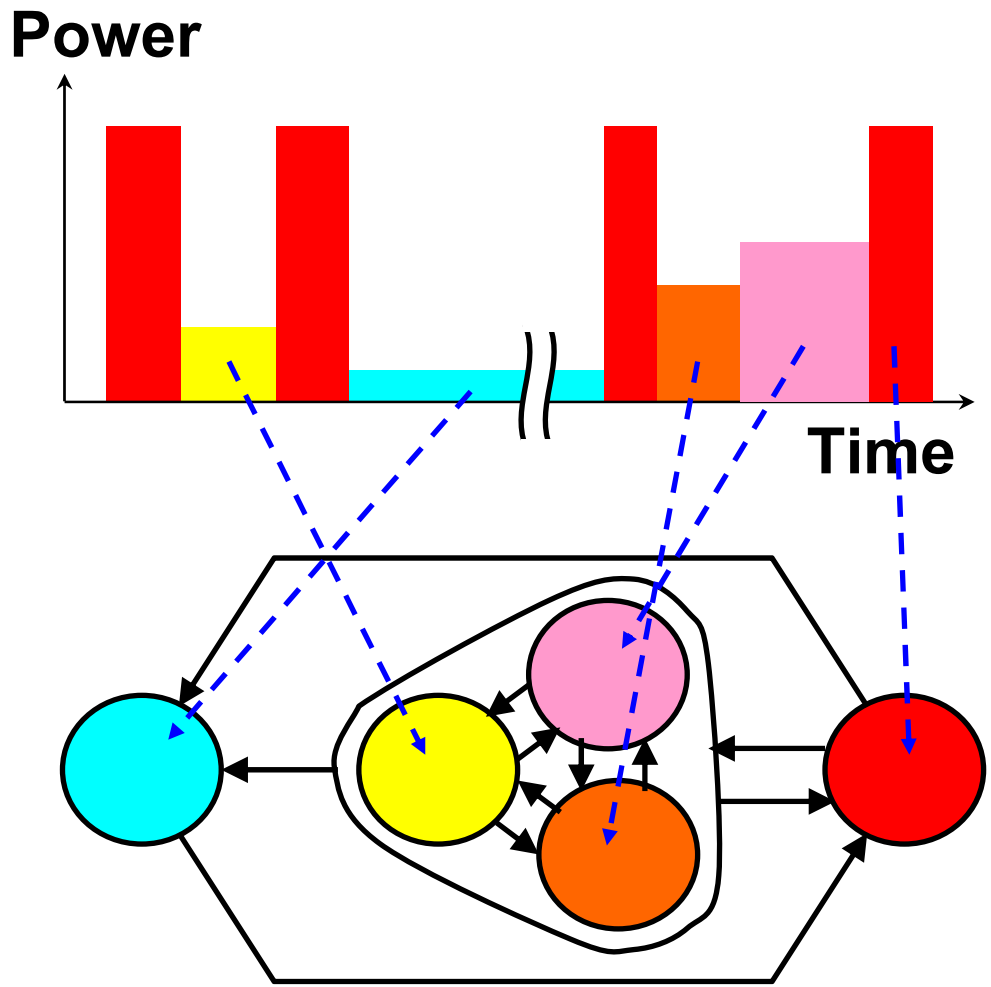
Power Domain Partitioning

Use Case Scenario Analysis

Power Mode Definition

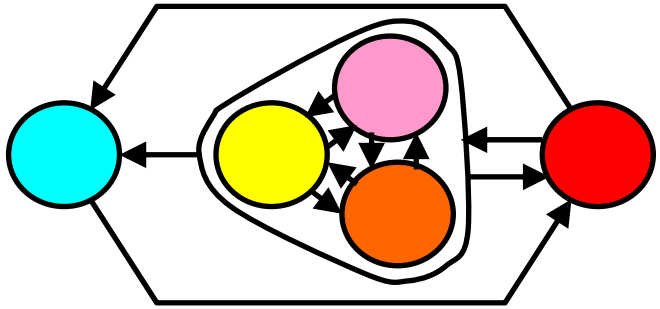
Power Domain Partitioning

- Full Operation
- Receive Standby
- Host Communication
- Sleep
- Deep-Sleep



Power Domain Partitioning

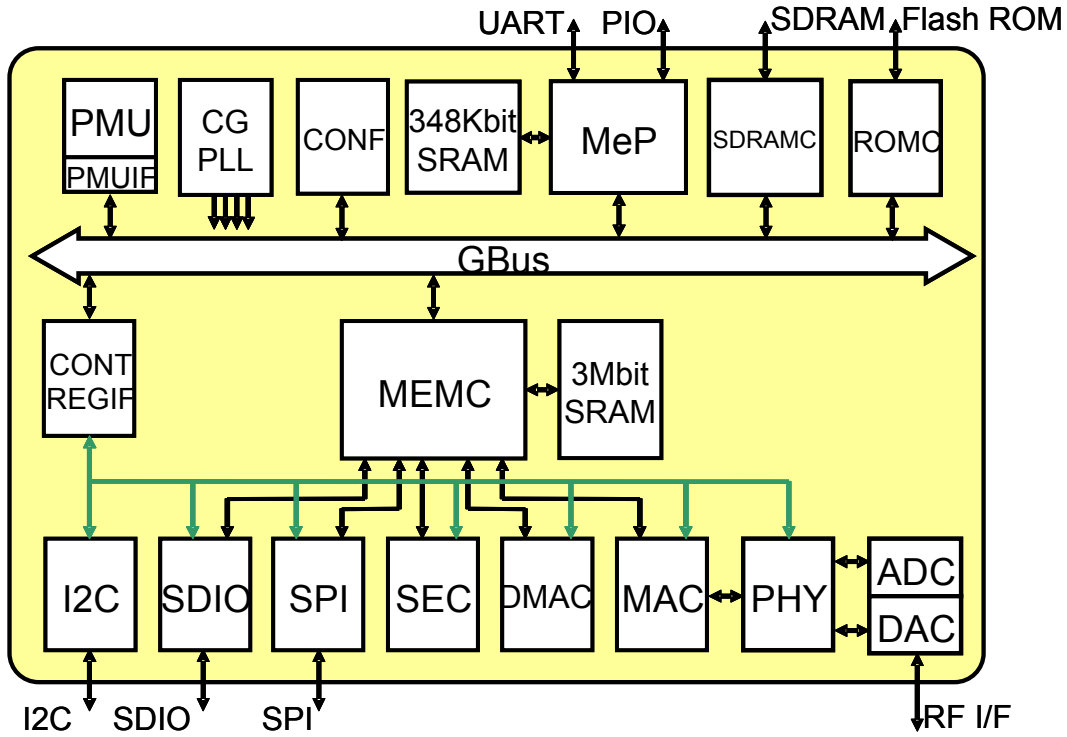
Use Case Scenario Analysis



Power Mode Definition

Power Domain Partitioning

- **Full Operation**
- **Receive Standby**
- **Host Communication**
- **Sleep**
- **Deep-Sleep**



Full Operation Mode

Use Case Scenario Analysis

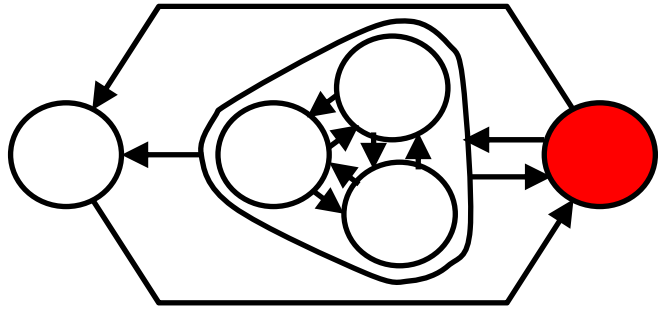
⇩

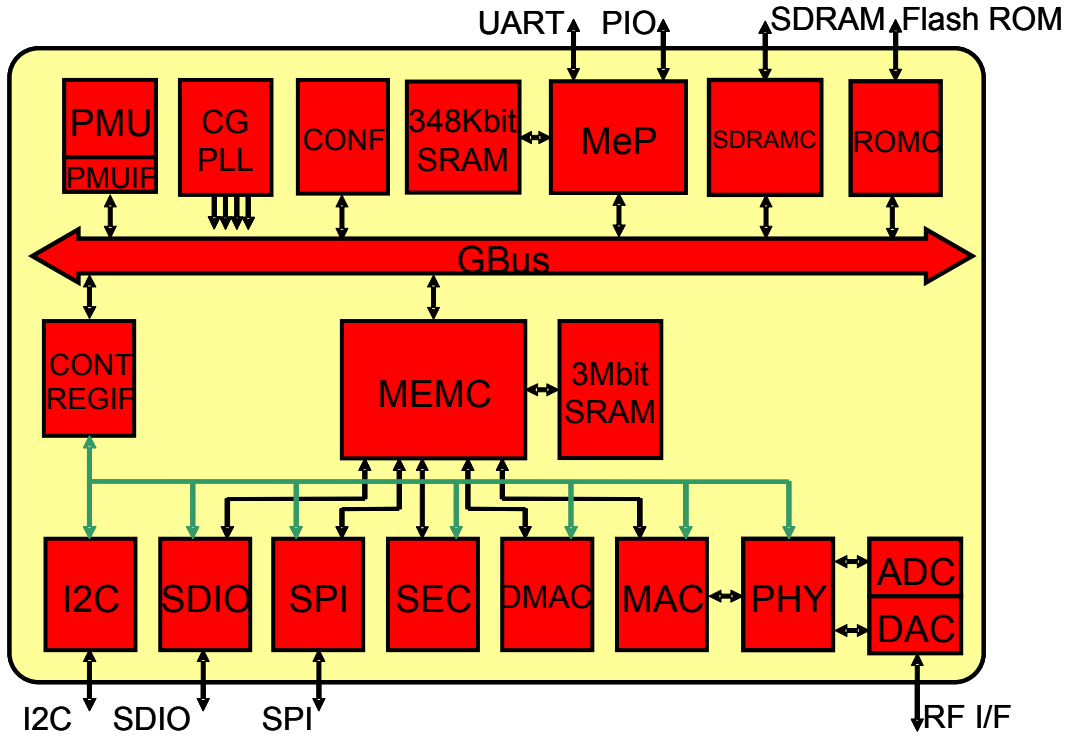
Power Mode Definition

⇩

Power Domain Partitioning

Full Operation
Receive Standby
Host Communication
Sleep
Deep-Sleep





Receive Standby Mode

Use Case Scenario Analysis

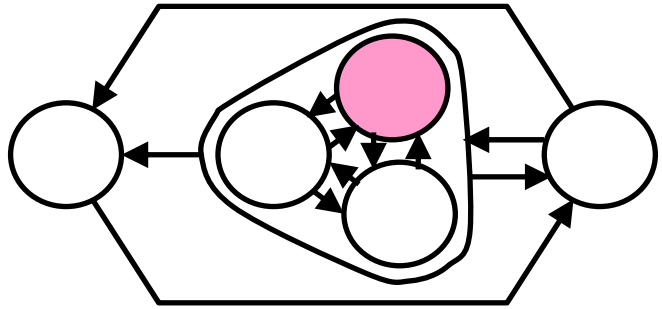
⇩

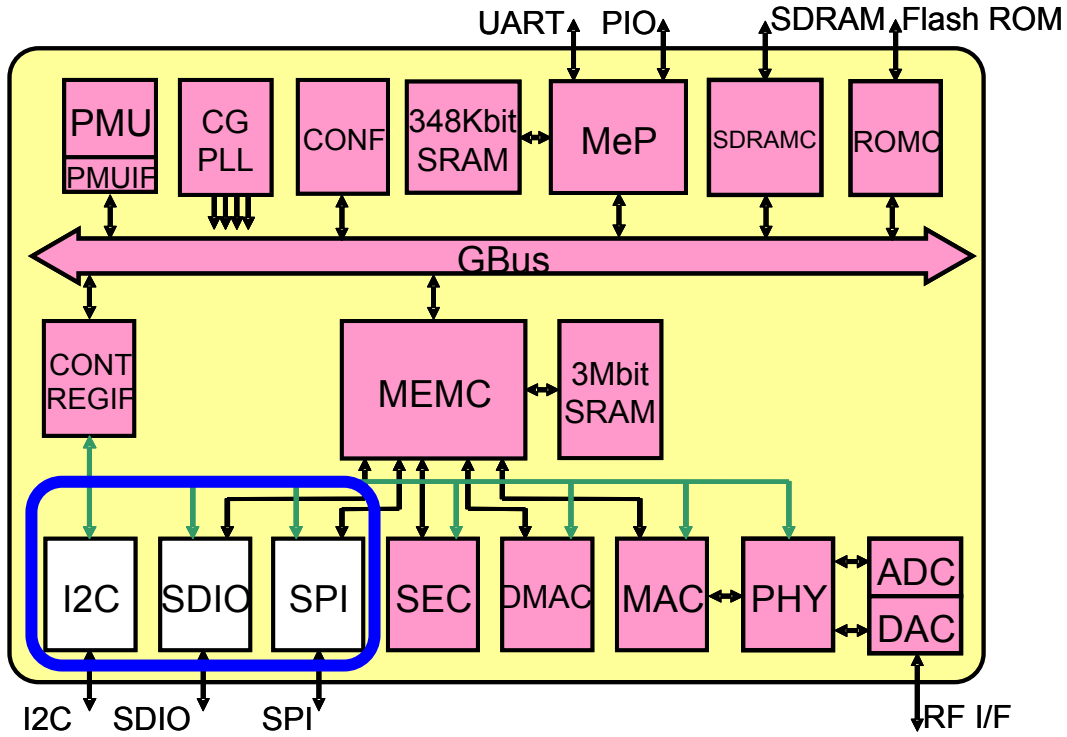
Power Mode Definition

⇩

Power Domain Partitioning

Full Operation
Receive Standby
Host Communication
Sleep
Deep-Sleep





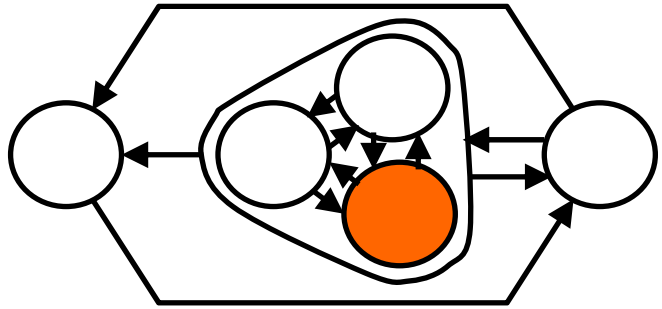
Host Communication Mode

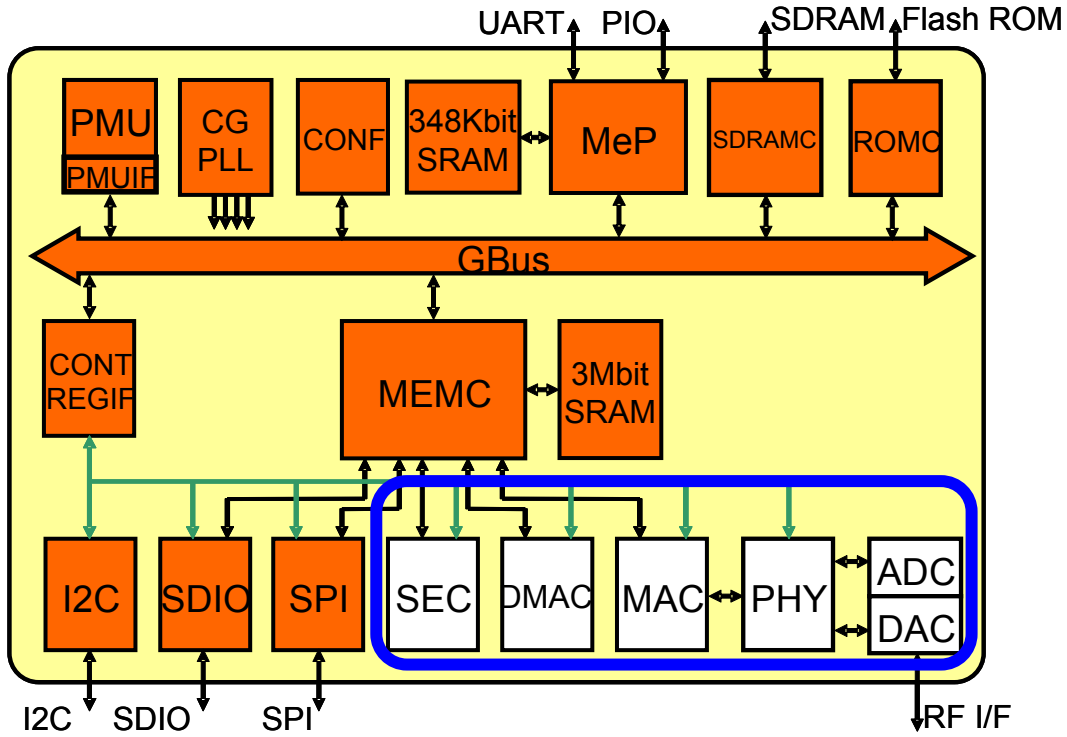
Use Case Scenario Analysis

Power Mode Definition

Power Domain Partitioning

Full Operation
Receive Standby
Host Communication
Sleep
Deep-Sleep





Sleep Mode

Use Case Scenario Analysis

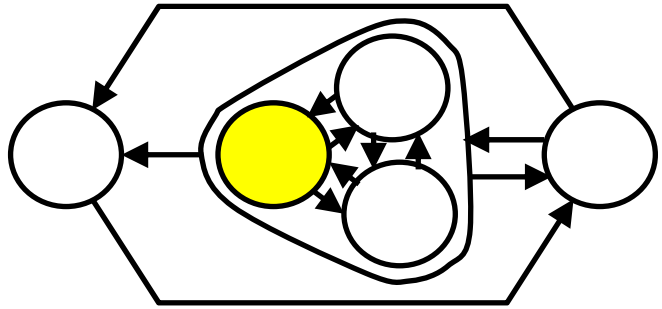
⇩

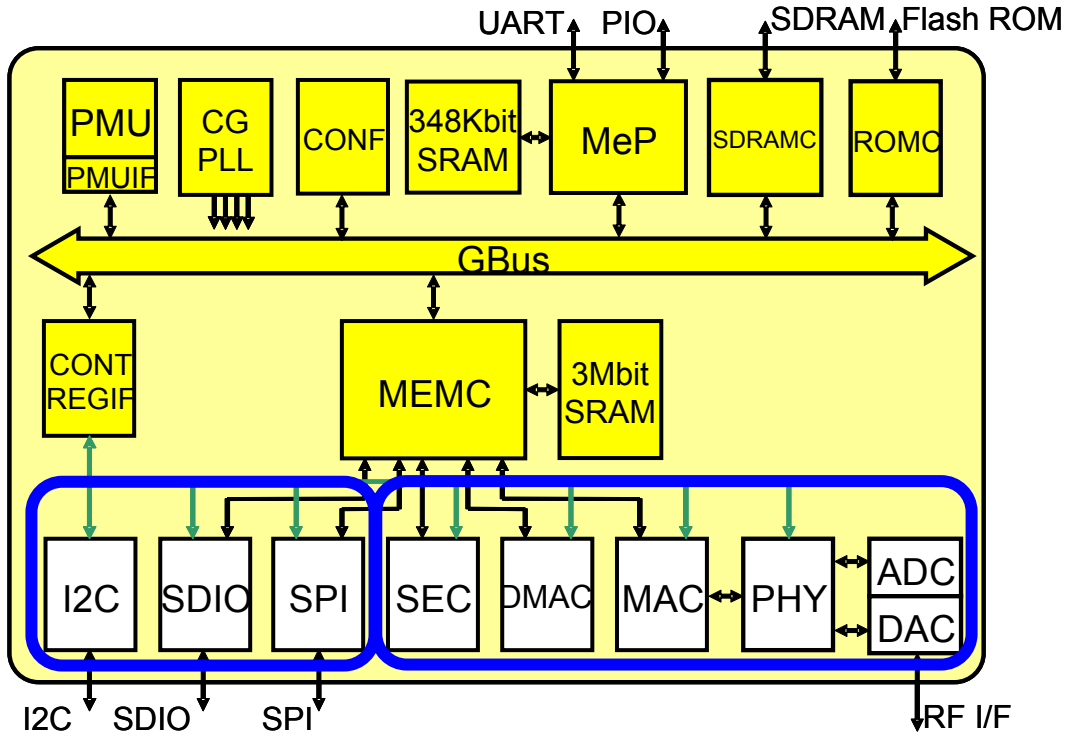
Power Mode Definition

⇩

Power Domain Partitioning

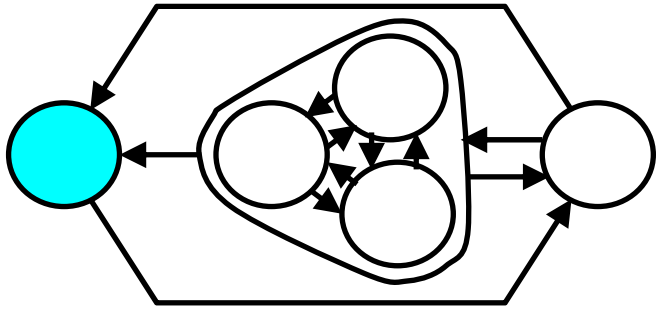
Full Operation
Receive Standby
Host Communication
Sleep
Deep-Sleep





Deep-Sleep Mode

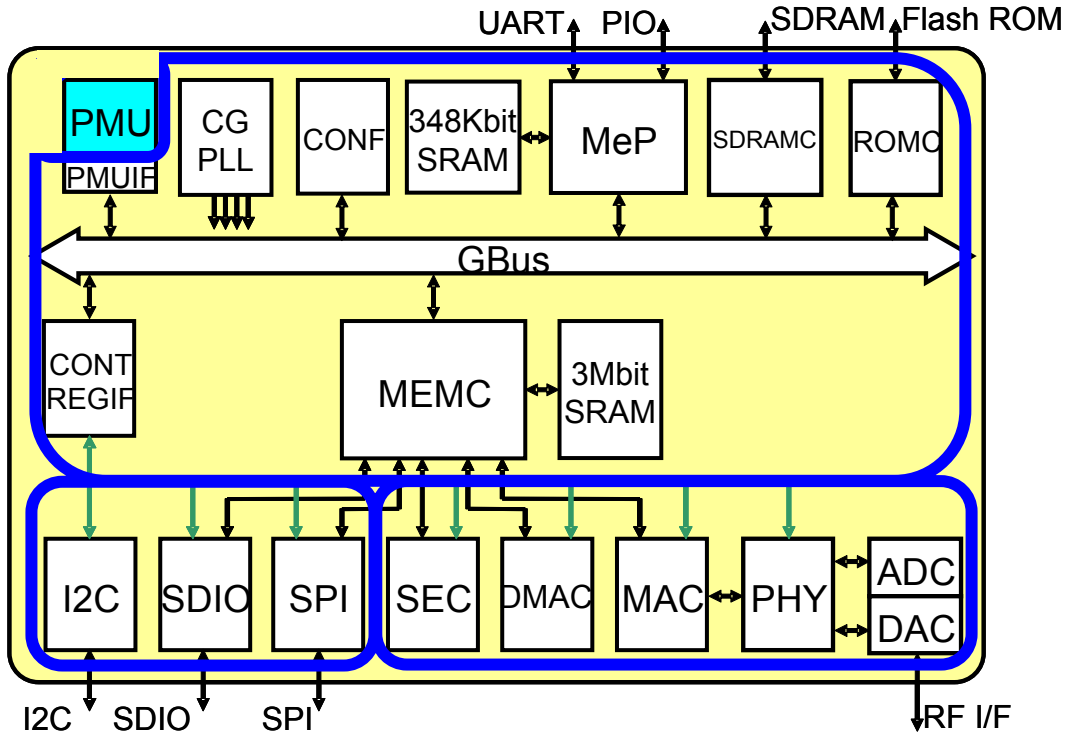
Use Case Scenario Analysis



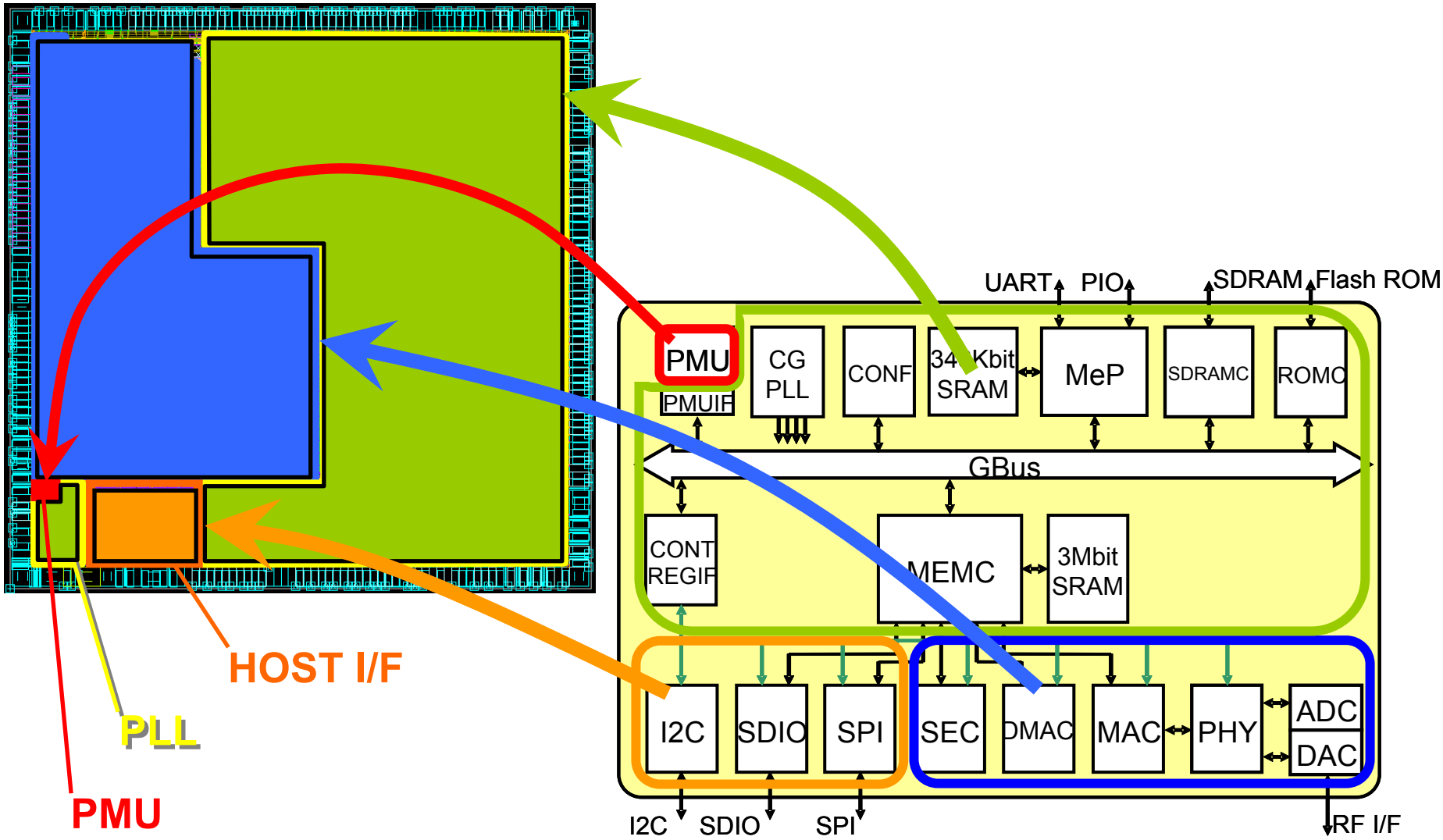
Power Mode Definition

Power Domain Partitioning

Full Operation
Receive Standby
Host Communication
Sleep
Deep-Sleep



Layout Result



Top Down Power Design Flow

Use Case Scenario Analysis

↓

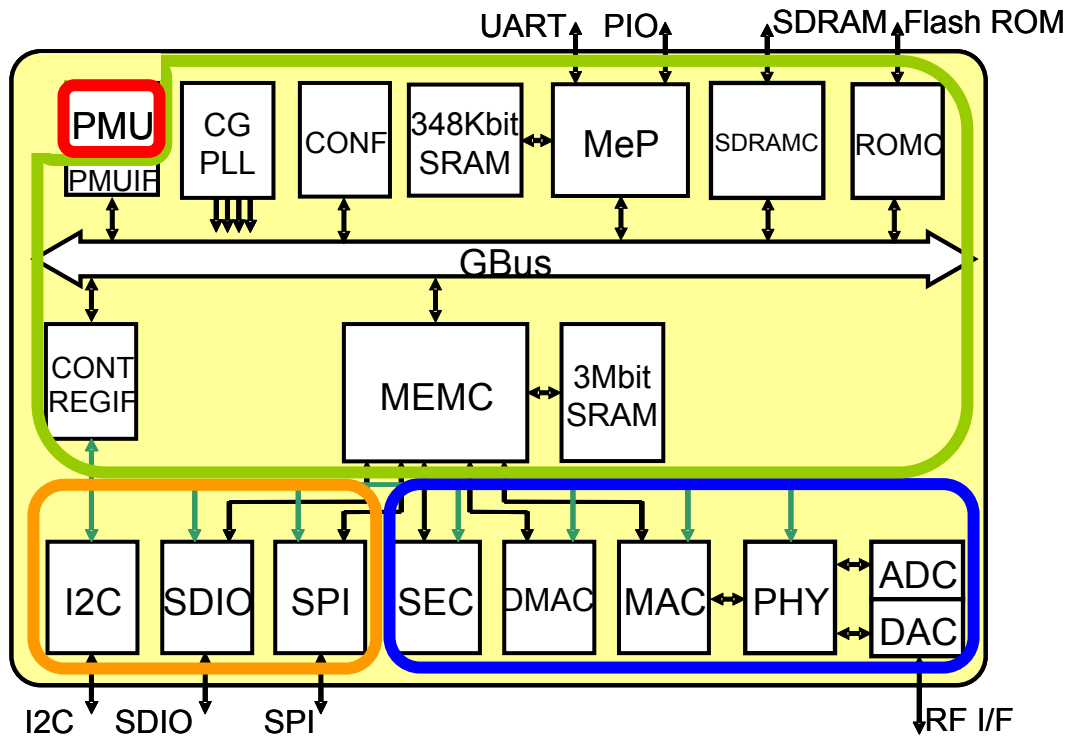
Power Mode Definition

↓

Power Domain Partitioning

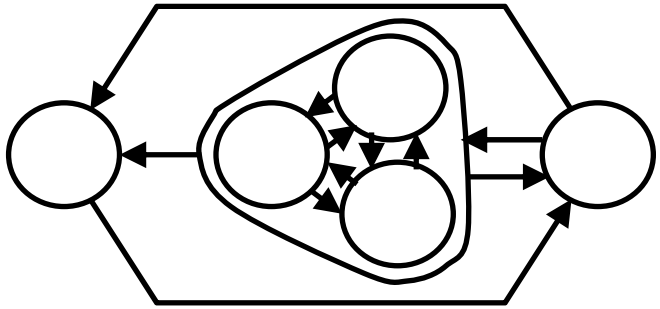
↓

Low Power Design Other Than Power Gating



Top Down Power Design Flow

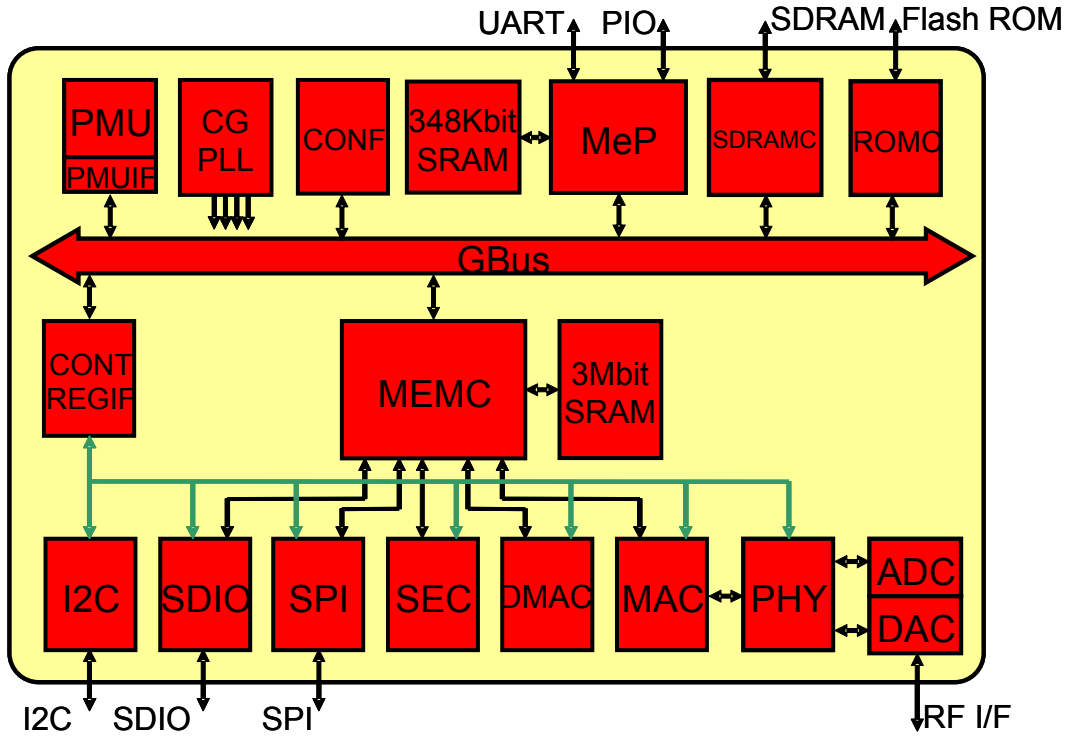
Use Case Scenario Analysis



Power Mode Definition

Power Domain Partitioning

Low Power Design
Other Than Power Gating



Applied Low Power Techniques Other Than Power Gating

- **Dynamic frequency scaling (DFS)**
  - 160/80 MHz CPU Clock → 40/20 MHz in Sleep mode
- **Clock gating**
- **Low-power flip-flops**
  - Conditional data-mapping flip-flops
  - Low power flip-flops with the optimized design parametes
- **Multi-Vth**
  - High-Vth / Low-Vth
- **Thick gate-oxide transistors for PMU**

Result of Power Estimation

	Estimated Power	BB	AD/DA	HOST	CPU	PLL	PMU
Full Operation	80 mW	ON	ON	ON	ON	ON	ON
Receive Standby		ON	ON	OFF	ON	ON	ON
Host Communication		OFF	OFF	ON	ON	ON	ON
Sleep	1.5 mW	OFF	OFF	OFF	ON	ON	ON
Deep-Sleep	22 uW	OFF	OFF	OFF	OFF	OFF	ON

The ultra low power chip TC90535XBG is being fabricated.

Summary of Today's Talk

- **New SDL-based MAC hardware design and verification method has been introduced.**
  - Test vectors and expectation values are automatically generated. Verification has become very reliable and efficient.
- **New FPGA-based PHY hardware design and verification method has been introduced.**
  - HW Noise generator is constructed. SNR-PER evaluation has become very fast and its result is very accurate.
- **Top-down ultra low power design method for wireless LAN BB SoC has been developed.**
  - Both operation power of 80mW and deep-sleep power of 22uW are estimated quite low.


Thankyou