Design and Verification Methods of Toshiba’s Wireless LAN Baseband SoC

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Toshiba WLAN Baseband SoC Series

- **TC90515XBG**
  - Over 30 Mbps on TCP/IP.
  - Build-in DTCP (Digital Transmission Content Protection).
  - Suitable for HD (High-Definition) video transmission.

- **TC90525XBG**
  - 20 Mbps on TCP/IP.
  - Small-sized, low-cost chip.
  - Suitable for various embedded systems like consumer electronics, security cameras, toys and so on.

- **TC90535XBG**
  - 20 Mbps on TCP/IP.
  - Ultra low power.
  - Suitable for various low power mobile devices.
Requirements of WLAN Baseband SoC

• **MAC layer** must conform with many specifications, authentication tests, radio laws of each country.
  – A great deal of verification is needed for MAC hardware.
• **PHY layer** is composed of many complicated signal processing circuits.
• **PHY layer** is difficult to evaluate its wireless performance.
  – Wireless performance is not guaranteed only by clock speed. Packet error rate (PER) is also a crucial metric.
  – But, RTL simulation to evaluate PER takes very long time.
• **Low Power** is becoming increasingly necessary for WLAN SoC.
  – WLAN are getting installed into much more mobile devices.
  – Ever-increasing data rate and multi antennas are pushing up power.
  – Ultra low power design method is needed.
Outline

• Design and Verification method of MAC
• Design and Verification method of PHY
• Design method of Ultra Low Power Wireless BB SoC
• Summary
Outline

• Design and Verification method of MAC
• Design and Verification method of PHY
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• Summary
MAC Needs Lots of Verification

• Standards
  – 802.11a / b / g / n / e / h / i / k, …
    • Each having complicated protocols:
      – CDMA/CA, PCF, DCF, Backoff, Ad Hoc, RTS/CTS, …

• Authentication tests
  – Wi-Fi tests
  – Interoperability tests

• Laws
  – Radio Law, Technical Regulations Conformity Certification (Japan)
  – Federal Communications Commission (US)

Efficient and Reliable verification method is needed.
**Conventional MAC Verification Method**

- **Reliability problem**
  - Many complicated MAC protocols.
  - Some scenarios may be wrong or lacking due to human errors.
  - Verification scenarios not validated.

- **Efficiency problem**
  - Many test vectors and expectation values are made by human hand.
  - It’s cumbersome and time-consuming.
New MAC Verification Method

- SDL is introduced.
New MAC Verification Method

- SDL is introduced.
- MAC is modeled by SDL.
What is SDL?

• **Specification and Description Language**
  – Formal language standardized by ITU-T.
  – Describes specification **without ambiguity**.
  – Its model can be verified by the SDL simulator.

  – It’s usually used for software development, but we use it for **hardware** development.

ITU-T : International Telecommunication Union
Telecommunication Standardization Sector
SDL Model of MAC

- Top diagram of 802.11 Access Point

System Access_Point

DataGenerator_AP

Includes MAC MIB, MIB access, and filtering of MLme request and confirm.

MAC_Management_Service_AP

MAC_Data_Service_Sta

Includes request validation and add/remove MAC headers.

Includes encryption, fragmentation, TIM generation, and queuing for BC/MC, PSM, CFP & fromDS.

MPDU_Generation_AP

MAC_Scheduling_AP

Distribution_Service_AP

MLME_AP

Includes start BSS, beacon, dwell, CFP & occupancy timing, (re/dis)associate, (de)authenticate, probe response, and monitor of station & power save state.

Includes DCF, PCF, PS-Poll response, Acknowledgement, Rts/Cts, and retry.

Protocol_Control_AP

Transmission_AP

Reception_AP

Includes validate, decrypt, address & duplicate filter, defragment, channel state (physical and virtual carrier sense), and IFS & slot timing.

Includes backoff, FCS generate, and timestamp insert.

PHY_Emulator_AP

MAC_SAP2

MaUnitdata.request

Sch_TEST

AddrError

MLME_TEST

C1
dgErrorSig

DataStart,

DataStop

C1
C2

SM_MLME_SAP

(MlmeConfirmSignals),

(MlmeIndicationSignals)

(MlmeRequestSignals)

SM_MLME_SAP_IF

MAC_SAP

MaUnitdata.indication,

MaUnitdataStatus.indication

MaUnitdata.request

MAC_SAP_IF

RMAC5_IF

MMGT_IF

(MmgtRequestSignals)

(MmgtConfirmSignals),

(MmgtIndicationSignals)

RSDU_IF

RMAC2_IF

ResetMAC

TSDU_IF

RMAC1_IF

ResetMAC

RMAC3_IF

ResetMAC

RMAC4_IF

Sch_TEST_IF

DSM

ToDsm

FromDsm

DSM_IF

RSDU

MsduIndicate

RSDU_IF

TSDU_IF RMAC1_IF

FRDS_IF

RMAC2_IF

MMGT_IF

MmRequest,

PsResponse

MmConfirm,

PsInquiry

MMTX_IF

TODS_IF MMDS_IF

MLME_MACS

(MLMEtoSchUpAP)

StaState

MLME_MACS_IF

MLME_TEST

RMAC2_IF

MMTX

MmRequest,

PsResponse

MmConfirm,

PsInquiry

MMTX_IF

TODS

Msdu_Indicate

TODS_IF TPDU_IF RMAC3_IF

MMDSDsInquiry,DsNotify

DsResponse

MMDS_IF

PC_MACS_IF

TX_IF

TX

TxRequest

TxConfirm

MCTL_IF

SsResponse,SwChnl,

PsChange

MmIndicate,

SsInquiry,SwDone

MCTL_IF PS_IF

PS

ChangeNav

MLME_PLME_SAP_IF

RX_IF

TX_IF RMAC4_IF

RX

RxIndicate,

NeedAck,

RxCfPoll,

RxCfAck,

RxIndicate

ChangeNav,

ClearNav

RX_IF PS_IF

CS_IF

UseDifs

PHY_SAP_TX_IF

PHY_SAP_TX

(PhyTxRequestSignals)

(PhyTxConfirmSignals)

PHY_SAP_RX_IF

PHY_SAP_RX

PhyCcarst.request

(PhyRxSignals)

PHY_SAP_TX_IF MLME_PLME_SAP_IF PHY_SAP_RX_IF

AIR_SAP_IF

FrameTest,

PhyError

FrameTest
Scenarios Validation

*Scenarios are validated with the SDL model by using SDL simulator.*
Scenarios Validation

- Scenarios are validated with the SDL model by using SDL simulator.
- The simulator outputs MSC (Message Sequence Chart).
196 fundamental scenarios are prepared for 802.11a/e/h

- Complicated scenarios can be constructed from the fundamental ones.

<table>
<thead>
<tr>
<th>Category</th>
<th>Number of scenarios</th>
</tr>
</thead>
<tbody>
<tr>
<td>HCCA</td>
<td>34</td>
</tr>
<tr>
<td>EDCA</td>
<td>18</td>
</tr>
<tr>
<td>Management</td>
<td>6</td>
</tr>
<tr>
<td>802.11h</td>
<td>32</td>
</tr>
<tr>
<td>Sequence</td>
<td>23</td>
</tr>
<tr>
<td>Illegal input</td>
<td>68</td>
</tr>
<tr>
<td>Miscellaneous</td>
<td>15</td>
</tr>
<tr>
<td>Total</td>
<td>196</td>
</tr>
</tbody>
</table>
Test Vectors and Expectation Values Automatic Generation

- Frame information and HW control information are extracted during the SDL simulation.
  - Frame info: Frame header, frame length.
  - HW control info: Parameters for registers or memories.
Test Vectors and Expectation Values Automatic Generation

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  - Frame info: Frame header, frame length.
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Test Vectors and Expectation Values
Automatic Generation

- Frame information and HW control information are extracted during the SDL simulation.
- Test vectors and expectation values are automatically generated.
How Automatic generation works

Verification Scenarios

Simulation

SDL Model of 802.11 MAC

Process

Information Extraction

Frame info. and HW control info.

test vectors and expectation values
Summary of New Method

- Verification scenarios are validated, therefore, reliable.
- Test vectors and expectation values are automatically generated.

New method is reliable and efficient.
Outline

• Design and Verification method of MAC
• **Design and Verification method of PHY**
• Design method of Ultra Low Power Wireless BB SoC
• Summary
• In each design step, SNR-PER is evaluated.
**SNR-PER**
*(Signal-to-Noise Ratio to Packet Error Rate)*

- SNR-PER is the key metric to measure PHY performance.

SNR-PER depends on the noise model, therefore, accurate noise model is important to evaluate SNR-PER.

- AWGN is used as a basic noise model.
AWGN
(Additive White Gaussian Noise)

- Linear random noise
  - Constant spectrum density.
  - Its noise amplitude has normal distribution.

- In RTL simulation, C function `C_RAND()` is often used to generate accurate random noise.
- RTL simulation is too slow!
How slow the RTL simulation is

- It takes several hours to obtain only one curve by RTL simulation.
- It takes a full day (sometimes more days) to have only one modification of RTL.
FPGA-based Validation Environment

- Can FPGA model generate accurate AWGN noise like C model?
AWGN Generator

- LFSR generates pseudo-random numbers.
- Summation of some pseudo-random numbers becomes normal distribution (Central Limit Theorem).
- Three parameters are optimized with Taguchi method.

\[
\text{S0} + \text{S1} + \text{S2} + \text{S3} + \ldots + \text{Sn}
\]

- (1) Length of the LFSR
- (2) Bit width of one random value
- (3) Number of random values added up

Expected to be normal distributed noise.

\{00101101\} + \{10100101\} + \ldots + \{11010001\}
Taguchi Method

• Uses Design of Experiments (DoE) with orthogonal arrays to explore parameter space.
• Yields optimized parameters.
• Goal to optimize the parameters
  – Error margin ration of PER between FPGA model and C model is less than 10 %:
    \[
    \frac{|\text{PER (FPGA)} - \text{PER (C)}|}{\text{PER (C)}} < 10 \%
    \]
  – Optimization is done for 3 points of SNR values: 19dB, 20dB and 21dB in 54 Mbps mode of 802.11a.
DoE (Design of Experiments)

- DoE is based on a full factorial design with 2 levels (High/Low) for each parameter.

<table>
<thead>
<tr>
<th></th>
<th>Parameter 1</th>
<th>Parameter 2</th>
<th>Parameter 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPGA Simulation 1</td>
<td>L</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>FPGA Simulation 2</td>
<td>H</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>FPGA Simulation 3</td>
<td>L</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>FPGA Simulation 4</td>
<td>H</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>FPGA Simulation 5</td>
<td>L</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>FPGA Simulation 6</td>
<td>H</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>FPGA Simulation 7</td>
<td>L</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>FPGA Simulation 8</td>
<td>H</td>
<td>H</td>
<td>H</td>
</tr>
</tbody>
</table>

- Through those experiments, the most effective parameter is found.
- With few more experiments, the optimized parameters are determined.
SNR-PER from the FPGA model matches that from the C model very well.

This result is obtained with the parameters optimized for 54 Mbps mode of 802.11a.

What about the other modes?

Error margin ratio of PER between FPGA model and C model is only 7.8%.
Result for Other Data Rates

• Again, the FPGA model matches the C model very well for all the data rates of 802.11a.
Summary of New Method for PHY

• New FPGA-based environment gives an accurate and fast method for the evaluation of SNR-PER for all the data rate of 802.11a.
• Using this environment, the total design period of PHY has drastically decreased.
Outline

• Design and Verification method of PHY
• Design and Verification method of MAC
• **Design method of Ultra Low Power Wireless BB SoC**
• Summary
Top-Down Design is the Key

- There are so many low power technologies from the system level to the physical level.
- The higher level of technologies yields the bigger effects of low power.
- Therefore, low power design should take a top-down approach.
Top-Down Design Flow for Low Power

Use Case Scenario Analysis

Power Mode Definition

Power Domain Partitioning

Low Power Design Other Than Power Gating

For Power Gating Design

- The power gating has the biggest impact on low power.
Use Case Scenario

Use Case Scenario Analysis

Power Mode Definition

Power Domain Partitioning

Low Power Design Other Than Power Gating

Power

Time

Very long

Transmitting

No operation

Host communication
Power Mode Definition

Use Case Scenario Analysis

Power Mode Definition

Power Domain Partitioning

<table>
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<tr>
<td>Full Operation</td>
</tr>
<tr>
<td>Receive Standby</td>
</tr>
<tr>
<td>Host Communication</td>
</tr>
<tr>
<td>Sleep</td>
</tr>
<tr>
<td>Deep-Sleep</td>
</tr>
</tbody>
</table>

Diagram:
- Power Mode: No operation, Host communication, Transmitting, Host communication, Sleep, Deep-Sleep
- Time: Transmitting, Power

Legend:
- No operation
- Host communication
- Transmitting
Power Domain Partitioning

Use Case Scenario Analysis

Power Mode Definition

Power Domain Partitioning

- Full Operation
- Receive Standby
- Host Communication
- Sleep
- Deep-Sleep

Power

Time
Power Domain Partitioning

Use Case Scenario Analysis

Power Mode Definition

Power Domain Partitioning

Full Operation
Receive Standby
Host Communication
Sleep
Deep-Sleep
Full Operation Mode

Use Case Scenario Analysis

Power Mode Definition

Power Domain Partitioning

Full Operation
Receive Standby
Host Communication
Sleep
Deep-Sleep
Receive Standby Mode

Use Case Scenario Analysis

Power Mode Definition

Power Domain Partitioning

Full Operation
Receive Standby
Host Communication
Sleep
Deep-Sleep
Host Communication Mode

Use Case Scenario Analysis

Power Mode Definition

Power Domain Partitioning

- Full Operation
- Receive Standby
- Host Communication
- Sleep
- Deep-Sleep
Sleep Mode

Use Case Scenario Analysis

Power Mode Definition

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Full Operation
Receive Standby
Host Communication
Sleep
Deep-Sleep
Deep-Sleep Mode

Use Case Scenario Analysis

Power Mode Definition

Power Domain Partitioning

- Full Operation
- Receive Standby
- Host Communication
- Sleep
- Deep-Sleep
Top Down Power Design Flow

Use Case Scenario Analysis

Power Mode Definition

Power Domain Partitioning

Low Power Design Other Than Power Gating
Top Down Power Design Flow

Use Case Scenario Analysis

Power Mode Definition

Power Domain Partitioning

Low Power Design Other Than Power Gating
Applied Low Power Techniques Other Than Power Gating

- **Dynamic frequency scaling (DFS)**
  - 160/80 MHz CPU Clock → 40/20 MHz in Sleep mode
- **Clock gating**
- **Low-power flip-flops**
  - Conditional data-mapping flip-flops
  - Low power flip-flops with the optimized design parameters
- **Multi-Vth**
  - High-Vth / Low-Vth
- **Thick gate-oxide transistors for PMU**
## Result of Power Estimation

<table>
<thead>
<tr>
<th>State</th>
<th>Estimated Power</th>
<th>BB</th>
<th>AD/DA</th>
<th>HOST</th>
<th>CPU</th>
<th>PLL</th>
<th>PMU</th>
</tr>
</thead>
<tbody>
<tr>
<td>Full Operation</td>
<td>80 mW</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
</tr>
<tr>
<td>Receive Standby</td>
<td></td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
</tr>
<tr>
<td>Host Communication</td>
<td></td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
</tr>
<tr>
<td>Sleep</td>
<td>1.5 mW</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
</tr>
<tr>
<td>Deep-Sleep</td>
<td>22 uW</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
</tr>
</tbody>
</table>

The ultra low power chip TC90535XBG is being fabricated.
Summary of Today’s Talk

• New SDL-based MAC hardware design and verification method has been introduced.
  – Test vectors and expectation values are automatically generated. Verification has become very reliable and efficient.

• New FPGA-based PHY hardware design and verification method has been introduced.
  – HW Noise generator is constructed. SNR-PER evaluation has become very fast and its result is very accurate.

• Top-down ultra low power design method for wireless LAN BB SoC has been developed.
  – Both operation power of 80mW and deep-sleep power of 22uW are estimated quite low.
Thank you