SoC for Car Navigation Systems with a 53.3 GOPS Image Recognition Engine

Jan. 20, 2010


*Renesas Technology Corporation,  **Hitachi Ltd.
Contents

1. Car navigation application requirement and new SoC
2. IMP-X : New Image Recognition Engine
3. Application Example of IMP-X
4. Summary
Advanced Car Navigation Systems

**Navigation**
- Driver friendly user interface and graphics

**Safety**
- Object Recognition
- Passive/Active Safety

**Amusement**
- Digital TV display
- Audio playback

Multi Applications assisting and entertaining our driving

The car is approaching.
Demanded Technology for Advanced Car navigation Systems

**Navigation**
- High Performance and various Graphic processing technology
- GPS technology

**Amusement**
- Multimedia interface technology
- Audio / video processing technology

**Safety**
- High performance embedded image recognition technology
- Connection with vehicle-control technology

**fundamental technology**
- High-performance MPU
- High speed bus and data I/O technology
- etc…
Products Lineup for Embedded Car Navigation Systems

Delivering advanced technology for 1-Chip Car Navigation Systems

- **SH-Navi1 (SH7770)**
  - CPU (400MHz), 2DG, 3DG, Vin, GPS, DDR1

- **SH-Navi2V (SH7774)**
  - CPU (600MHz), 2DG, Vin, Image Recog., DDR2

- **SH-Navi3 (SH7776)**
  - CPU x2 (533MHz), 2D/3DG., Image Recog., PCI Express, DDR3

- **SH-4A Dual core**
  - Integration of Image recognition (IMP-X)

Integration of Image recognition (IMP)

For high-end model

Year:
- ~2005
- 2006
- 2007
- 2008
- 2009
- 2010

The 15th ASPDAC ©2010. Renesas Technology Corp., All rights reserved.
Next Generation 1-Chip Solution : SH-Navi3

**SH-Navi3**

- **Core1**: SH-4A 533MHz
- **Core2**: SH-4A 533MHz

- 2D/3D Graphic Accelerator
- Image Recognition processing engine
- Video Input (3ch)
- Display Unit (2ch)
- DDR3-SDRAM memory interface (2ch)
- SuperHyway bus

**For multi-core system**

- **EXREAL Platform™**
  1. ExVisor : inter-OS prevention technology (Domain Separation)
  2. ExARIA : inter-OS communication interface (Domain interoperation)

**External Peripheral Interfaces** / USB2.0, CAN, PCI Express, ATA, etc...

**Memory (DDR3)**

**Domain1**
- App1
- OS1
- CPU1

**Domain2**
- App2
- OS2
- CPU2
Specification of SH-Navi3

<table>
<thead>
<tr>
<th></th>
<th>SH-Navi2V (SH7774)</th>
<th>SH-Navi3 (SH7776)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>90nm</td>
<td>65nm</td>
</tr>
<tr>
<td>CPU</td>
<td>SH-4A 600MHz (1080MIPS) FPU: 4.2 GFLOPS</td>
<td>SH-4A x 2 533MHz (960MIPS) x2 FPU: 7.46 GFLOPS</td>
</tr>
<tr>
<td>Cache</td>
<td>I: 32KB, D: 32KB</td>
<td>I: 32KB, D: 32KB, L2: 128KB</td>
</tr>
<tr>
<td>Image recognition engine</td>
<td>38.4 GOPS engine</td>
<td>53.3 GOPS engine Distortion Correction module</td>
</tr>
<tr>
<td>Graphics IP</td>
<td>2D accelerator</td>
<td>2D/3D accelerator PowerVR SGX *</td>
</tr>
<tr>
<td>Video in Unit</td>
<td>2ch</td>
<td>3ch</td>
</tr>
<tr>
<td>Display Unit</td>
<td>1ch</td>
<td>2ch</td>
</tr>
<tr>
<td>Temperature range</td>
<td>-40 ~ 85°C</td>
<td>-40 ~ 85°C</td>
</tr>
<tr>
<td>External memory</td>
<td>DDR2 (DDR600)</td>
<td>DDR3 (DDR1066) 2ch</td>
</tr>
</tbody>
</table>
SH-Navi3 Characteristics

- Dual high-performance SH-4A CPU cores for superior processing performance of 1,920 MIPS with Low Power Consumption
  -- Multi core supporting both AMP and SMP

- On-chip 2-D and 3-D graphics functions achieving high-speed and varied rendering functions
  -- PowerVR SGX and renesas 2D/3D graphic processor

- Recognition processing IP (IMP-X) and Distortion Correction module (IMR)

- DDR3-SDRAM memory interface, serial ATA interface, and PCI Express interface for ultra-high-speed data transfer
  -- realize high-quality display through ultra-high-speed transfer (up to 4.27 GB/s) of large volume multimedia data
Automotive Safety System based on Image Recognition

Current demands

Object recognition for avoidance of traffic accident
- vehicle, pedestrian, traffic sign, lane, etc…

Making more understandable images
- parking assist etc…

vehicle
pedestrian
changing view point

Caution! The car is approaching.
Caution! A pedestrian is detected.
1-Chip Solution’s Problem with Image Recognition

- Application of image recognition in real-time consumes a lot of CPU power and it could disturb the other applications.

Solution: Embedded Image recognition accelerator (IMP-X)
Concept of Image Recognition Accelerator (IMP-X)

- IMP-X accelerates frequency-used functions
- CPU calculates the others or complicated functions
- IMP-X & CPU access same image memory region with same distance

Process time distribution of image recognition application

Relationship of between IMP-X, CPU, bus, and image memory region

IMP-X acceleration

Only CPU

CPU & IMP-X

Simple functions

Complicated functions (CPU processing)

Image dataset
Process Flow of Image Recognition

CPU
533MHz x 2

Video Input x3

DDR3 memory

Display Unit x2

Peripherals

SuperHyway bus (266MHz/64bit)

SuperHyway bus (133MHz/128bit)

IMP-X(266MHz)

128bit

Local bus

Main processing unit

Line memory controller

local parallel & pipeline processors

Post processing unit

Histogram processor

Pre processing unit

Line memory

90fps@VGA

Feed back loop
IMP-X Characteristics

For High-speed processing
- Various image functions - up to 53.3 GOPS
- Distortion correct

For Integration into SoC

For Versatile processing

Local parallel processing
Pipeline processing
Function specific accelerator (IMR)
Compact Architecture
PIPE (Programmable Image Processing Extensions)
What functions does IMP-X accelerate?

- Image Affine Transformation
- Pixel Transformation
- Inter Pixel Arithmetic Calculations
- Inter Pixel Logical Calculations
- Binary Image Shape Transformation
- Convolution → 0.58ms@VGA

- Minimum/Maximum Filter
- Rank Filter
- Labeling
- Gray Scale Image Characteristics
- Binary Image Characteristic Extraction → 1.15ms@VGA

- Memory Access
- Binary Pipeline Filter
- Pipeline Control
- YUV Color Processing
- Binary Matching Filter
- Optical flow
- Template Matching (SAD, Normalized Correlation etc)
- Matrix operation
- FFT
- etc...

Normalized Correlation is operated at 53.3 GOPS (Max performance of IMP-X)
For High-speed Processing : Template Matching

- Calculate similarity between template pattern \( f \) and part of image \( g \)

  Normalized Correlation Coefficient
  \[
  \frac{\sum \sum (f(x, y) - \bar{f})(g(x, y) - \bar{g})}{\sqrt{\sum \sum (f(x, y) - \bar{f})^2} \times \sqrt{\sum \sum (g(x, y) - \bar{g})^2}}
  \]

- Total Processing: \((1+2+2+3) \) Operations \( \times 25 \) GSEUs \( \times 266 \) MHz = 53.3 GOPS
For High-speed Processing : Distortion Correction

- Generating image pattern for distortion correction, rotation, zoom out/in
  - Control by flexible triangle mesh with vertex data set
- Vertex Data Optimization
  - Triangle Strip of N vertex, Automatic generation of inner vertex data in Rectangle mesh
- YUV image format (combination/independent), Gray-scale format (8bpp)
- Hi-Speed drawing engine at 90fps with VGA

Raw image from camera

Intensity(Y)plane

Rotation, Zoom-Out

Distortion Correction

Color(UV)plane

Result image

Intensity(Y)plane

Color(UV)plane

Image Recognition

Color Graphic

Function specific accelerator (IMR)
For Integration into SoC and versatile processing

- **Programmable processing** at each line with micro-code control
- **Reducing data traffic** between IMP-X and memory by store and reuse of processed data in IMP-X

Comparison of 3 image-functions behavior between IMP and IMP-X

---

**PIPE (Programmable Image Processing Extensions) architecture**

* DDR3 1066: up to 8.5GB/s
Process Flow of Image Recognition

Video Input x3

DDR3 memory

Display Unit x2

Peripherals

CPU 533MHz x 2

SuperHyway bus (266MHz/64bit)

SuperHyway bus (133MHz/128bit)

IMP-X(266MHz)

Local bus

128bit

0x0

Pre processing unit

Line memory

Main processing unit

line memory controller

Local parallel & pipeline processors

Post processing unit

Histogram processor

IMR 90fps@VGA

Feed back loop
Bus traffic reduction for Corner detector

Harris corner detector requires 14 functions

\[
H = \begin{bmatrix}
\sum I_x^2 & \sum I_x I_y \\
\sum I_x I_y & \sum I_y^2 \\
\end{bmatrix} = \begin{bmatrix}
a & b \\
b & c \\
\end{bmatrix}
\]

where

\[
I_x = \frac{\partial I}{\partial x}, \quad I_y = \frac{\partial I}{\partial y}
\]

\[
det(H) = ac - b^2
\]

\[
Trace(H) = a + c
\]

\[
R = det(H) - kTrace(H)^2
\]

![Diagram of corner points](image)

<table>
<thead>
<tr>
<th>proc time [ms]</th>
<th>bus efficiency [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>only image processing</td>
<td></td>
</tr>
<tr>
<td>9.25 ms</td>
<td>11.19 ms</td>
</tr>
<tr>
<td>11.23 ms</td>
<td></td>
</tr>
<tr>
<td>with many processing CPU, Display, Video in, IMR, etc.</td>
<td></td>
</tr>
<tr>
<td>31.04 ms</td>
<td></td>
</tr>
</tbody>
</table>

**Corner**

**The 15th ASPDAC**

\[
bus efficiency = \frac{\text{load & store request for DRAM}}{\text{all IMP – X cycles}}
\]
Practical Application: Pedestrian Detection with Neural Network

- Pedestrian Detection is one of the important applications for safety systems.
- Three-layered neural network is used for recognizing pedestrian patterns.

With CPU...

- 1600 Neural Network processing time: **204.0 ms**
- Total Pedestrian detection application processing time: **233 ms**
The neural network consists of two matrix product operation stages (1,3) and several mathematical transformation stages (2, 4).

With IMP-X ...

- **1600 Neural Network processing time**: 204.0ms → 8.9 ms
- **Total Pedestrian detection application processing time**: 233 ms → 29.4 ms
Summary

SH-Navi3 embeds:
- High performance dual RISC processors (1920 MIPS)
- 2D/3D graphic accelerators
- Image Recognition Engine
  - High-speed processing (up to 53.3GOPS):
    parallel processing + pipeline architecture + function specific accelerator
  - Bus traffic reduction & Line programmability:
    PIPE architecture
- High speed bus technology

Achieves a 1-Chip solution for Next-Generation Car Navigation Systems