The 15th ASPDAC
Session 5D : Designer's Forum : State-of-the-art SoCs
5D-4

SoC for Car Navigation Systems with a 53.3 GOPS Image Recognition Engine

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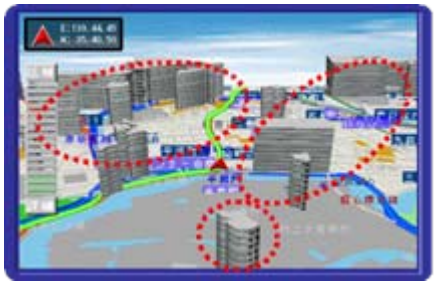
Contents

Advanced Car Navigation Systems

Navigation



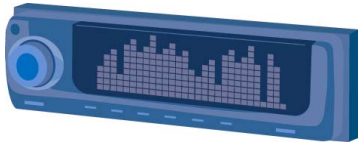
Driver friendly user interface and graphics

Safety

Object Recognition
Passive/Active Safety

Amusement

Digital TV display



Audio playback

Multi Applications assisting and entertaining our driving

Demanded Technology for Advanced Car navigation Systems

Navigation

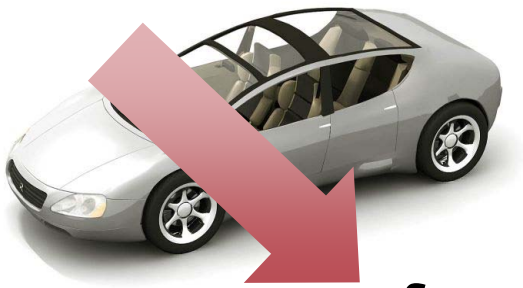
High Performance and various Graphic processing technology

GPS technology

Safety

High performance embedded image recognition technology

Connection with vehicle-control technology



Amusement

Multimedia interface technology

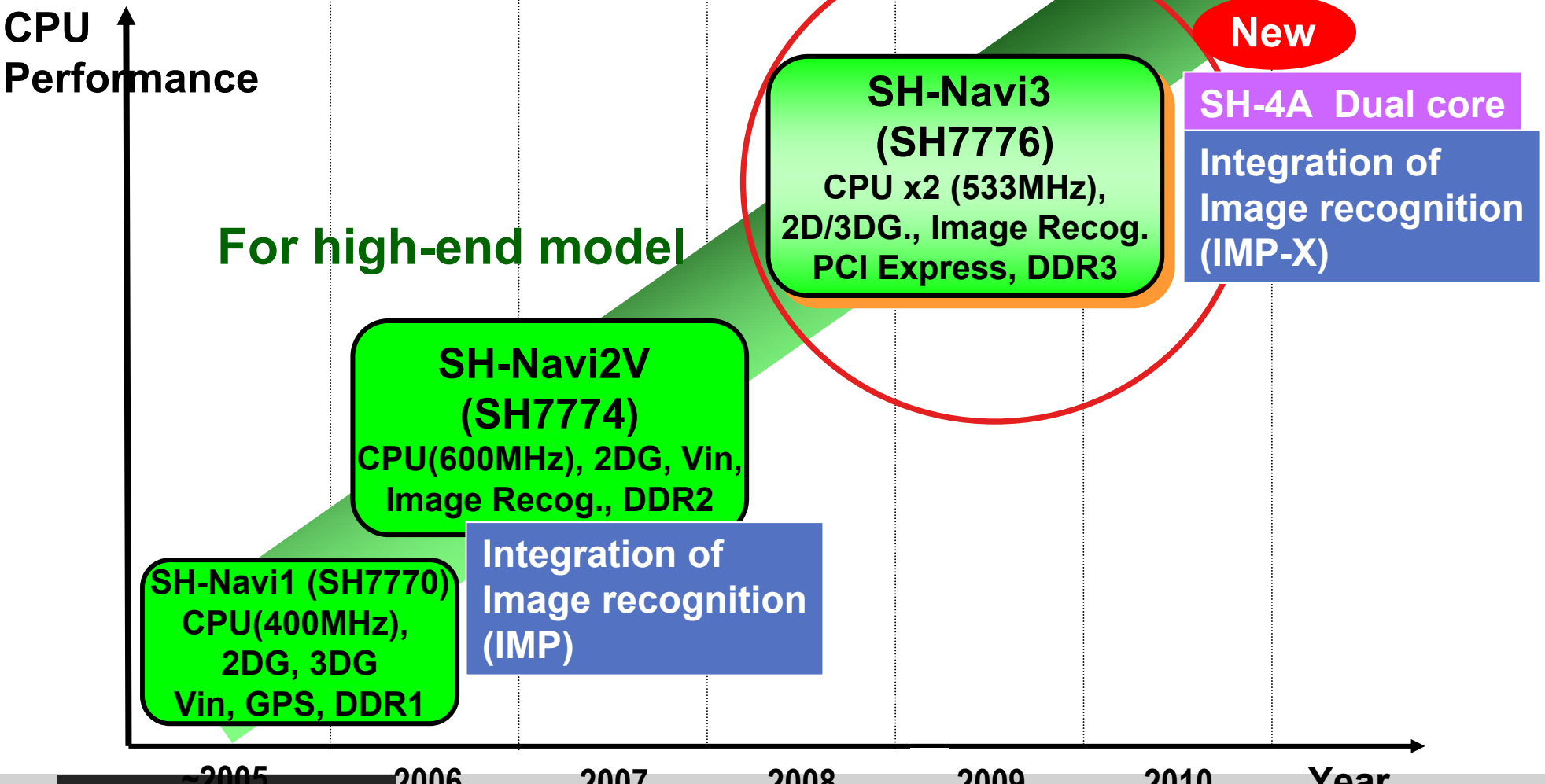
Audio / video processing technology

fundamental technology

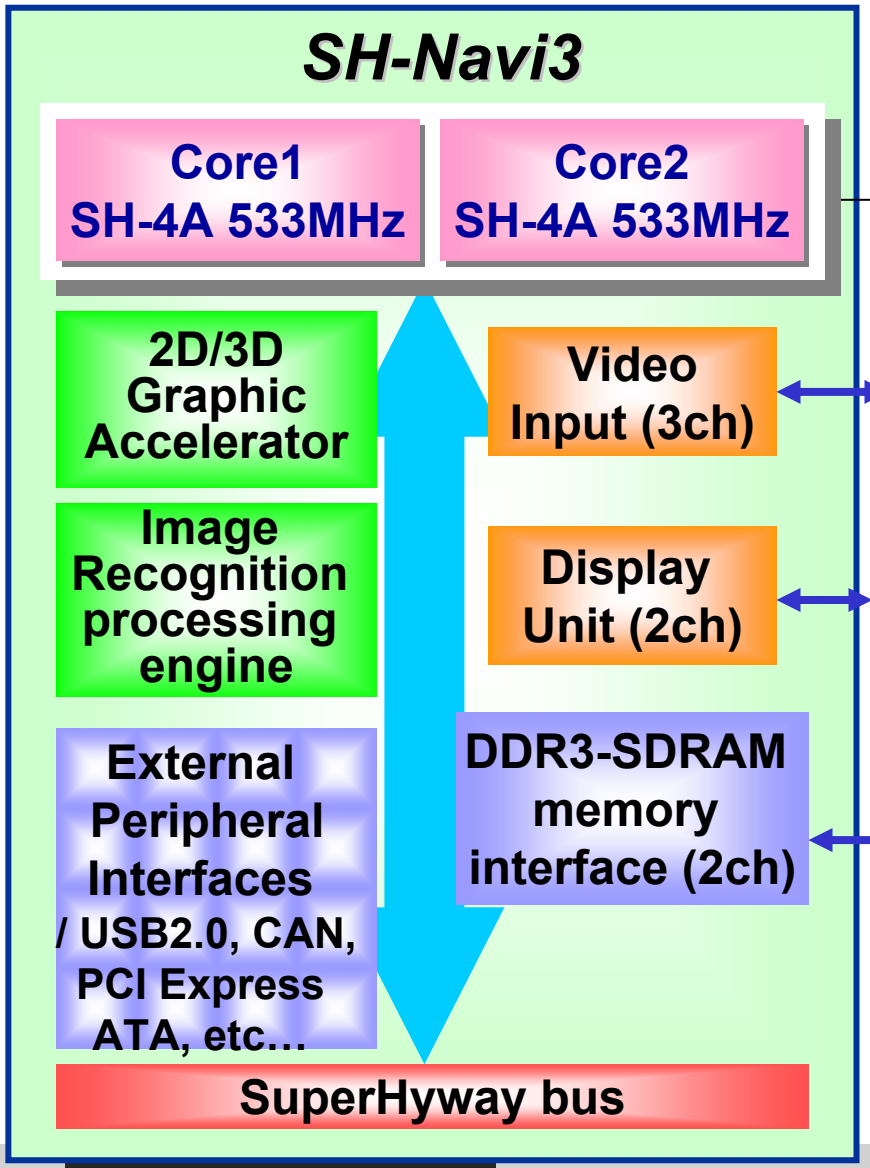
- High-performance MPU
- High speed bus and data I/O technology
- etc…

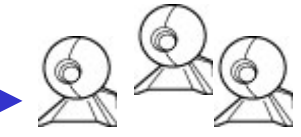
Products Lineup for Embedded Car Navigation Systems

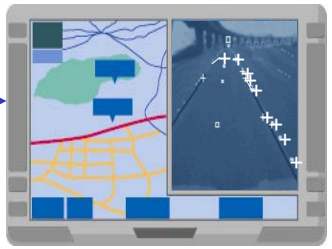
Delivering advanced technology for 1-Chip Car Navigation Systems



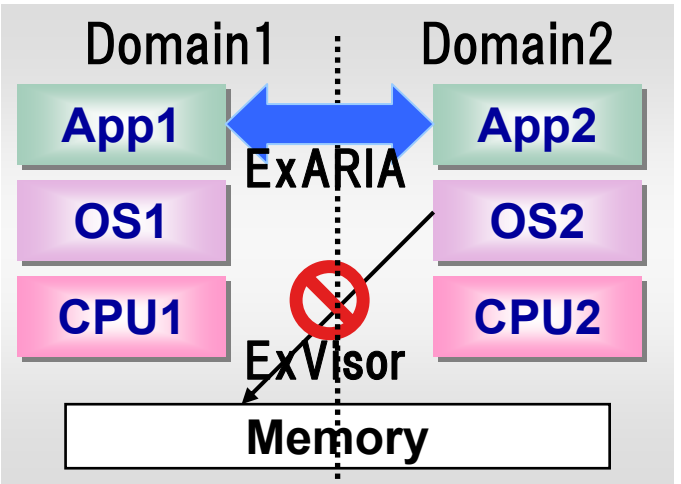
Next Generation 1-Chip Solution : SH-Navi3







- For multi-core system
- EXREAL Platform™
  1. ExVisor : inter-OS prevention technology (Domain Separation)
  2. ExARIA : inter-OS communication interface (Domain interoperation)



Specification of SH-Navi3

	SH-Navi2V (SH7774)	***SH-Navi3 (SH7776)***
Technology	90nm	65nm
CPU	SH-4A 600MHz (1080MIPS) FPU : 4.2 GFLOPS	SH-4A x 2 533MHz (960MIPS) x2 FPU : 7.46 GFLOPS
Cache	I : 32KB, D : 32KB	I:32KB,D : 32KB,L2 : 128KB
Image recognition engine	38.4 GOPS engine	53.3 GOPS engine Distortion Correction module
Graphics IP	2D accelerator	2D/3D accelerator PowerVR SGX *
Video in Unit	2ch	3ch
Display Unit	1ch	2ch
Temperature range	-40 ~ 85° C	-40 ~ 85° C
External memory	DDR2 (DDR600)	DDR3 (DDR1066) 2ch

* Imagination Technology

SH-Navi3 Characteristics

- **Dual high-performance SH-4A CPU cores for superior processing performance of 1,920 MIPS with Low Power Consumption**
  - **-- Multi core supporting both AMP and SMP**

- **On-chip 2-D and 3-D graphics functions achieving high-speed and varied rendering functions**
  - **-- PowerVR SGX and renesas 2D/3D graphic processor**

- **Recognition processing IP (IMP-X) and Distortion Correction module (IMR)**

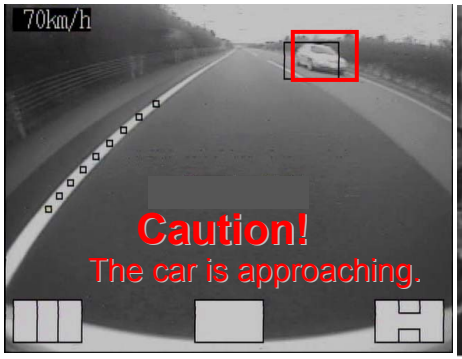
- **DDR3-SDRAM memory interface, serial ATA interface, and PCI Express interface for ultra-high-speed data transfer**
  - **-- realize high-quality display through ultra-high-speed transfer (up to 4.27 GB/s) of large volume multimedia data**

Automotive Safety System based on Image Recognition

Current demands

Object recognition for avoidance of traffic accident

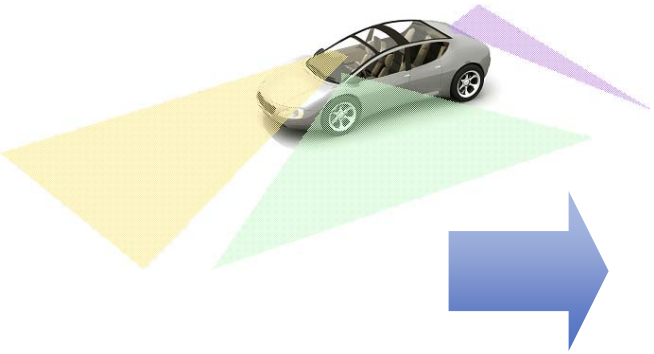
- vehicle, pedestrian, traffic sign, lane, etc…

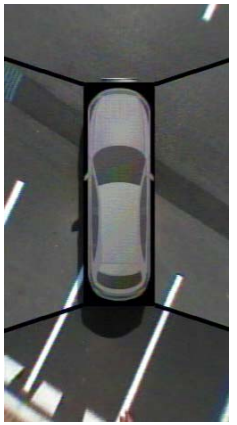


vehicle pedestrian

Making more understandable images

- parking assist etc…

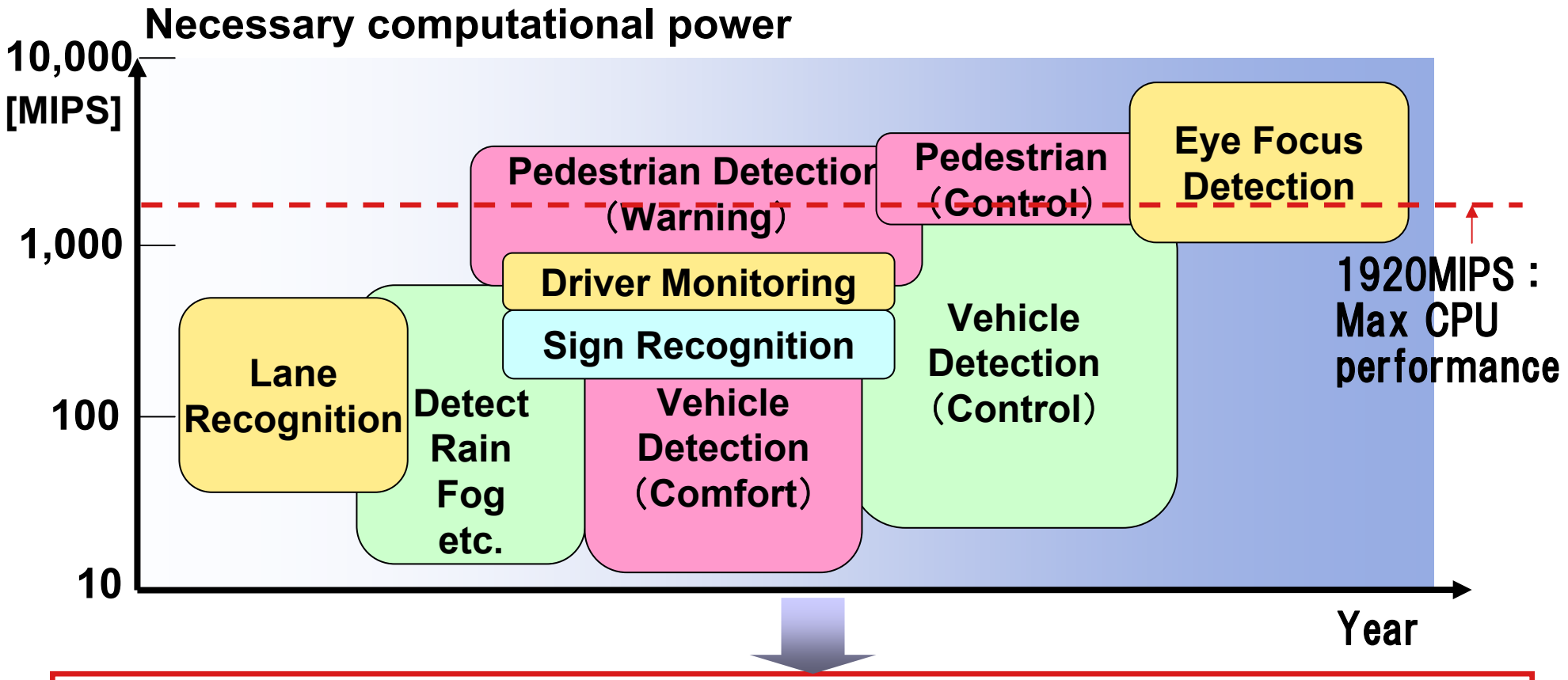




changing view point

1-Chip Solution's Problem with Image Recognition

- **Application of image recognition in real-time consumes a lot of CPU power and it could disturb the other applications**

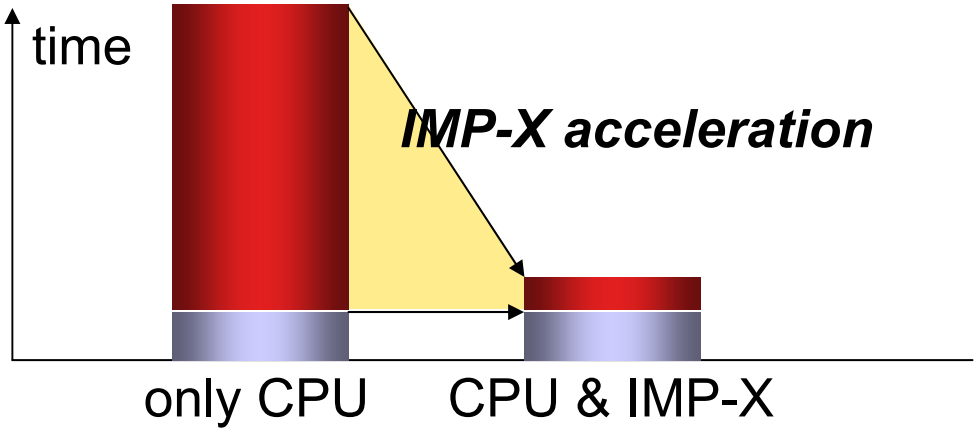


Solution : Embedded Image recognition accelerator (IMP-X)

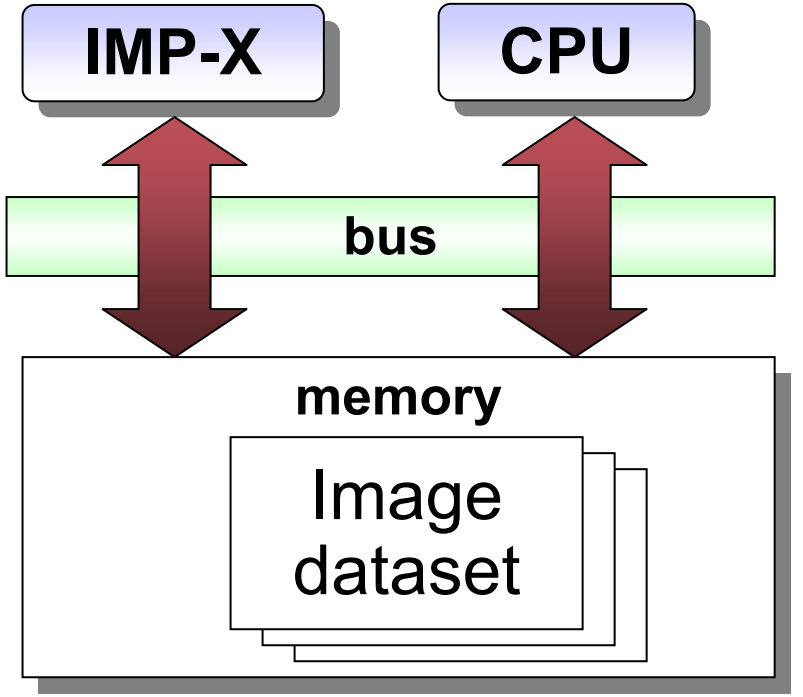
Concept of Image Recognition Accelerator (IMP-X)

- **IMP-X accelerates frequency-used functions**
- **CPU calculates the others or complicated functions**
- **IMP-X & CPU access same image memory region with same distance**

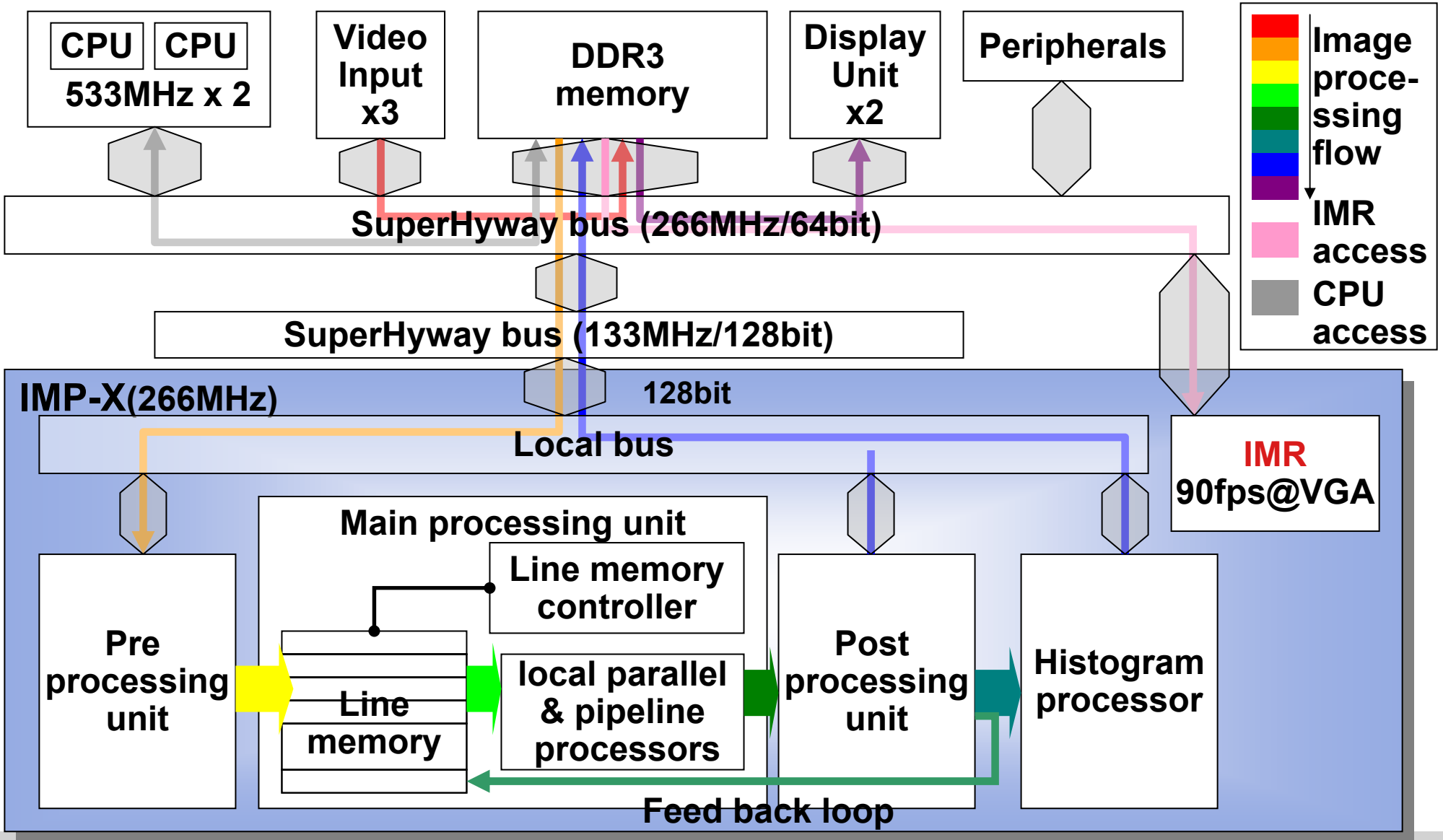
Process time distribution of image recognition application



Relationship of between IMP-X, CPU, bus, and image memory region



Process Flow of Image Recognition



IMP-X Characteristics

For High-speed processing

- Various image functions
  - up to 53.3 GOPS

→ Local parallel processing
→ Pipeline processing

- Distortion correct

→ Function specific accelerator (IMR)

For Integration into SoC

→ Compact Architecture
→ PIPE (Programmable Image Processing Extensions)

For Versatile processing

For High-speed Processing : Various Image Functions

What functions does IMP-X accelerate ?

- Image Affine Transformation
- Pixel Transformation
- Inter Pixel Arithmetic Calculations
- Inter Pixel Logical Calculations
- Binary Image Shape Transformation
- Convolution → **0.58ms@VGA**

- Minimum/Maximum Filter
- Rank Filter
- Labeling
- Gray Scale Image Characteristics
- Binary Image Characteristic Extraction → **1.15ms@VGA**

- Memory Access
- Binary Pipeline Filter
- Pipeline Control
- YUV Color Processing
- Binary Matching Filter
- Optical flow
- Template Matching (SAD, Normalized Correlation etc)
- Matrix operation
- FFT
- etc…

Normalized Correlation is operated at 53.3 GOPS (Max performance of IMP-X)

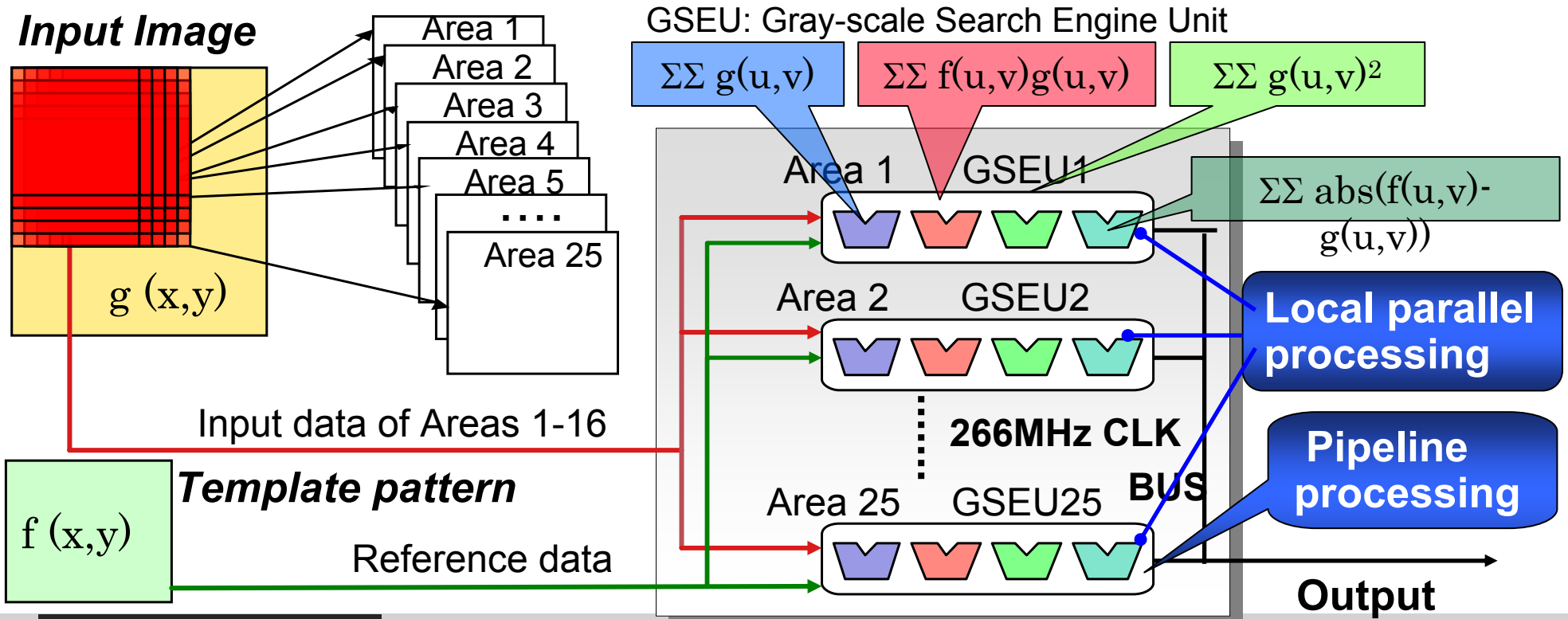
For High-speed Processing : Template Matching

- **Calculate similarity between template pattern(f) and part of image(g)**

Normalized Correlation Coefficient

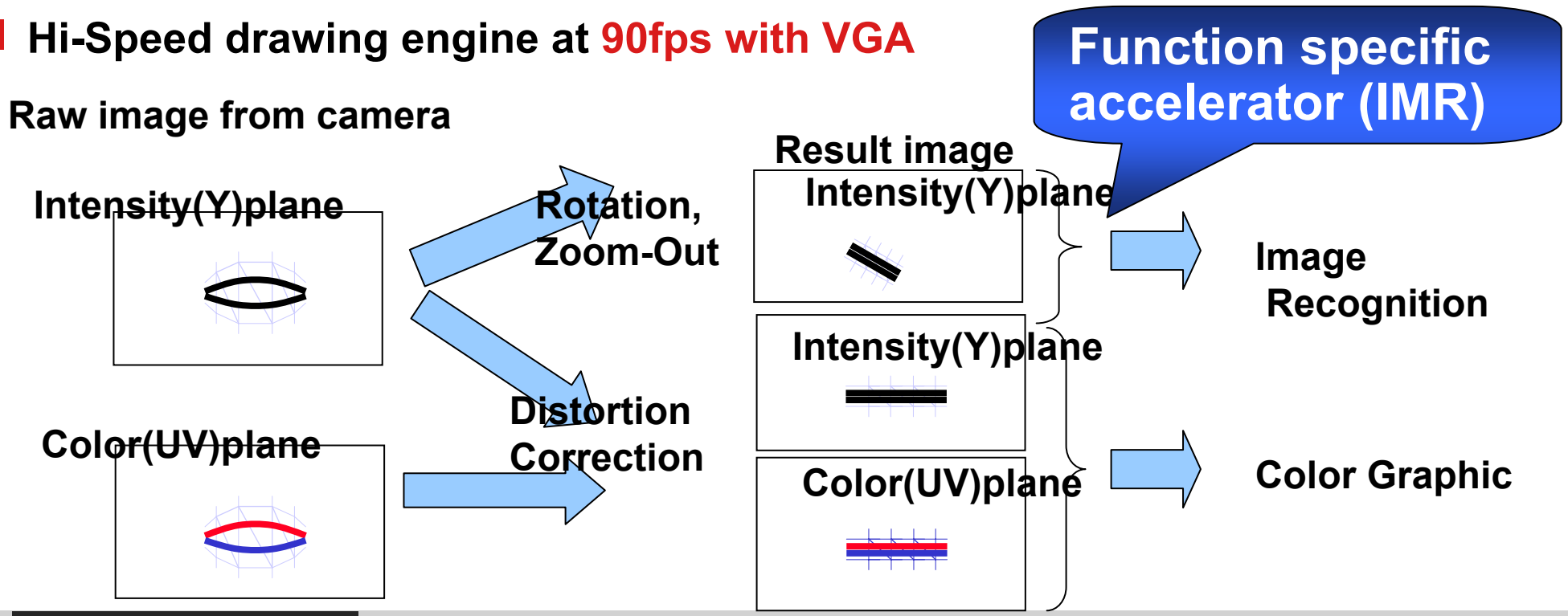
$$= \frac{\sum\sum \left(f(x,y)-\bar{f}\right)\left(g(x,y)-\bar{g}\right)}{\sqrt{\sum\sum \left(f(x,y)-\bar{f}\right)^2} \times \sqrt{\sum\sum \left(g(x,y)-\bar{g}\right)^2}}$$

- **Total Processing: (1+2+2+3) Operations * 25 GSEUs * 266 MHz = 53.3GOPS**



For High-speed Processing : Distortion Correction

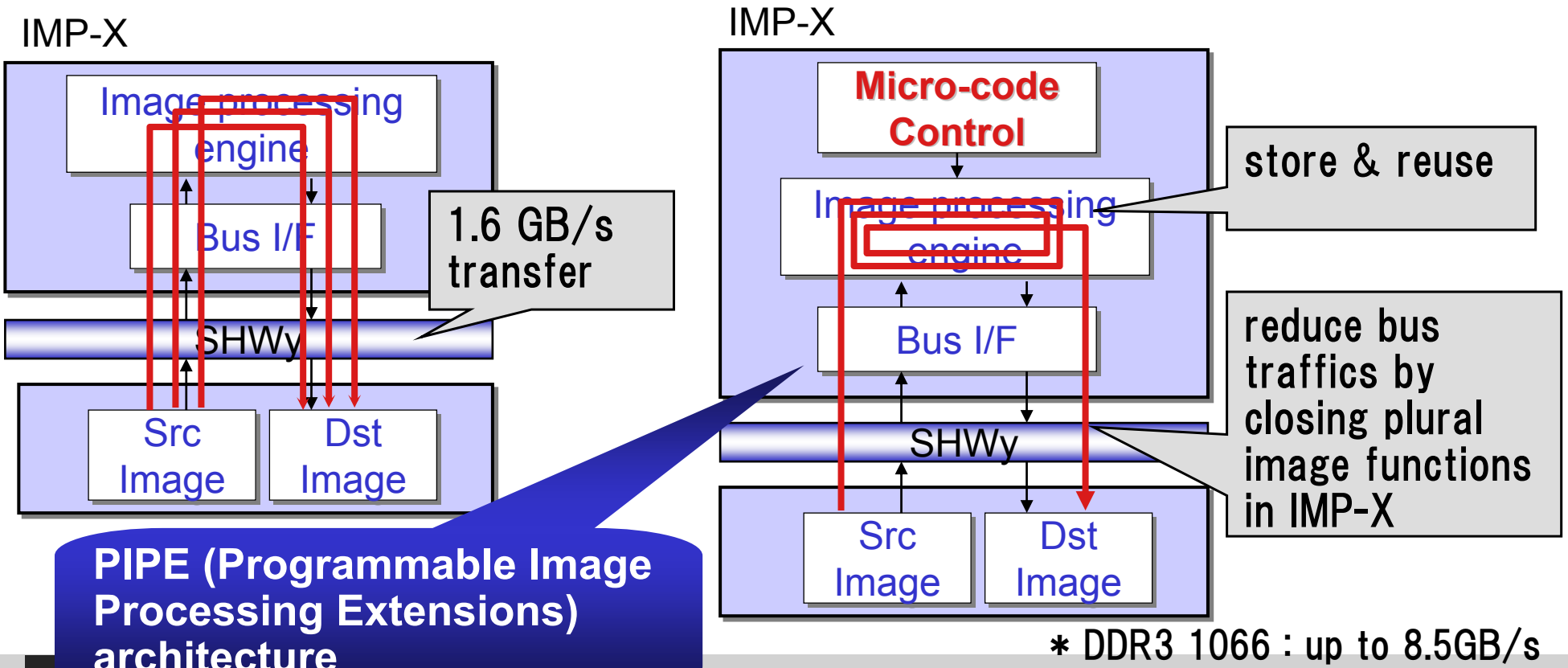
- **Generating image pattern for distortion correction, rotation, zoom out/in**
  - **Control by flexible triangle mesh with vertex data set**
- **Vertex Data Optimization**
  - **Triangle Strip of N vertex, Automatic generation of inner vertex data in Rectangle mesh**
- **YUV image format (combination/independent), Gray-scale format (8bpp)**
- **Hi-Speed drawing engine at 90fps with VGA**



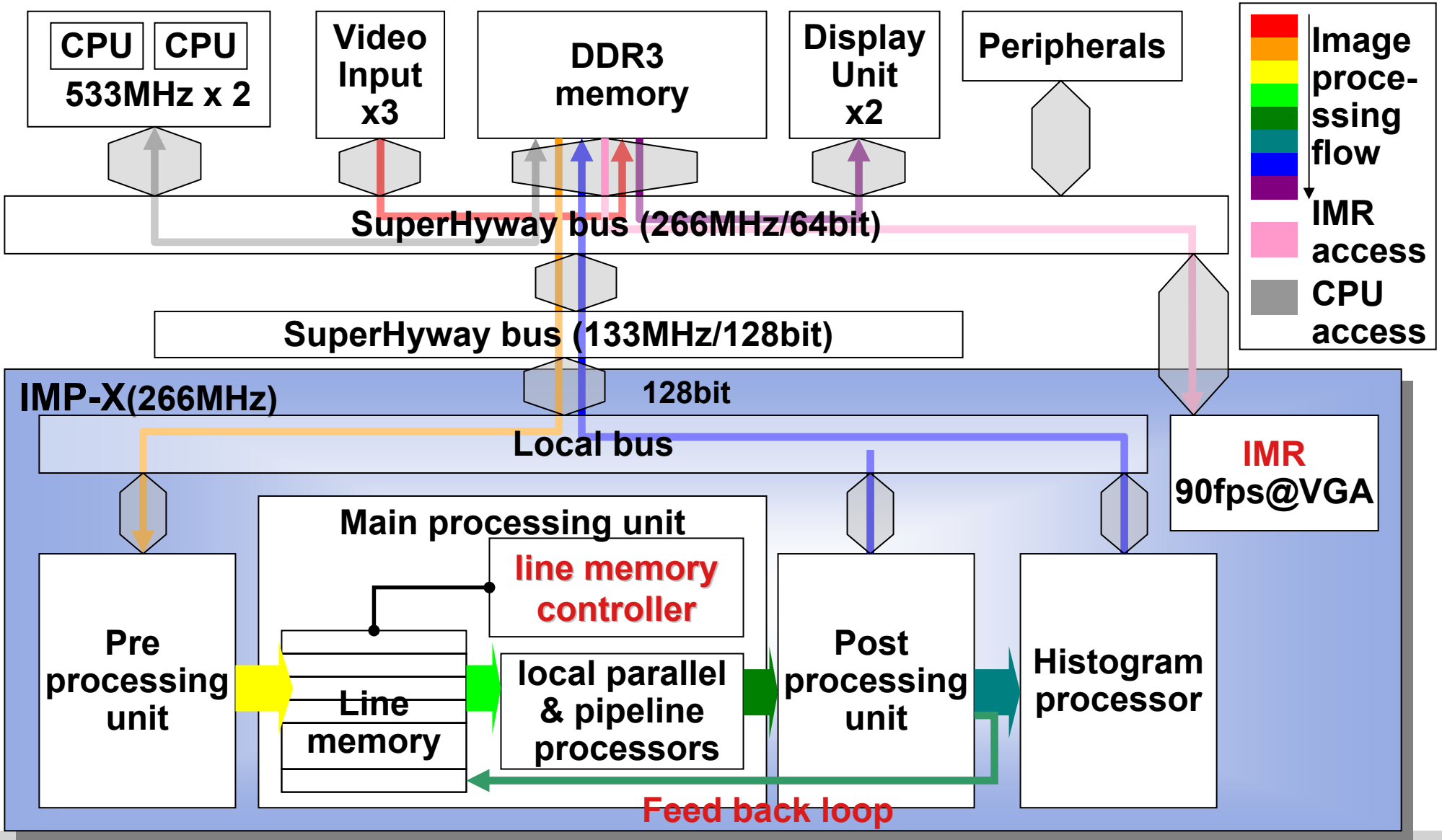
For Integration into SoC and versatile processing

- **Programmable processing at each line with micro-code control**
- **Reducing data traffic between IMP-X and memory by store and reuse of processed data in IMP-X**

Comparison of 3 image-functions behavior between IMP and IMP-X



Process Flow of Image Recognition



Bus traffic reduction for Corner detector

Harris corner detector requires 14 functions

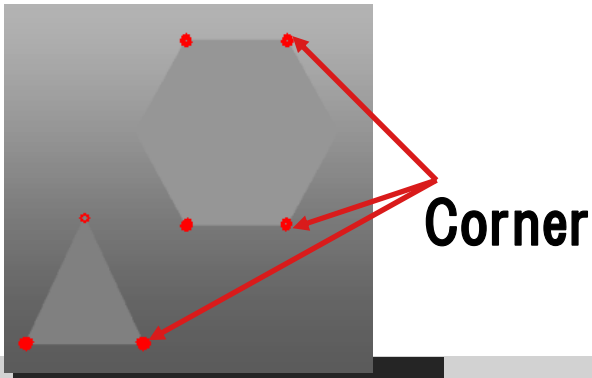
$$H = \begin{bmatrix} \sum I_x^2 & \sum I_x I_y \\ \sum I_x I_y & \sum I_y^2 \end{bmatrix} = \begin{bmatrix} a & b \\ b & c \end{bmatrix}$$

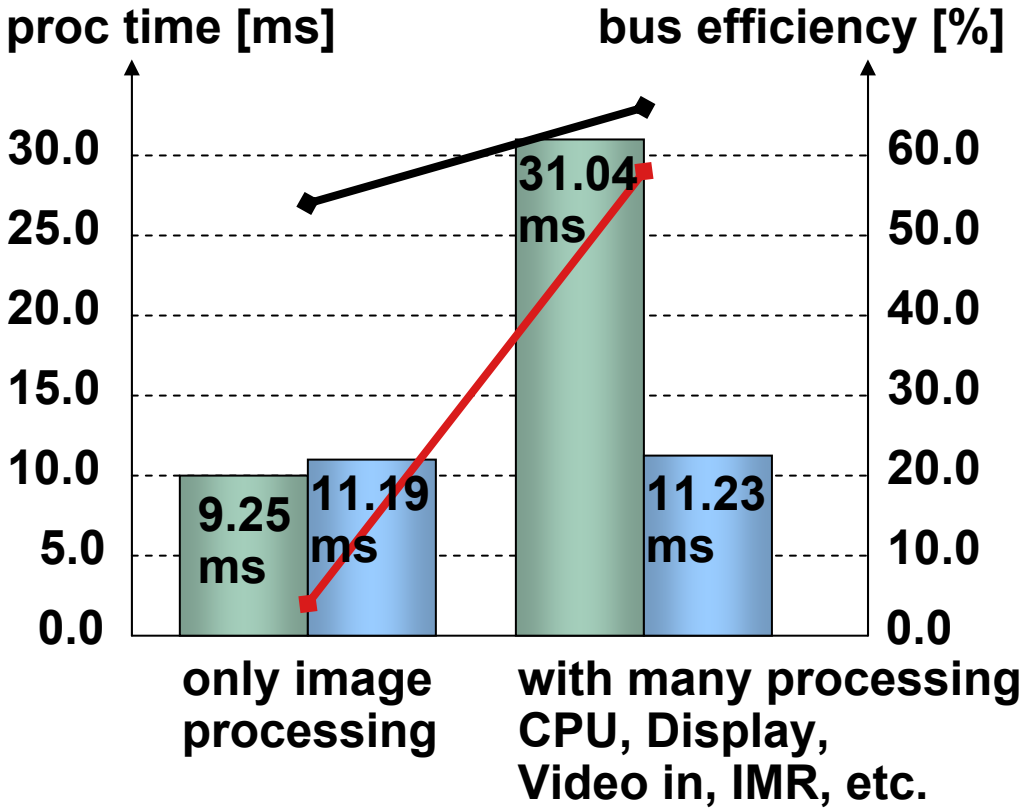
where $I_x = \frac{\partial I}{\partial x}, \quad I_y = \frac{\partial I}{\partial y}$

$$\det(H) = ac - b^2$$

$$Trace(H) = a + c$$

$$R = \det(H) - kTrace(H)^2$$





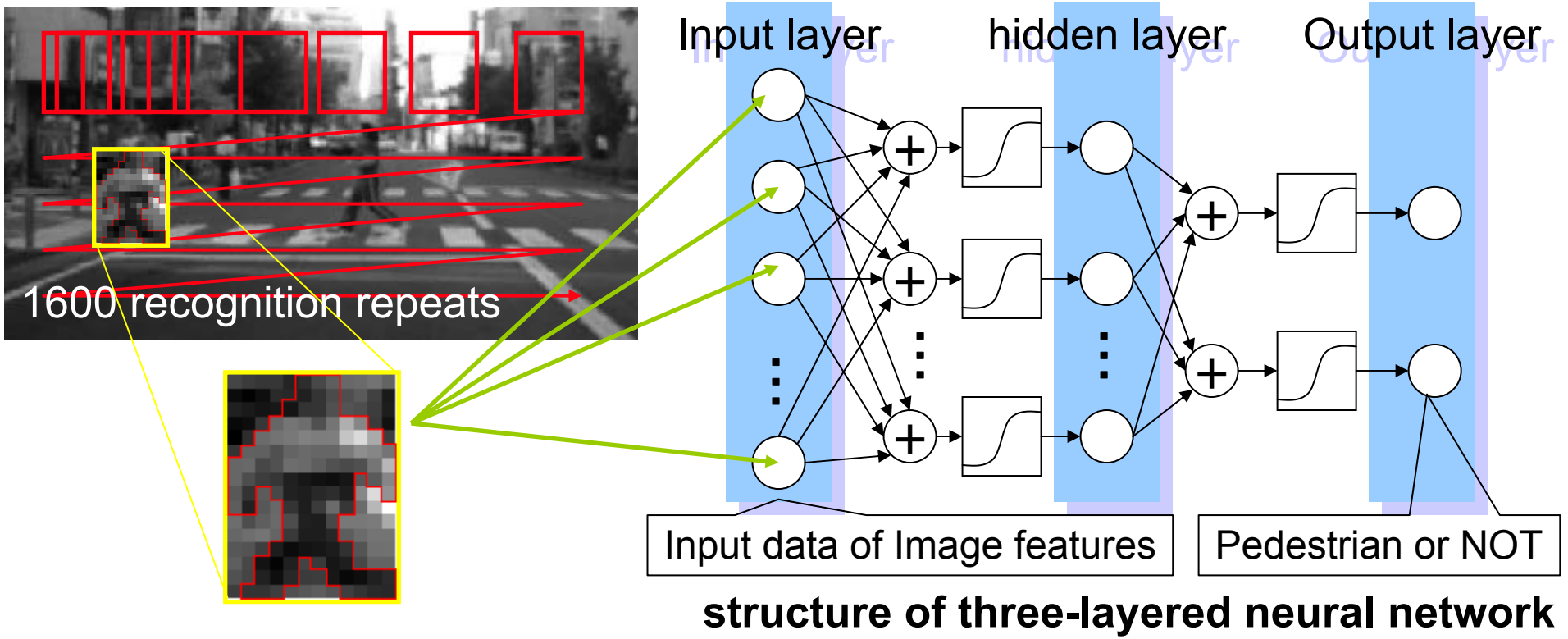
without PIPE processing

PIPE processing

$$\text{bus efficiency} = \frac{\text{load \& store request for DRAM}}{\text{all IMP} - \text{X cycles}}$$

Practical Application : Pedestrian Detection with Neural Network

- **Pedestrian Detection is one of the important application for safety system.**
- **Three-layered neural network is used for recognizing pedestrian pattern..**



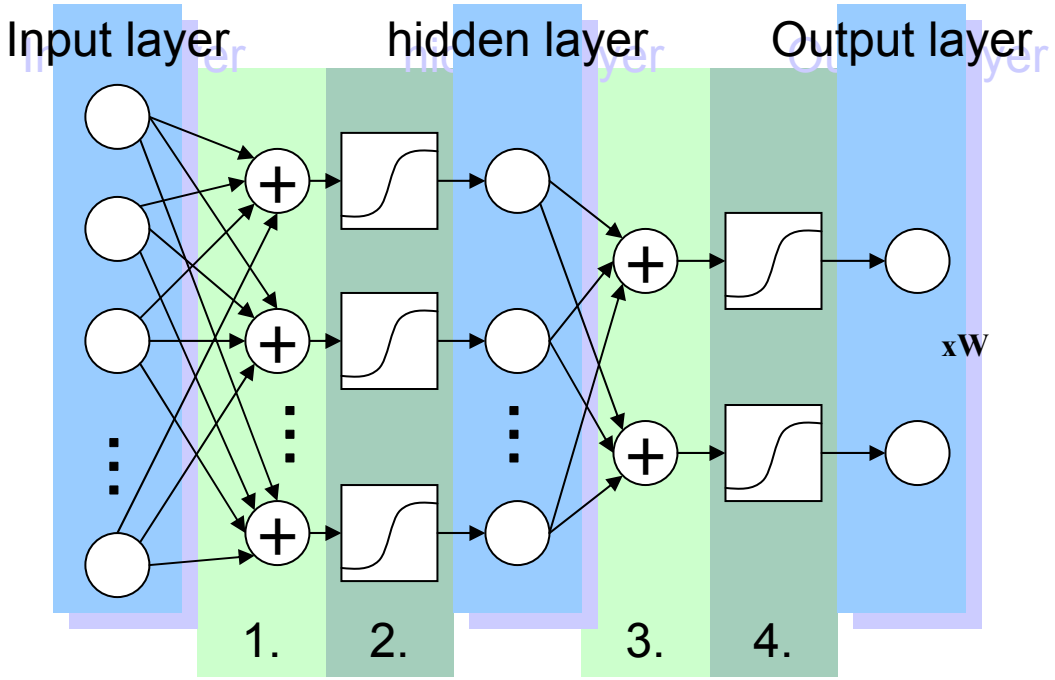
structure of three-layered neural network

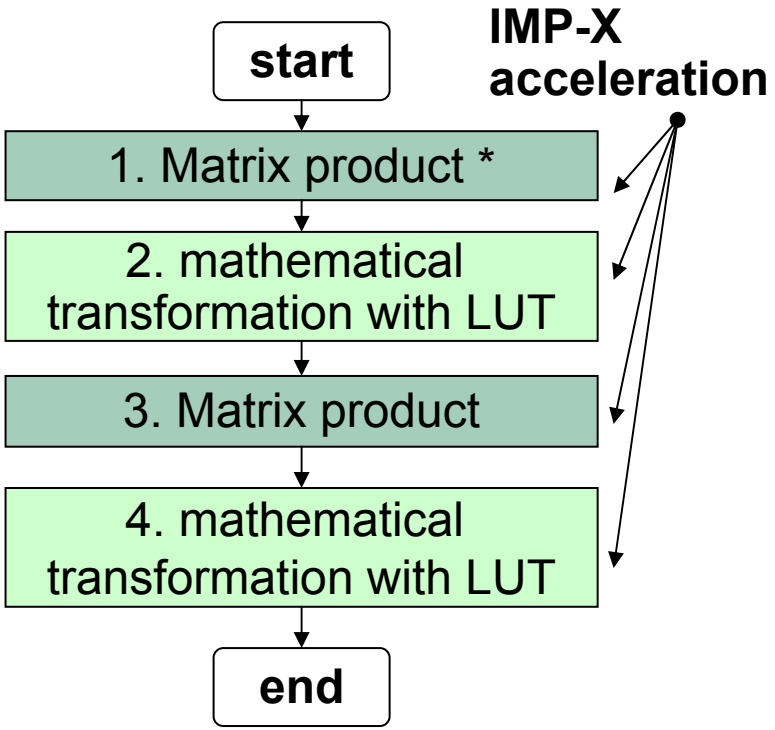
With CPU ...

- **1600 Neural Network processing time : 204.0ms**
- **Total Pedestrian detection application processing time : 233 ms**

Practical Application : Acceleration of Neural Network

- **The neural network consists of two matrix product operation stages(1,3) and several mathematical transformation stages (2, 4).**





* Matrix product is operated by 25 parallel inner product operation unit

With IMP-X ...

- **1600 Neural Network processing time : 204.0ms → 8.9 ms**
- **Total Pedestrian detection application processing time : 233 ms → 29.4 ms**

Summary

SH-Navi3 embeds

- High performance dual RISC processors (1920 MIPS)
- 2D/3D graphic accelerators
- Image Recognition Engine

  -- High-speed processing (up to 53.3GOPS) :
  parallel processing + pipeline architecture + function specific accelerator

  -- Bus traffic reduction & Line programmability :
  PIPE architecture
- High speed bus technology

Achieves a 1-Chip solution for Next-Generation Car Navigation Systems

RENESAS

HITACHI

Inspire the Next

Renesas Technology