Buffered Clock Tree Sizing for Skew Minimization under Power and Thermal Budgets

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Review

- **Sequential-Linear-Programming based clock sizing**
  - Low-power and skew minimization [Wang, etc. IEEE Trans. ‘05]
  - Process-variation-aware clock skew minimization under power budget [Guthaus, etc. DAC’06]

- **Thermal-aware clock network design**
  - Balanced thermal-aware skew under given thermal profiles [Cho, etc. ICCAD’05]
  - Thermal-aware bottom-up merging based on thermal sensitivity [Yu, etc. ISPD’07]
  - Thermal-aware 3D clock routing algorithm design [Minz, etc. ASPDAC’08]
Challenges

• Wire/buffer sizing impacts on delay / thermal / power
  – Impact of sizing on thermal variations can not be ignored

• Thermal profiles are changed during optimization

• Consider power and thermal budget simultaneously
Contributions

• Thermal-Aware Sequential-Linear-Programming (TA-SLP)
  – Thermal-aware clock skew minimization under power and thermal budgets

• Single and multiple thermal profiles

• Thermal-aware skew or skew range minimization
  – Minimize skew value under single steady-state thermal profile
  – Minimize skew range under multiple thermal profiles

• Loosely-Thermal-Aware-Sequential-Linear-Programming (LTA-SLP)
  – A speedup scheme to update delay, thermal and power sensitivity
Problem formulation: Thermal-aware clock sizing

- **Input:**
  - Non-sized buffered clock tree
  - Thermal profile (single or multiple)
  - Power and thermal budgets

- **Output:**
  - A sized-clock tree: wire widths and buffer sizes are determined

- **Object:**
  - Minimize thermal-aware clock skew (skew value or skew range)

- **Constraint:**
  - Power budget
  - Temperature budget
Overview: TA-SLP sizing flow

1. Initial Clock Tree
   - Plimit, Tlimit
2. Thermal analysis
3. Delay / skew analysis
4. Delay / Thermal / Power sensitivity analysis
5. Solve SLP
   - Wire/buffer size
6. Converged?
   - Yes: Sized clock tree
   - No: Repeat steps 2-5
Thermal analysis

• Power consumption
  – Underlying power: Substrate devices
  – Clock power: Clock wires and buffers

• Compact substrate thermal model*
  \[ t = R \times p \]
  \[ R_{ij} = \frac{\partial T_i}{\partial p_j} \]
  – n x n thermal tiles
  – R: thermal resistance matrix
  – t, p: temperature and power vectors

Thermal-aware delay models

- Thermal impact on wire model
  - Temperature-dependent resistance
  \[ R(T) = \frac{\rho_0 \cdot l}{w \cdot t} \times (1 + \beta_0 \cdot T) \]

- Thermal impact on buffer model
  - Driving resistance
    - linearly depends on temperature within a small region.
  - Intrinsic delay with buffer size \( S \) and temperature \( T \)
    - 10x to 70x buffer size, at 60 to 110 °C, \( \alpha = 0.005, \tau = 0.00013 \), mean absolute error = 0.04ps.

\[
\begin{align*}
t_d(T, S) &= t_{d0}(S) \times (1 + \beta_{in}(S) \cdot (T - T_0)), \\
\beta_{in}(S) &= \alpha - S \cdot \tau,
\end{align*}
\]
Sensitivity computation

For a wire/buffer $j$, with $w_j^0$ changes to $w_j^0 + \epsilon_j$:

$$\hat{w}_j^0 = [w_1^0, w_2^0, \ldots, w_j^0 + \epsilon_j, \ldots, w_m^0]^T$$

- **G**: Delay sensitivity matrix
  - Delay variation caused by sizing

$$G_{ij} = \left. \frac{\partial d_i}{\partial w_j} \right|_{w_j = w_j^0} \approx \frac{d_i(t_j^0, \hat{w}_j^0) - d_i(t^0, w^0)}{\epsilon_j}$$

$$d_i^1 = d_i^0 + \sum_{j} G_{ij} \cdot \delta_j$$

Where $i \in \text{sinks}$, $j \in \text{wires/buffers}$

$$\hat{t}_j^0 = t(\hat{w}_j^0)$$
Sensitivity computation (cont.)

• $\Gamma$: Thermal sensitivity matrix
  - Average thermal variation of thermal tiles caused by sizing
  \[
  \Gamma_{ij} = \left. \frac{\partial t_i}{\partial w_j} \right|_{w_j = w_j^0} \approx \frac{t_i(\hat{w}_j^0) - t_i(w^0)}{\epsilon_j}
  \]
  \[
  t_i^1 = t_i^0 + \sum_{j} \Gamma_{ij} \cdot \delta_j
  \]
  Where $i \in \text{tiles}$, $j \in \text{wires/buffers}$

• $\beta$: Power sensitivity vector
  - Total power variation caused by sizing
  \[
  \beta_j = \left. \frac{\partial p}{\partial w_j} \right|_{w_j = w_j^0} \approx \frac{p(\hat{w}_j^0) - p(w^0)}{\epsilon_j}
  \]
  Where $j \in \text{wires/buffers}$
Linear sub-problem in TA-SLP

- Given the current wire/buffer size $w^0$, decide the size change $\delta$

Minimize

$$d_{\text{max}} - d_{\text{min}}$$

Subject to

$$d_1^1 = d_0^0 + G \cdot \delta$$

$$t_1^1 = t_0^0 + \Gamma \cdot \delta$$

$$p_1^1 = p_0^0 + \beta^T \cdot \delta$$

$$d_i^1 \geq d_{\text{min}}, \quad \forall i \in \text{sinks}$$

$$d_i^1 \leq d_{\text{max}}, \quad \forall i \in \text{sinks}$$

$$t_j^1 \leq T_{\text{limit}}, \quad \forall j \in \text{tiles}$$

$$p_1^1 \leq P_{\text{limit}}$$
Wire/buffer size update and control

New size after sizing:

\[ w_j^1 = w_j^0 + \delta_j \]

Restrict to:

\[ w_j^1 \in [\max(L_j, w_j^0 - \epsilon_j), \min(U_j, w_j^0 + \epsilon_j)] \]

\( \epsilon_j \): size perturbation for

In each linear sub-problem, the variable \( \delta_j \) for each wire/buffer is restricted within a small range, which provides the approximated linear range for the delay gradient.
Extension: multi-thermal profiles

• Single thermal profile -> multiple thermal profiles

• Minimization: thermal-aware skew -> thermal-aware skew range

• Our strategy:
  – Single average thermal profile:
    Average thermal profile among the multiple non-uniform profiles
  – Thermal-aware clock sizing under the single average thermal profile, and then evaluate it using multiple profiles
Loosely-Thermal-Aware-Sequential-Linear-Programming

• Motivation:
  – TA-SLP spends most of time solving LP sub-problems
  – Density of G matrix affects the runtime

• A speed-up scheme: LTA-SLP
  – Keep thermal profile the same in G matrix calculation
  – Update the thermal profile in each iteration

\[
G_{ij} = \frac{\partial d_i}{\partial w_j} \bigg|_{w_j = w^0_j} \approx \left( d_i(t^0_j, \hat{w}^0_j) - d_i(t^0, w^0) \right) / \epsilon_j \\
\downarrow
\\
d_i(t^0_j, \hat{w}^0_j)
\]
Detail experiment settings

• 65nm technology:
  – Wire:
    \[ R = 0.15 \, \Omega/\text{um} \, , \, C = 0.2 \, \text{fF/um} , \, \text{at 0}^\circ C, \, \text{minimum size} \]
    Size: 0.24um – 0.96um
  – Buffer:
    \[ R_d = 4.7k\Omega, \, C_L = 0.47\text{fF}, \, t_d=17.4\text{ps}, \, \text{at 0}^\circ C, \, \text{minimum size} \]
    Size: 12X – 64X
  – Frequency: 5GHz, \( V_{dd} \): 1.2V

• Thermal profile:
  – Multiple non-uniform: 10 power / thermal profiles

<table>
<thead>
<tr>
<th>Circuits</th>
<th># Sinks</th>
</tr>
</thead>
<tbody>
<tr>
<td>r1</td>
<td>267</td>
</tr>
<tr>
<td>r2</td>
<td>598</td>
</tr>
<tr>
<td>r3</td>
<td>862</td>
</tr>
<tr>
<td>r4</td>
<td>1903</td>
</tr>
<tr>
<td>r5</td>
<td>3101</td>
</tr>
</tbody>
</table>
Wire and buffer sizing greatly impacts power and temperature.

Three cases: min-size, mid-size and max-size

- Total power increases by 4 times
- Temperature increases by 10 °C to 13 °C.
Impact of initial sizing

- Three initial sizing: min-size, mid-size and max-size
- The single average thermal profile out of 10 thermal profiles
- TA-SLP reduces thermal-aware clock skew to near zero, regardless of the initial solution

<table>
<thead>
<tr>
<th>Ckt.</th>
<th>Min-size 0.24um 12X</th>
<th>Mid-size 0.60um 38X</th>
<th>Max-size 0.96um 64X</th>
</tr>
</thead>
<tbody>
<tr>
<td>r1</td>
<td>0.00</td>
<td>0.00</td>
<td>0.77</td>
</tr>
<tr>
<td>r2</td>
<td>0.00</td>
<td>0.00</td>
<td>0.44</td>
</tr>
<tr>
<td>r3</td>
<td>0.01</td>
<td>0.00</td>
<td>0.31</td>
</tr>
<tr>
<td>r4</td>
<td>0.01</td>
<td>0.01</td>
<td>0.42</td>
</tr>
<tr>
<td>r5</td>
<td>0.01</td>
<td>0.01</td>
<td>0.44</td>
</tr>
</tbody>
</table>

Skew value based on single average thermal profile (ps)
Impact of initial sizing (cont.)

- Clock skew range based on 10 thermal profiles
  - Mid-size case is slightly better than max-size case
  - Min-size case is the worst
- We choose mid-size as initial sizing
Comparison: NTA-SLP vs TA-SLP

- NTA-SLP: Non-thermal-aware SLP-based sizing
  - Minimize skew under power budget only, which resembles an existing work*

<table>
<thead>
<tr>
<th></th>
<th>P_{\text{total}} (W)</th>
<th>T_{\text{max}} (^\circ \text{C})</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Budget</td>
<td>NTA-SLP</td>
</tr>
<tr>
<td>r1</td>
<td>2.87</td>
<td>2.86</td>
</tr>
<tr>
<td>r2</td>
<td>6.07</td>
<td>6.05</td>
</tr>
<tr>
<td>r3</td>
<td>8.65</td>
<td>8.60</td>
</tr>
<tr>
<td>r4</td>
<td>18.32</td>
<td>18.25</td>
</tr>
<tr>
<td>r5</td>
<td>28.61</td>
<td>28.46</td>
</tr>
</tbody>
</table>

Comparison: NTA-SLP vs TA-SLP (cont.)

- Skew reduction:
  - Avg. skew saving: 59%-77%
  - Max skew saving: 52%-69%
Impact of multiple thermal profiles

- TA-SLP with mid-size initial solution
- Under 10, 100, 1000 thermal profiles:
  - Average skew stays stable
  - Skew range increase with more thermal profiles

![Graph showing impact of multiple thermal profiles](image-url)
• Comparisons among NTA-SLP, TA-SLP, and LTA-SLP

<table>
<thead>
<tr>
<th>Ckt.</th>
<th>NTA-SLP</th>
<th>TA-SLP</th>
<th>LTA-SLP</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td># itr</td>
<td>CPU/itr</td>
<td># itr</td>
</tr>
<tr>
<td>r1</td>
<td>12</td>
<td>2.0</td>
<td>12</td>
</tr>
<tr>
<td>r2</td>
<td>12</td>
<td>8.8</td>
<td>13</td>
</tr>
<tr>
<td>r3</td>
<td>14</td>
<td>18.4</td>
<td>15</td>
</tr>
<tr>
<td>r4</td>
<td>15</td>
<td>75.9</td>
<td>13</td>
</tr>
<tr>
<td>r5</td>
<td>15</td>
<td>184.5</td>
<td>15</td>
</tr>
</tbody>
</table>

• Density of G matrix:
  - r5: G matrix in TA-SLP has 23.6 million non-zero elements
  - r5: G matrix in LTA-SLP has 2.0 million non-zero elements
Conclusions

• Proposed thermal-aware sequential-linear-programming (TA-SLP) based clock sizing

• Addressed the impact of clock sizing on power, thermal and delay

• Minimized thermal-aware clock skew under power and thermal budgets

• Narrowed clock skew range under multiple thermal profiles

• Proposed loosely-thermal-aware sequential-linear-programming (LTA-SLP)
Thank you