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Critical-PMOS-Aware Clock Tree Design Methodology for Anti-Aging Zero Skew Clock Gating

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SYSTEM VLSI CAD LAB.

Outline

- Introduction
- Preliminaries
- The Drawback of Conventional Clock Tree
- Anti-Aging Clock Tree
- ILP Formulations for Enable Logic Modification
- Experimental Results
- Conclusions


Introduction

- The most common clock distribution is to insert a number of buffers along the paths from the clock source to the flip-flops forming a clock tree structure.
- Clock skew minimization is always an important topic in the design of synchronous sequential circuit.
- Since the clock signal is the most active signal in the circuit, it is also important to distribute the clock signal with low power.
- Clock gating has been recognized as one of the most effective techniques to reduce the power consumption.


Introduction

- In deep sub-micron era, the NBTI (negative bias temperature instability) effect is a serious concern for the long-term reliability of a circuit.
- Under a target lifetime (e.g., ten years), the NBTI delay degradation of a PMOS transistor increases with its active probability.
- The NBTI effect is one source of the clock skew.
- In this paper, we present the first attempt for anti-aging zero skew clock gating.


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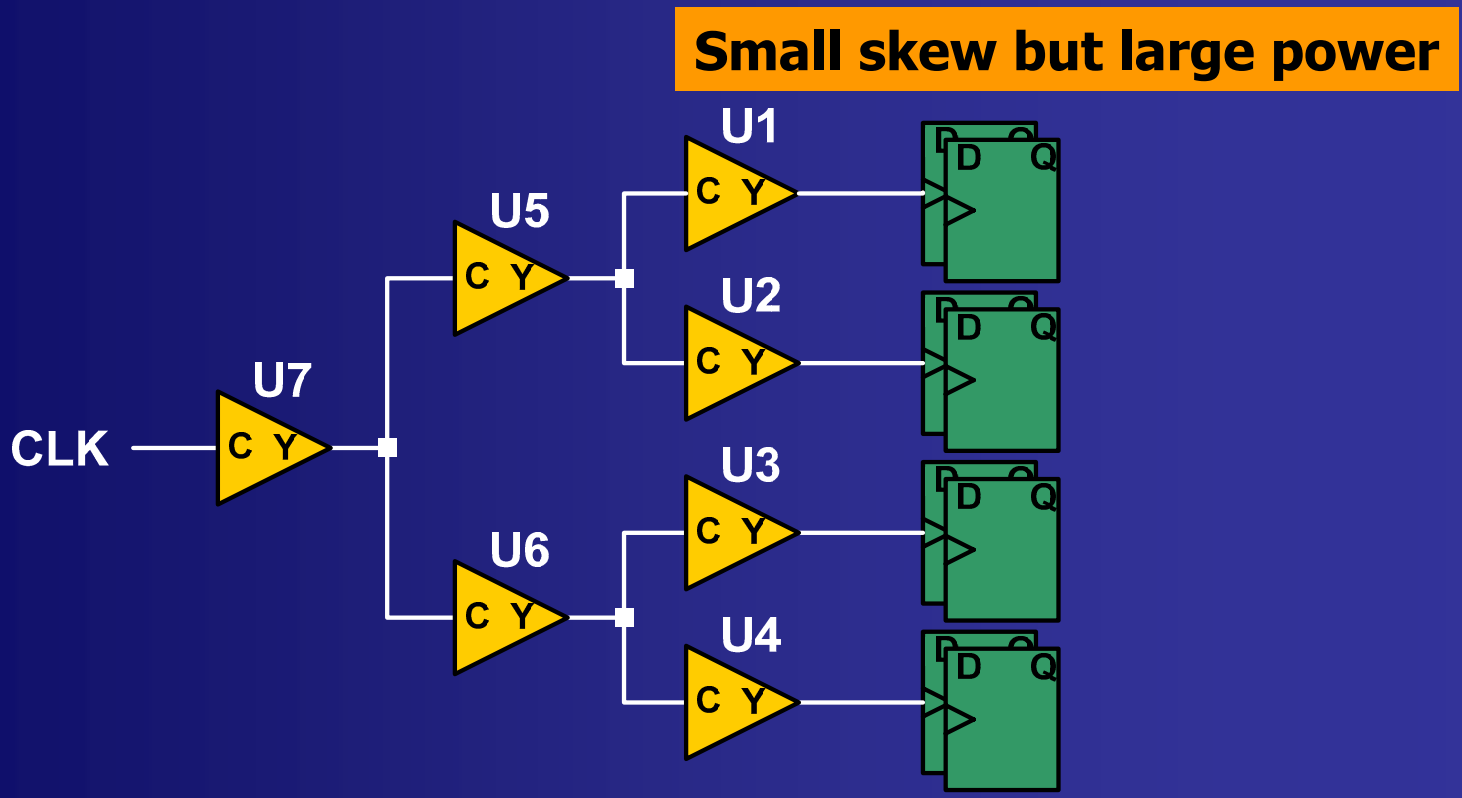
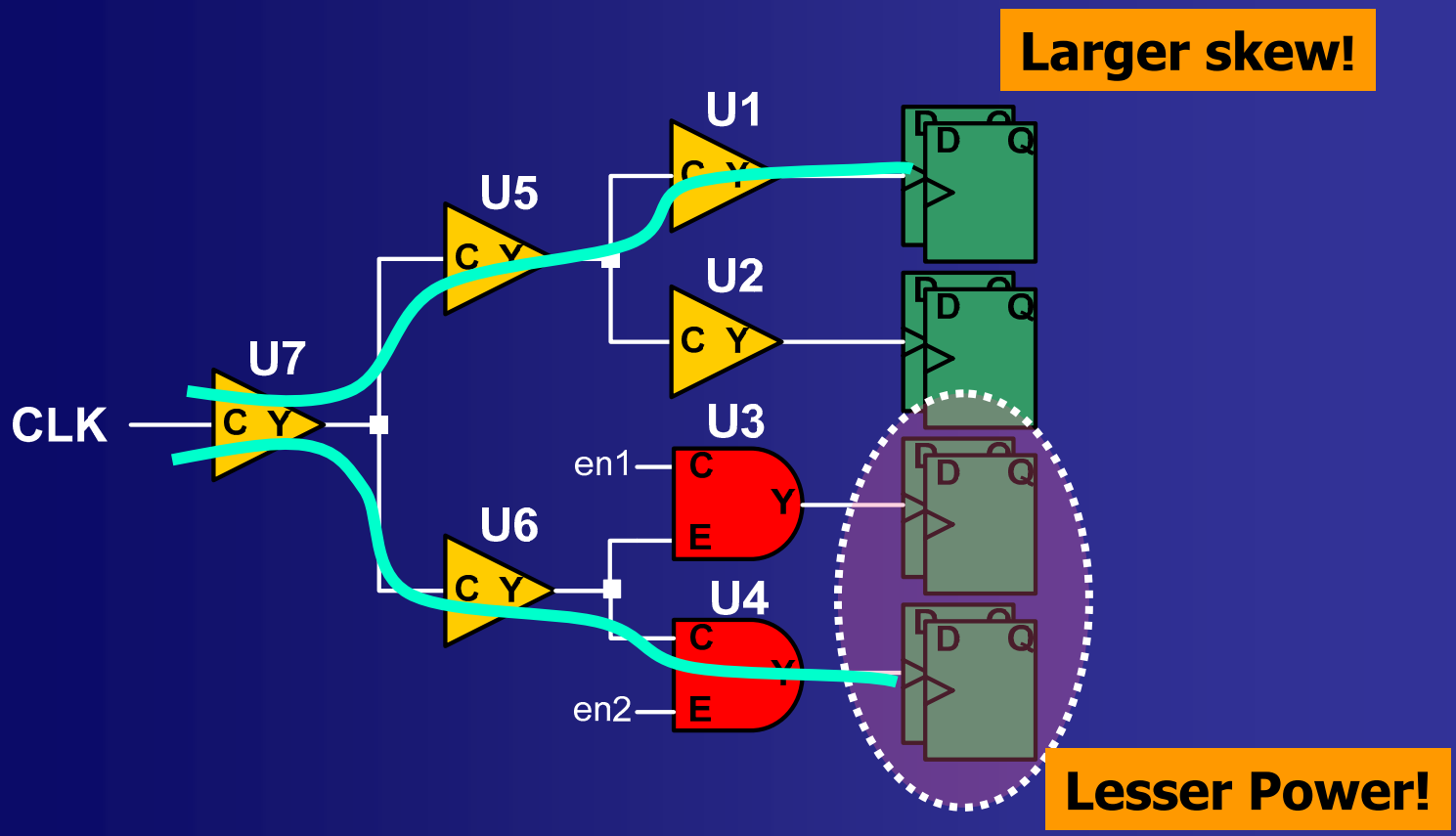
Preliminaries – Buffered Clock Tree

- Buffered Clock Tree



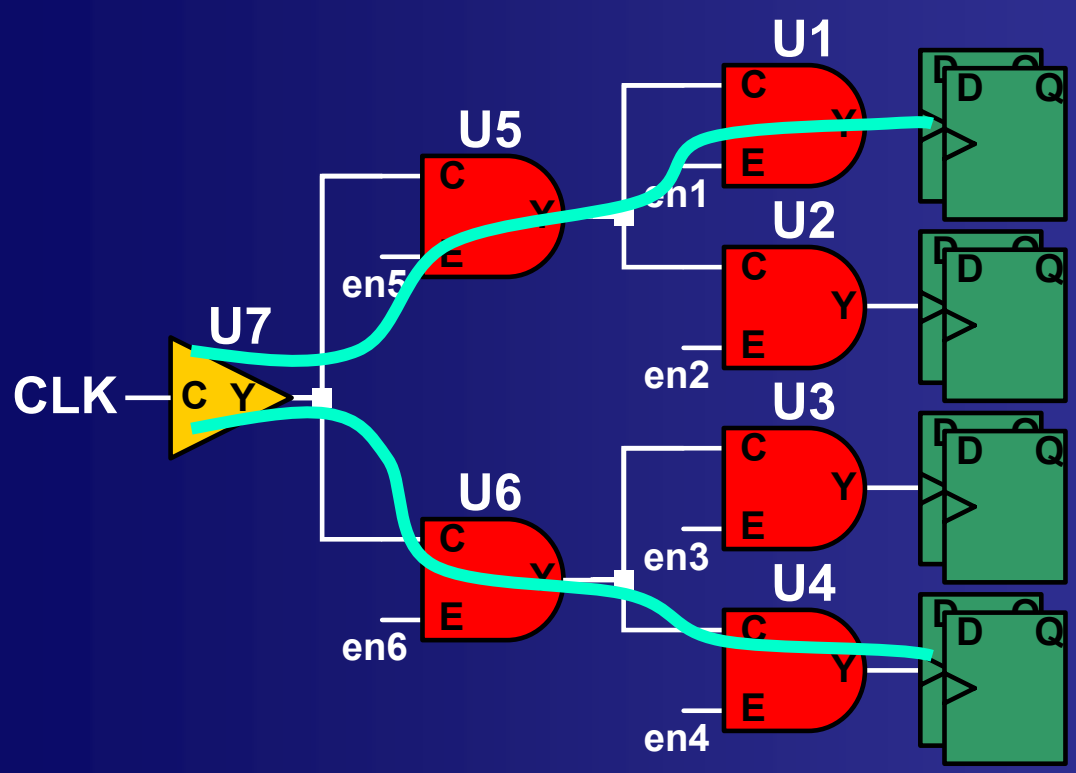
Preliminaries – Gated Clock Tree

- Clock Gating



Preliminaries – Conventional Clock Tree

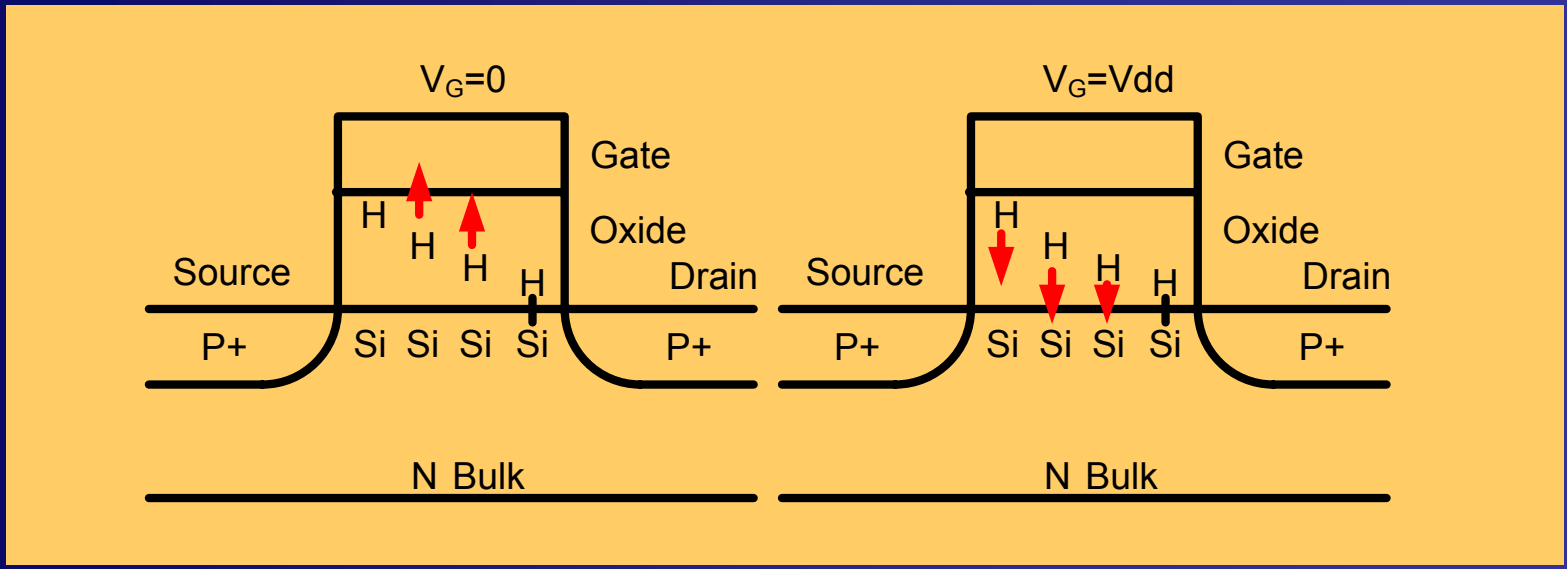
- Type-Matching Clock Tree can reduce the skew due to clock gating.



Zero skew!

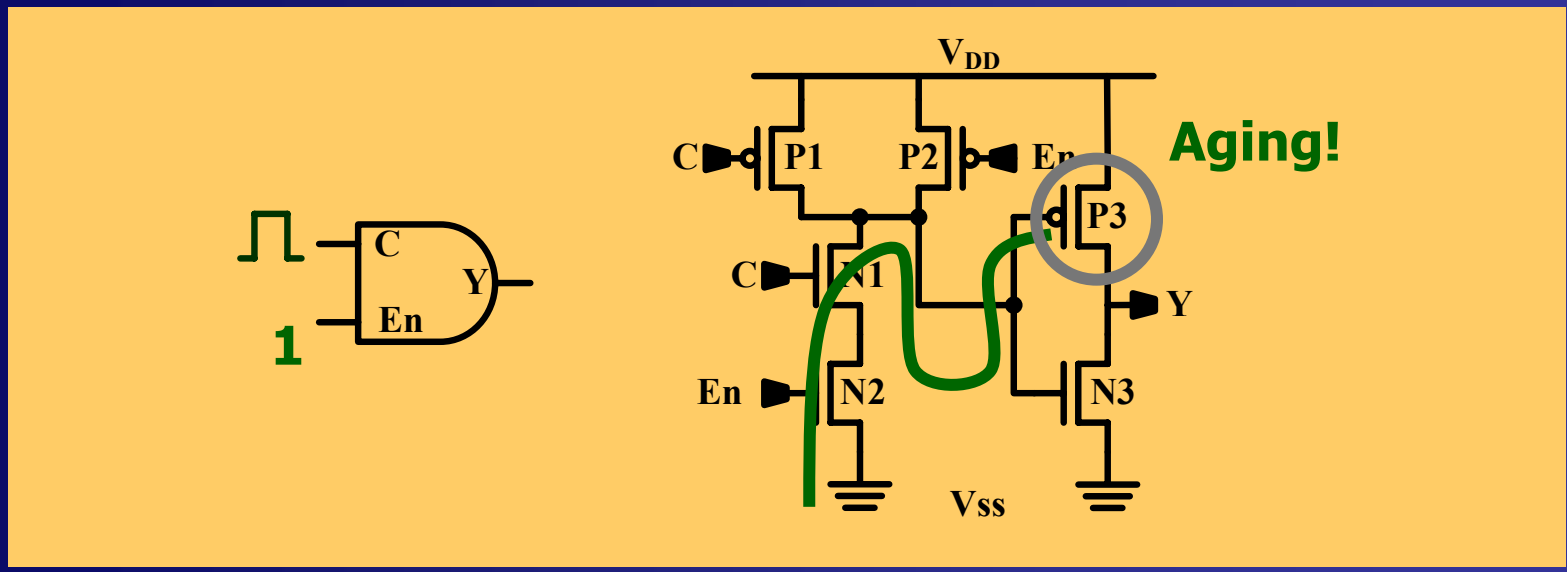
Preliminaries – NBTI Delay

- NBTI (Negative Bias Temperature Instability) effect becomes serious due to thinner gate oxide.
- NBTI increases threshold voltage (i.e. increasing delay).



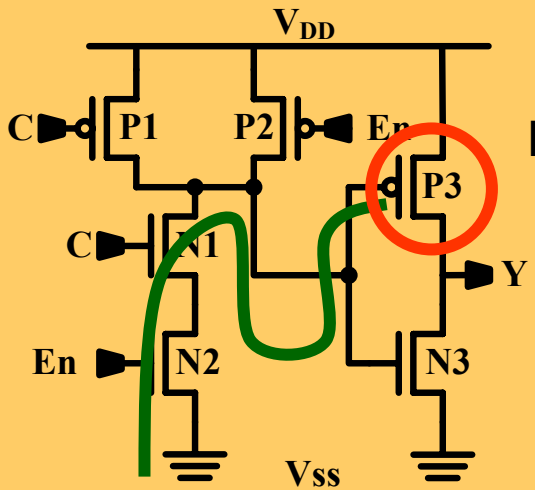
Preliminaries – NBTI while using AND gate

- Analyzing the AND gate in a general gated clock tree.
- P3 is actived while En=1
- The aging delay of PMOS P3 is proportional to the active probability of En signal



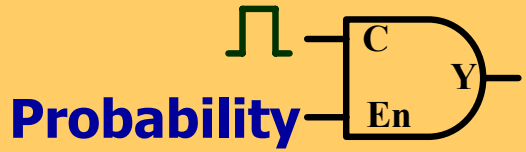
Preliminaries – Skew Due to Degradation Difference

Probability
20%

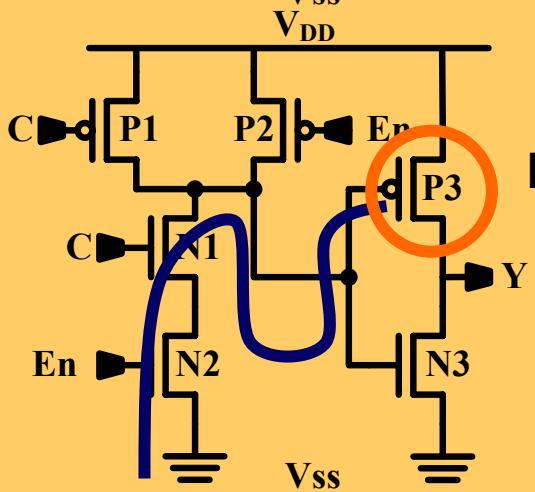


Delay = 0.3

Different Delay Degradations!



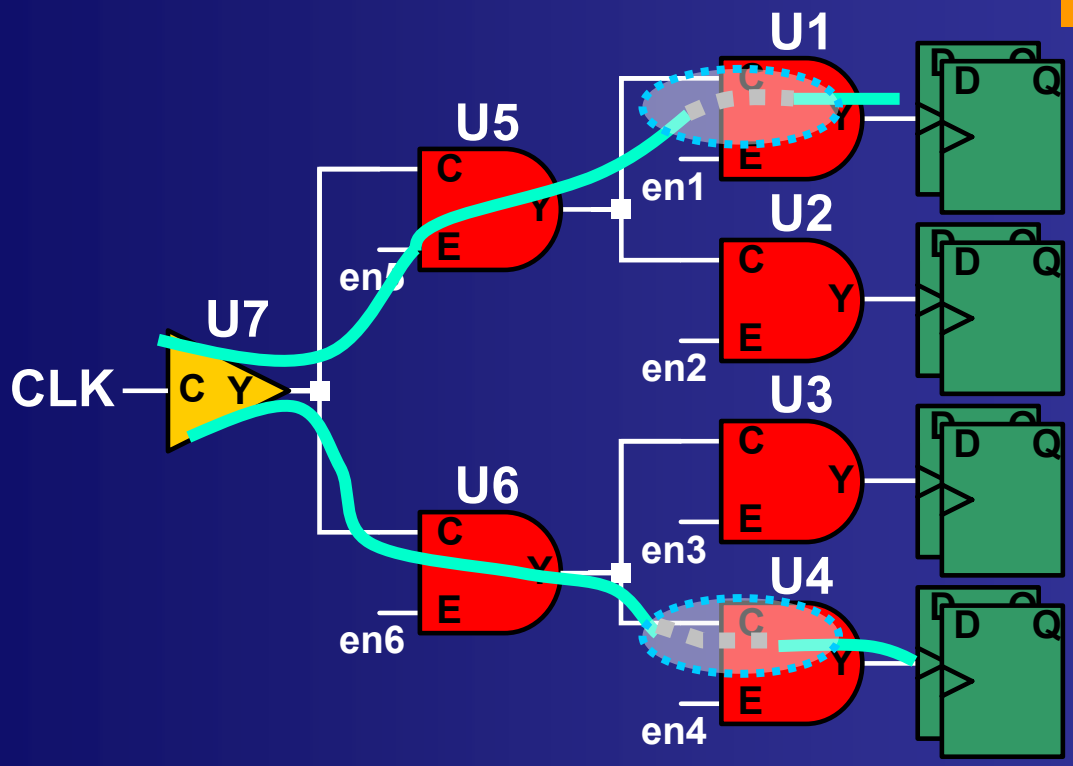
Probability
60%



Delay = 0.5

Preliminaries –
Weakness of Conventional Clock Tree

- As time goes by, the NBTI effect causes the aging skew if the probabilities of enable signals are different.



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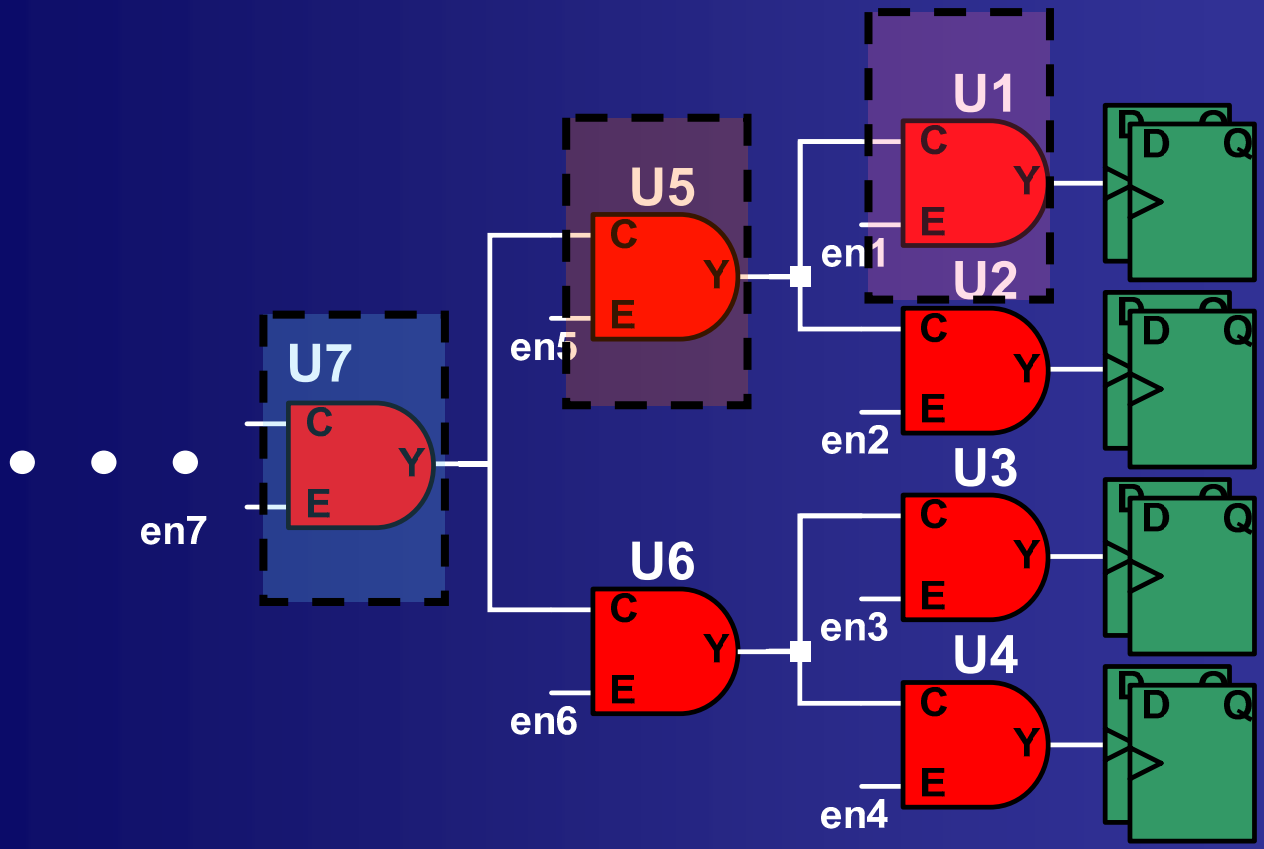
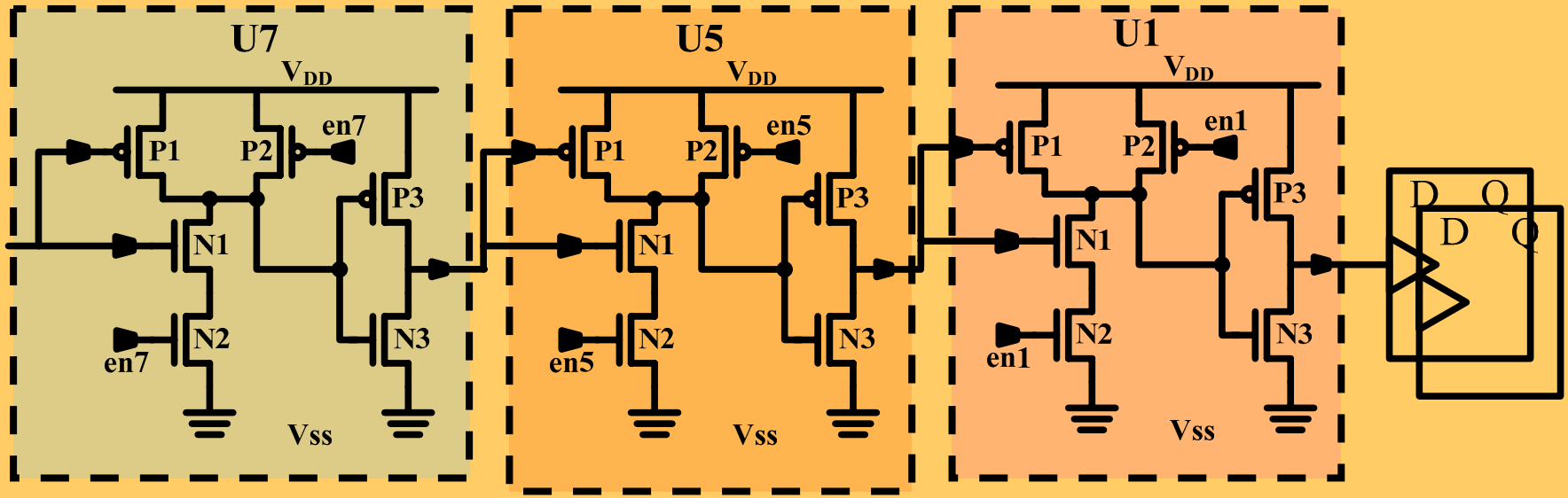
Conventional Clock Tree



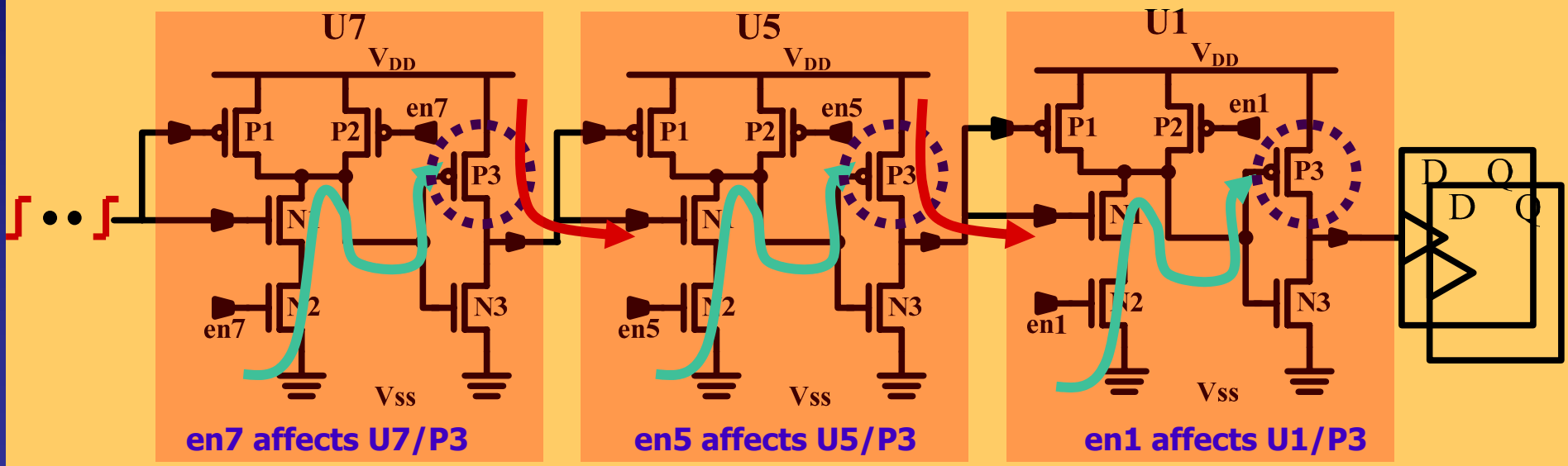
Conventional Clock Tree in Circuit Level



Conventional Clock Tree in Circuit Level

- If registers are rising-edge-triggered

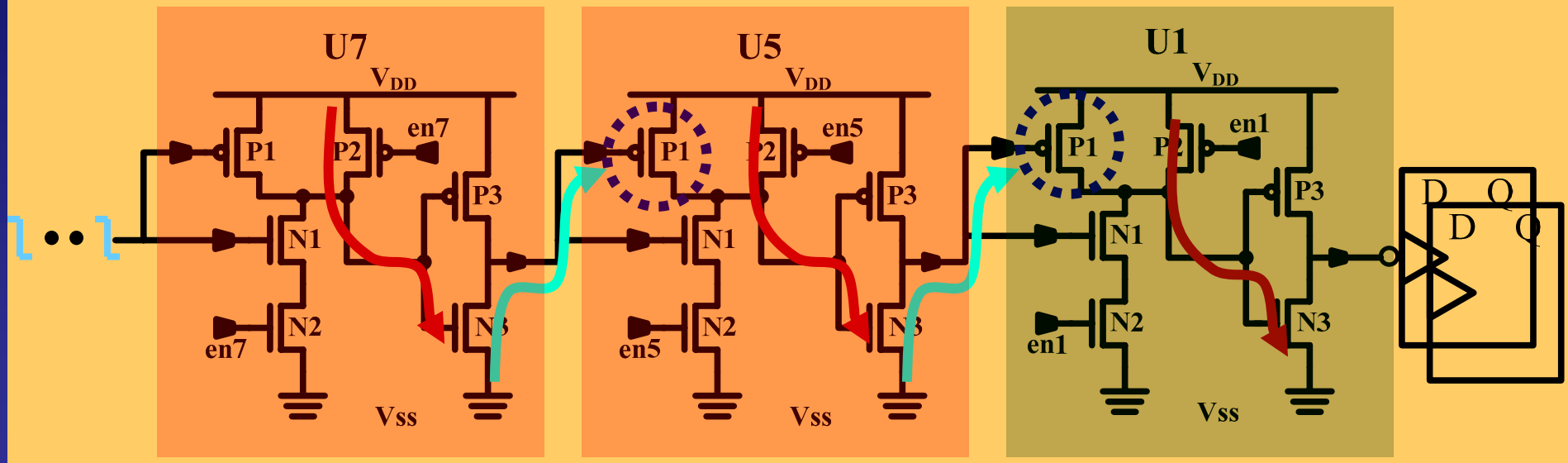
Aging effect needs to be considered in every level



Conventional Clock Tree in Circuit Level

- If registers are falling-edge-triggered

Only one "free" level in the clock tree

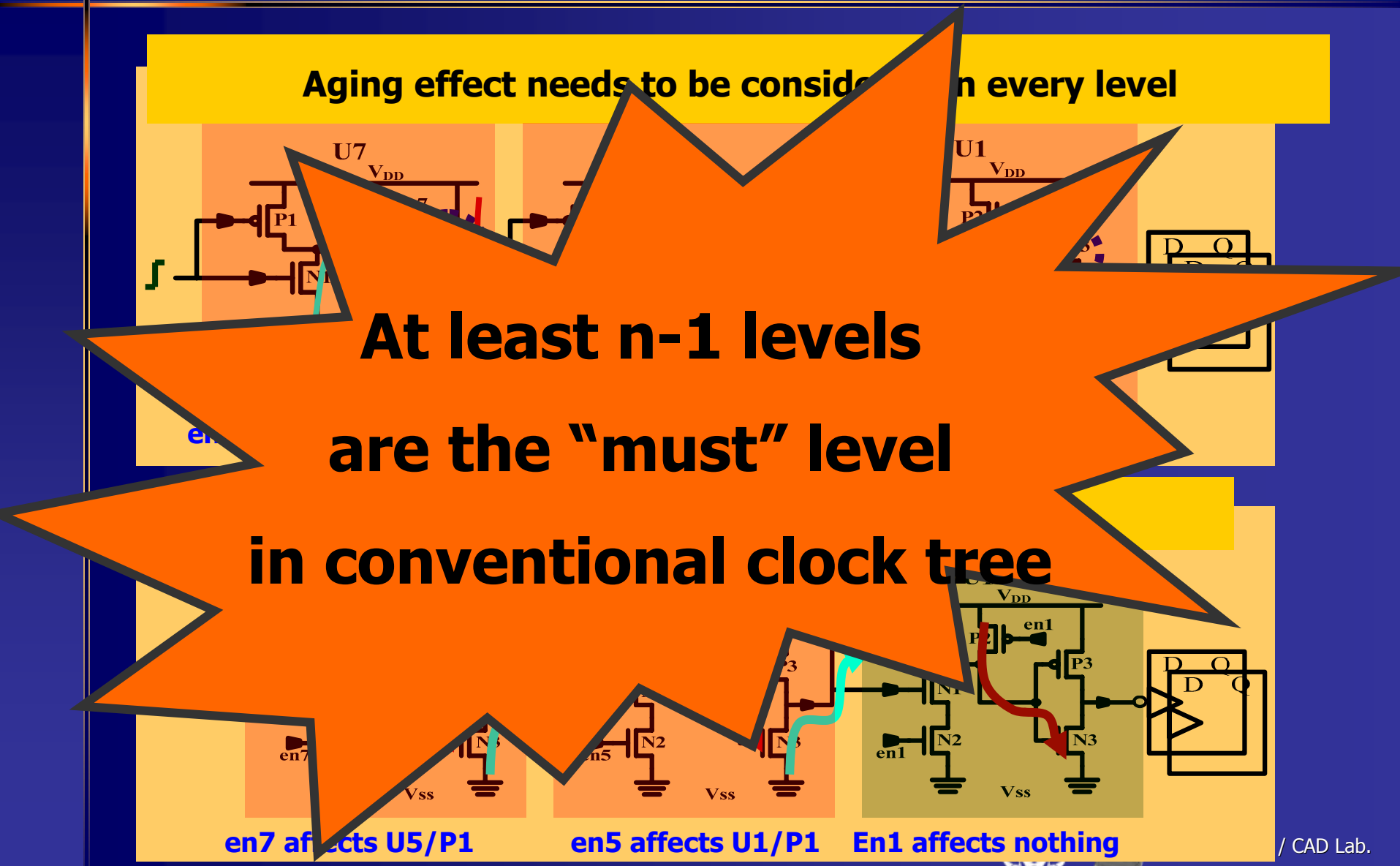


en7 affects U5/P1

en5 affects U1/P1

En1 affects nothing

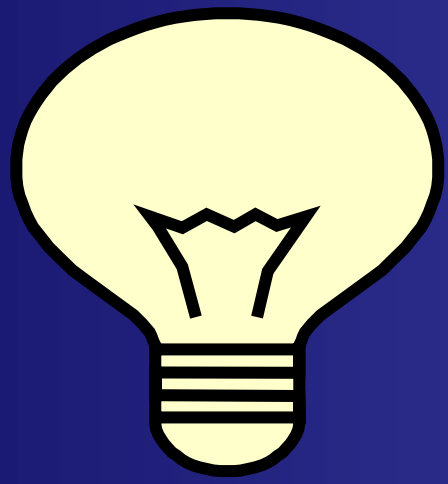
Conventional Clock Tree in Circuit Level



How to solve this aging skew problem ?

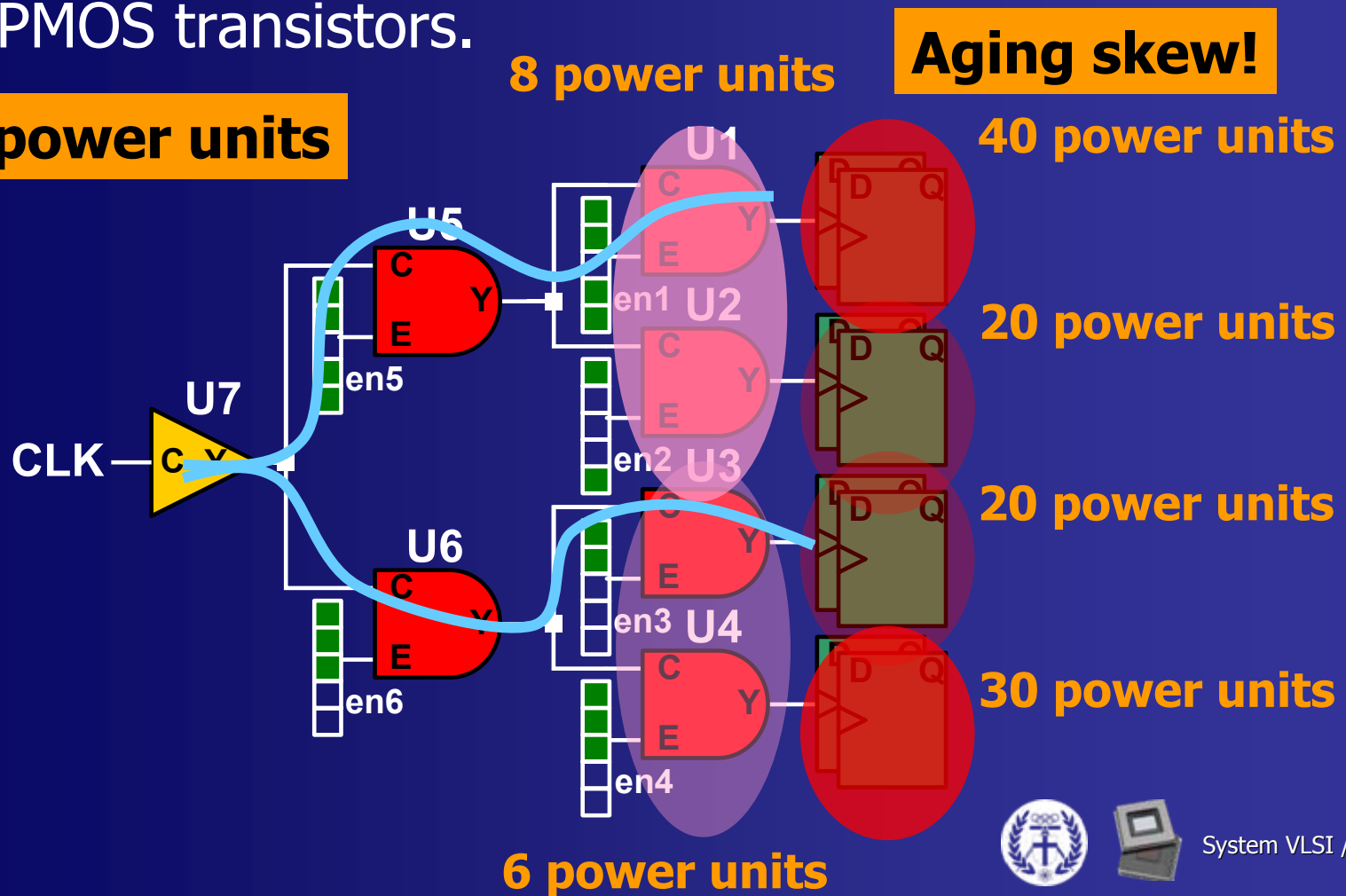
How to solve this aging skew problem

- Since the PMOS transistors at the same level have different active probabilities, we can increase the active probabilities of clock gates to ensure that the clock gates at the same level always have the same active probability.



Conventional Clock Tree – an Example

- The delay degradation of each clock gate is linearly proportional to the active probabilities of PMOS transistors.



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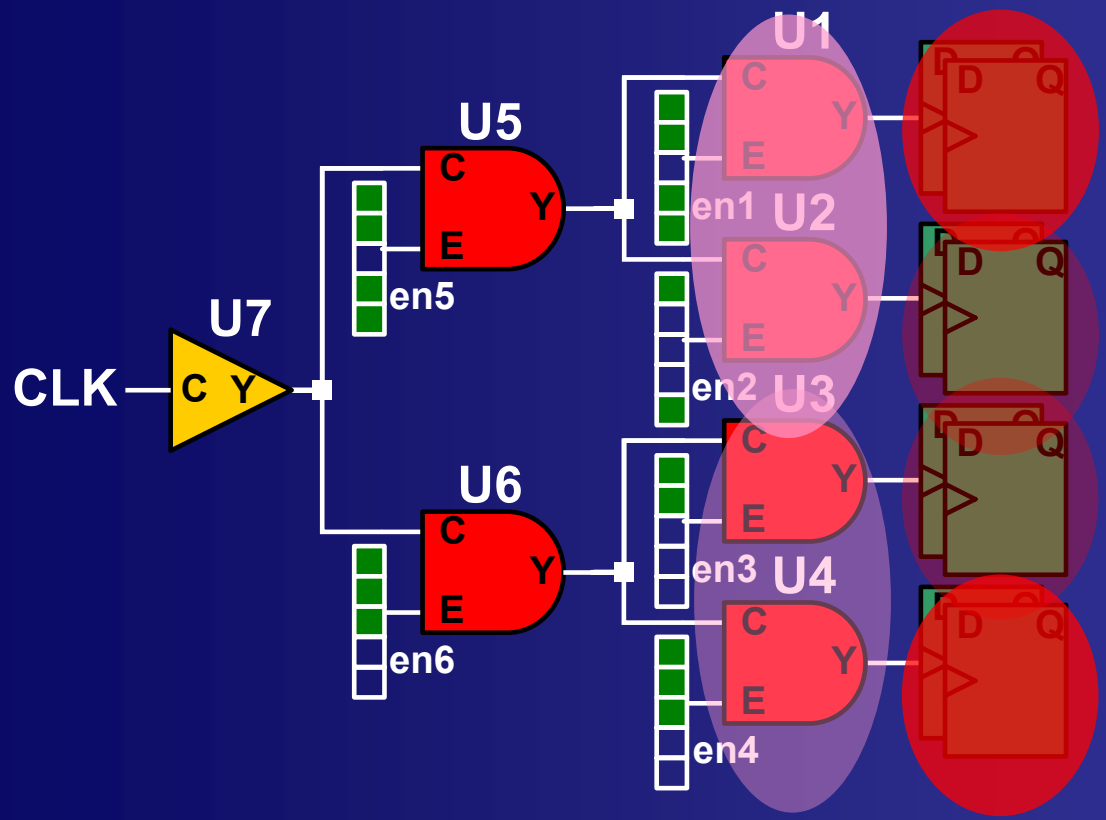
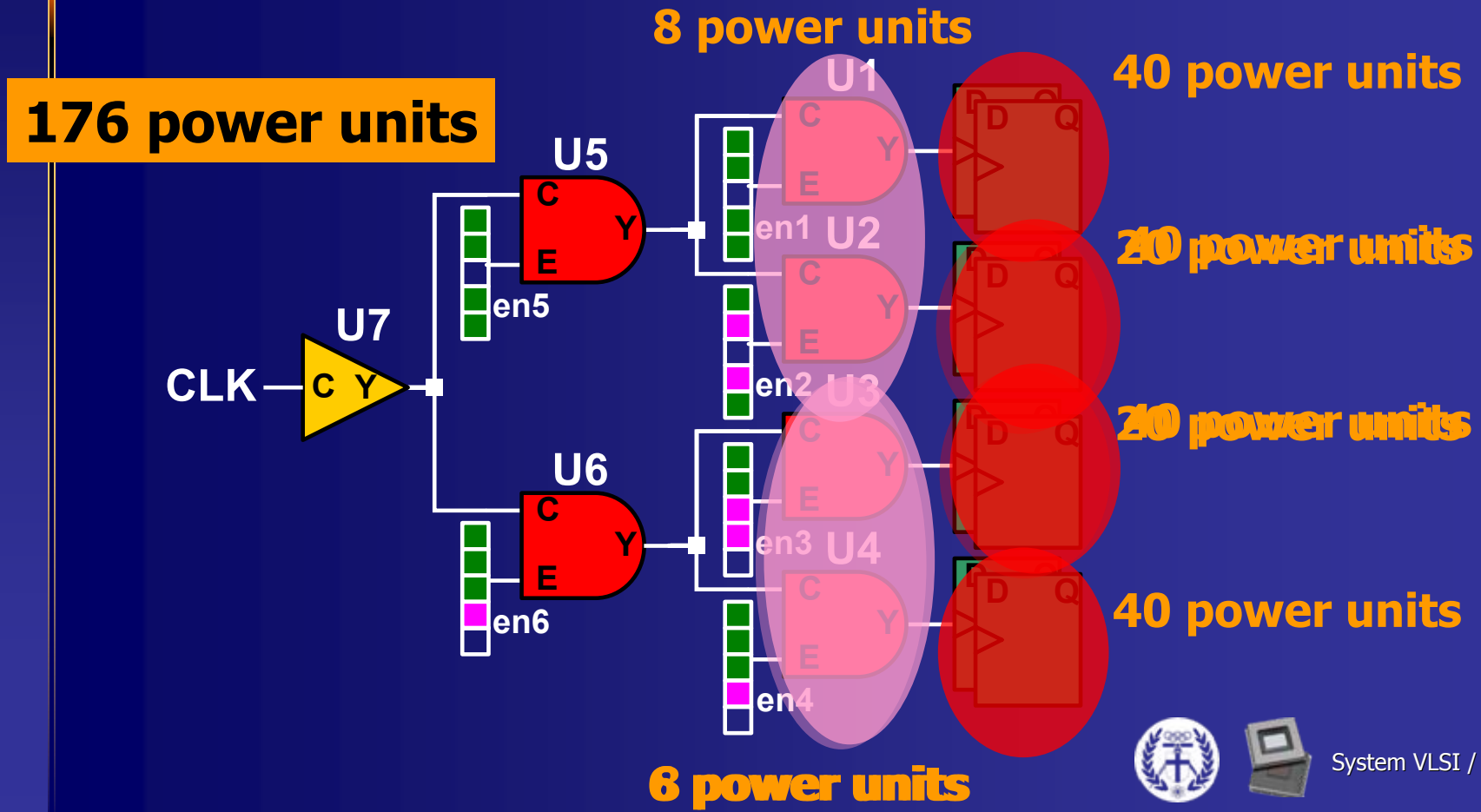


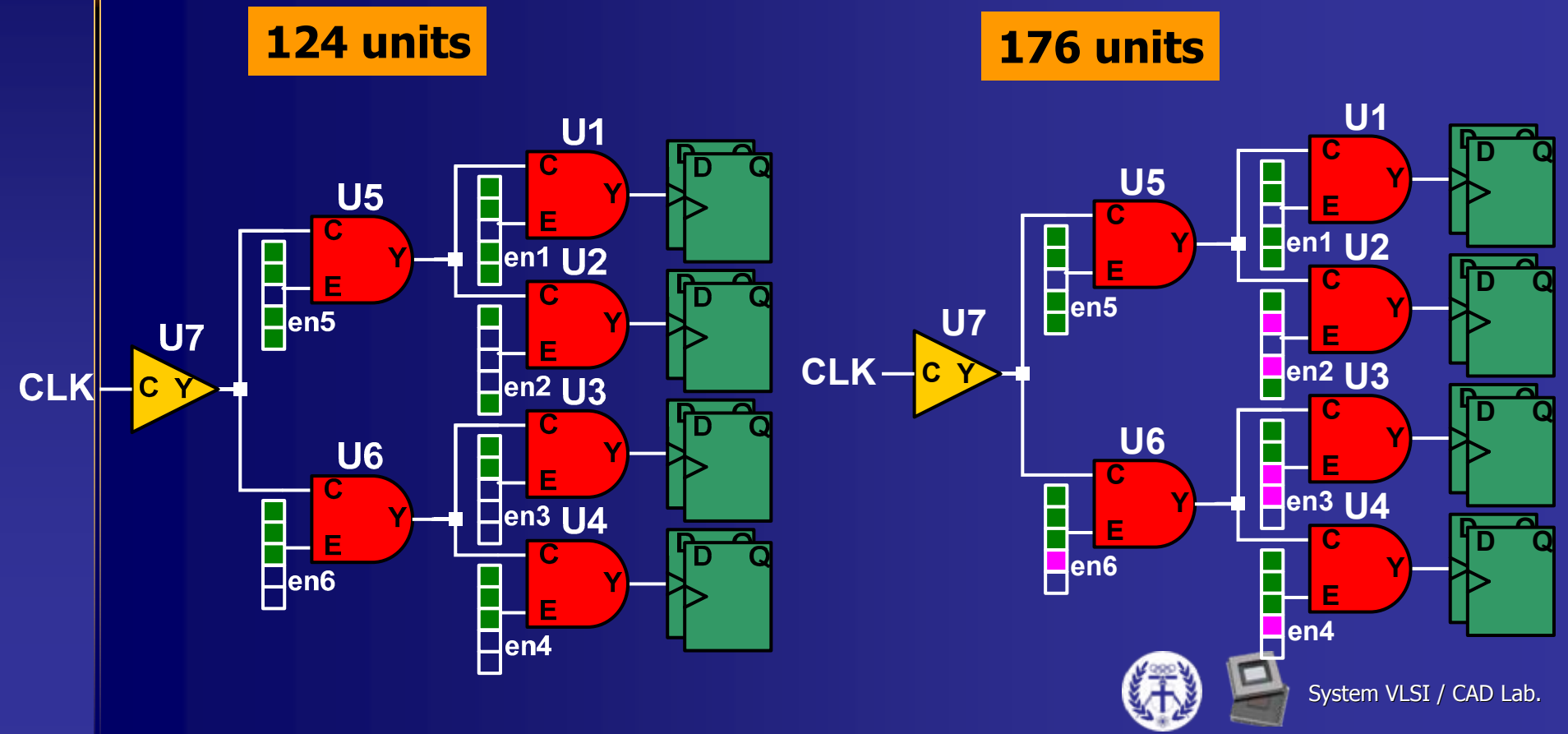
Conventional Clock Tree – an Example

- If the active probabilities of clock gates at the same level are the same, the NBTI delay degradations will be the same.



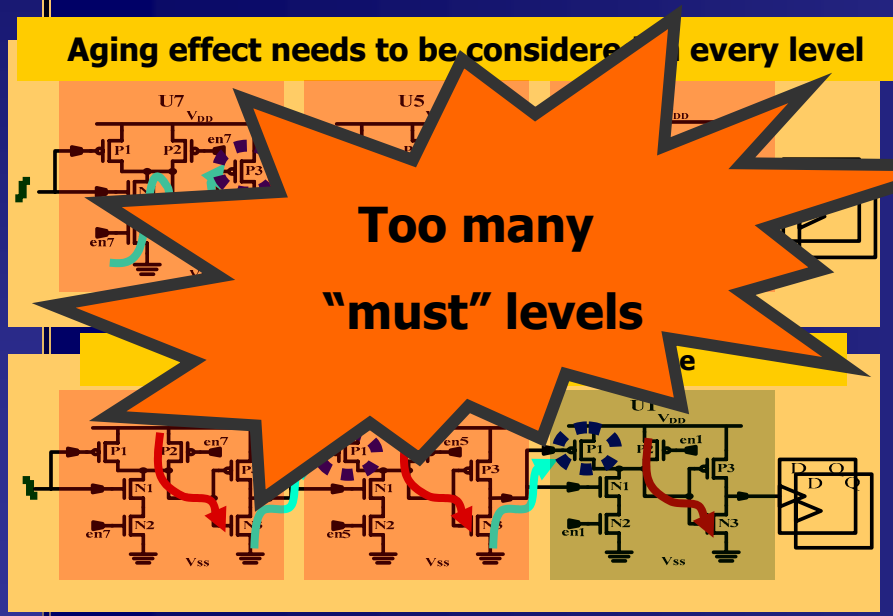
Conventional Clock Tree – an Example

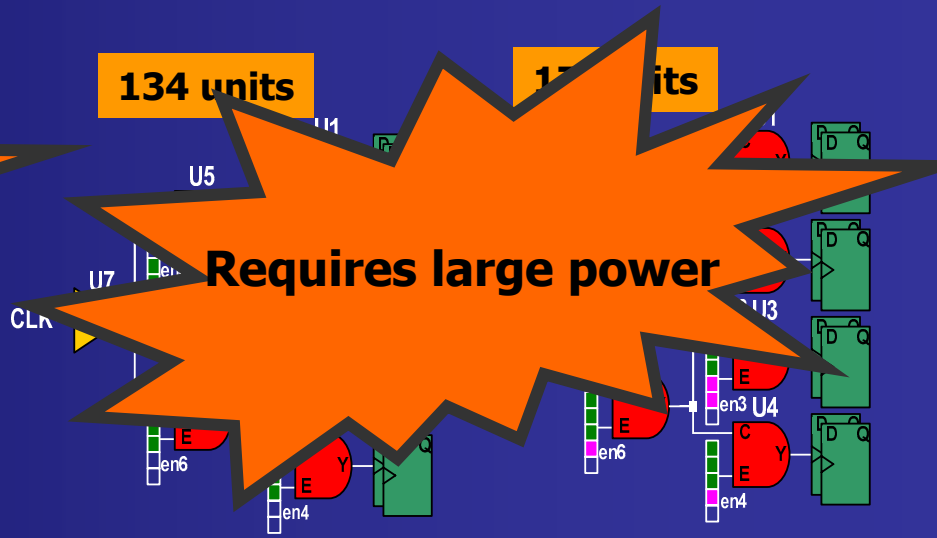
- Although we can eliminate the aging skew by increasing the active probabilities of clock gates , it requires extra 52 power units.



Drawback of Conventional Tree

- In worst case, every level is the "must" level
- It requires large power to eliminate aging skew





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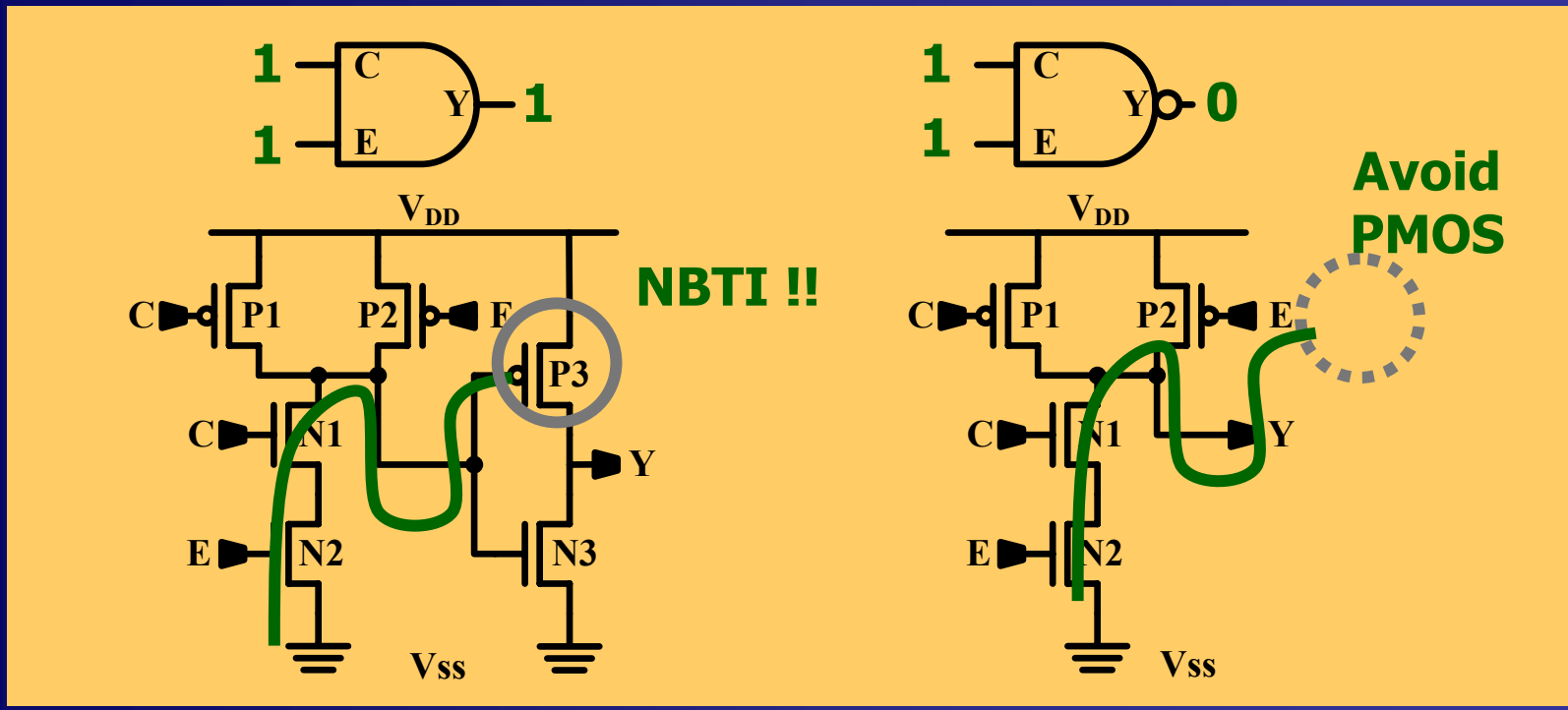
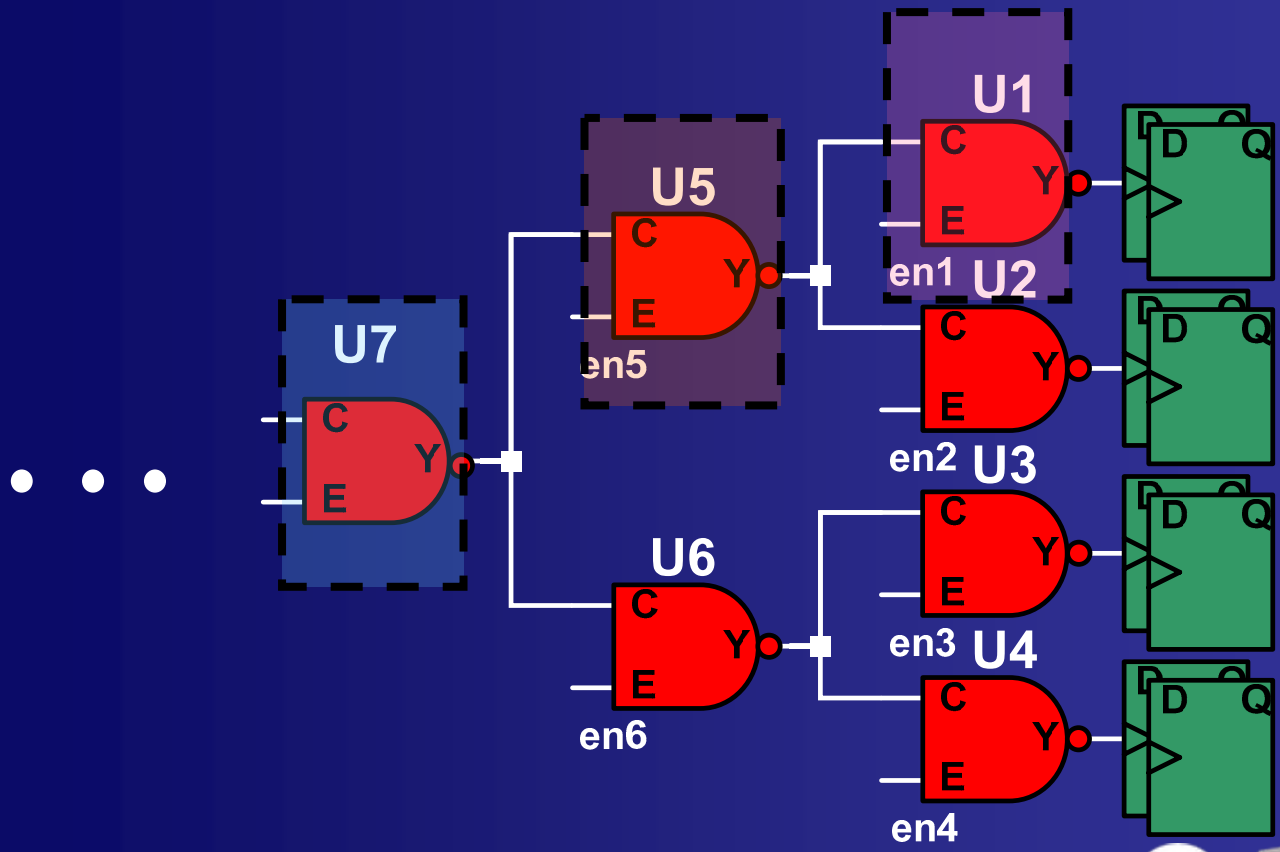
Anti-Aging Clock Tree (1/2)

- Since the NBTI only affects PMOS transistors, by carefully planning the clock signal propagation paths, we can let the active probabilities do not affect the degradation difference.

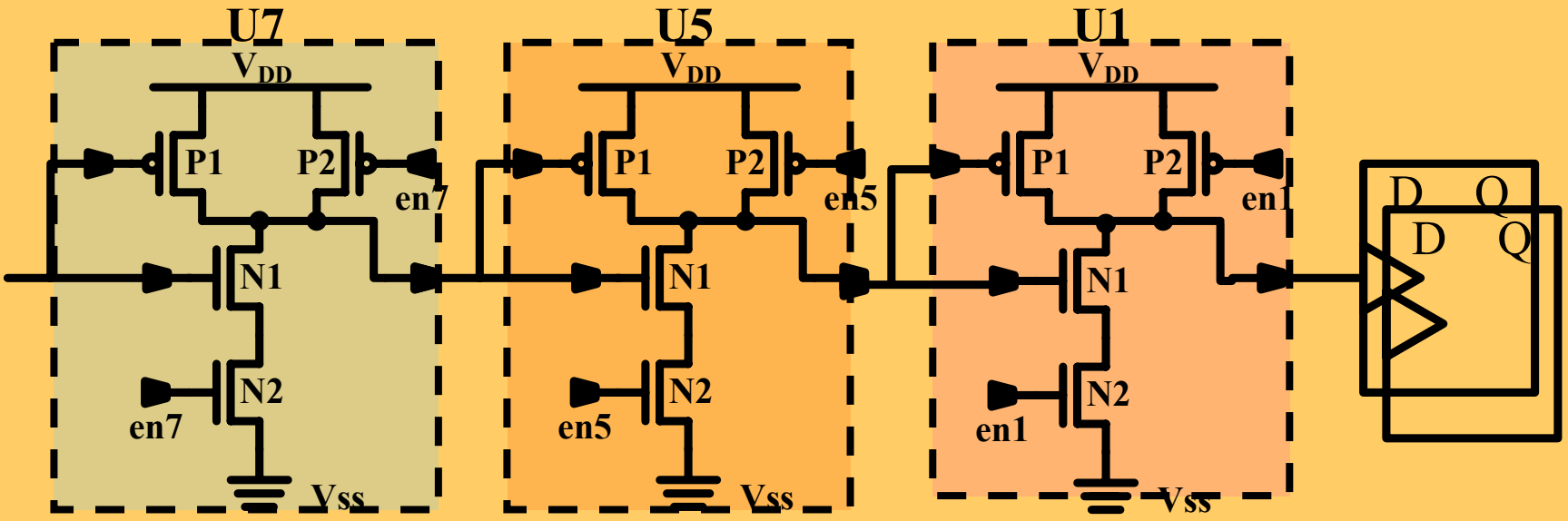


Anti-Aging Clock Tree (2/2)

- In our design methodology, we use NAND-type-matching clock tree.



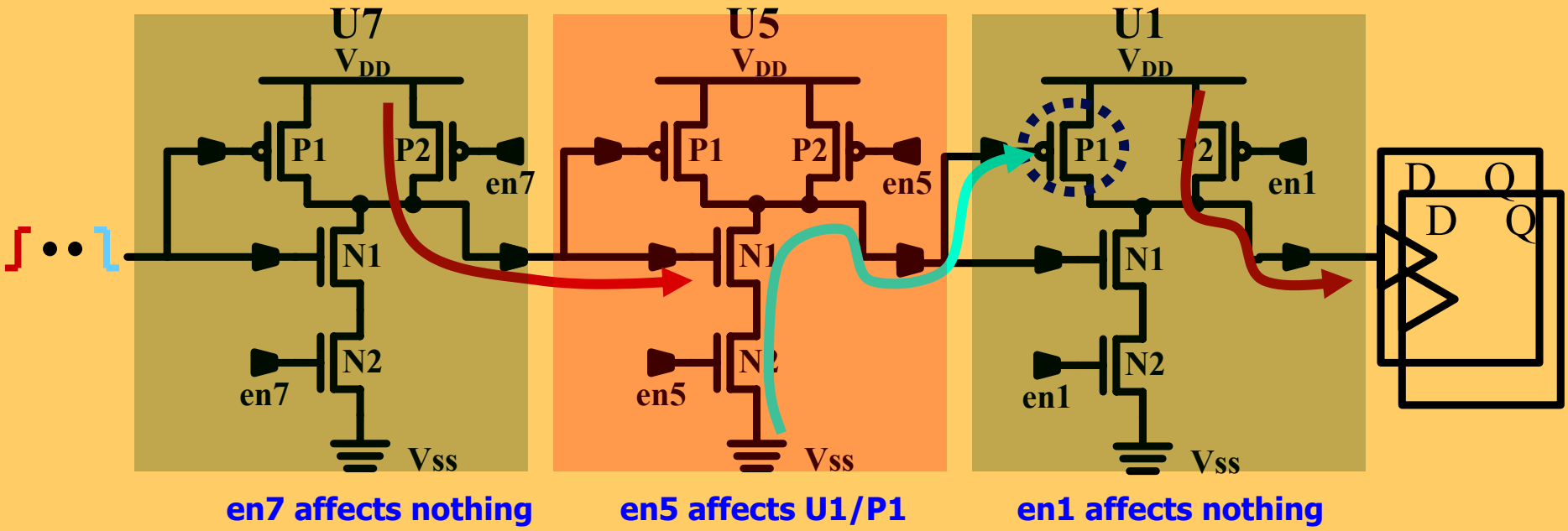
Anti-Aging Clock Tree in Circuit Level



Anti-Aging Clock Tree in Circuit Level

- If registers are rising-edge-triggered

Aging effect needs to be considered in even levels

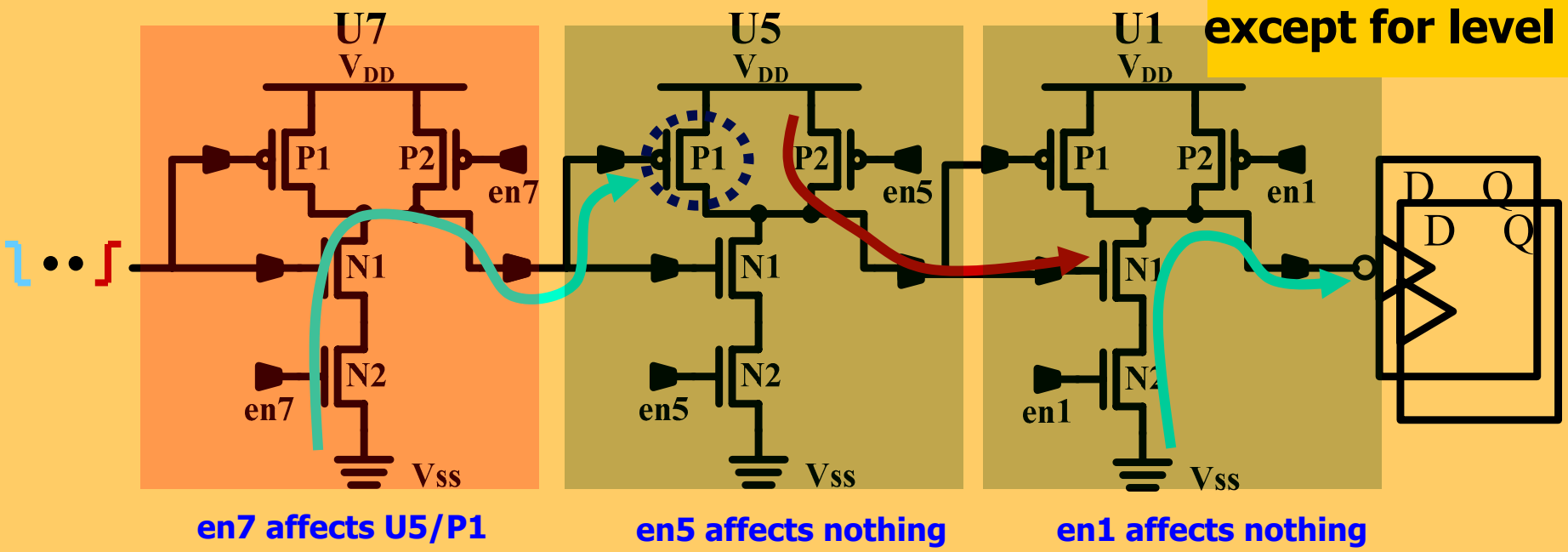


Anti-Aging Clock Tree in Circuit Level

- If registers are falling-edge-triggered

Aging effect needs to be considered in odd levels

except for level 1



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en5 affects nothing

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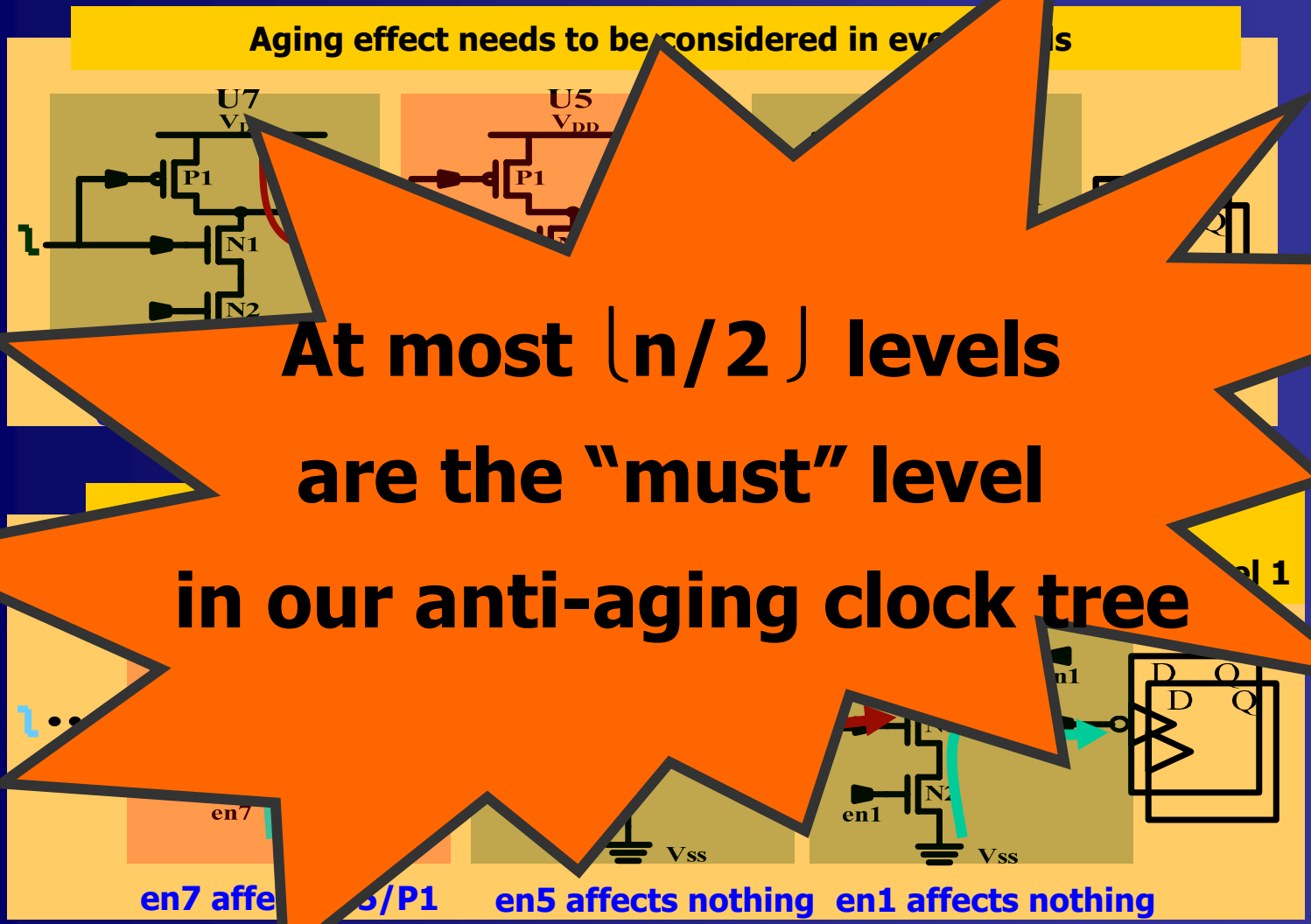
Anti-Aging Clock Tree in Circuit Level



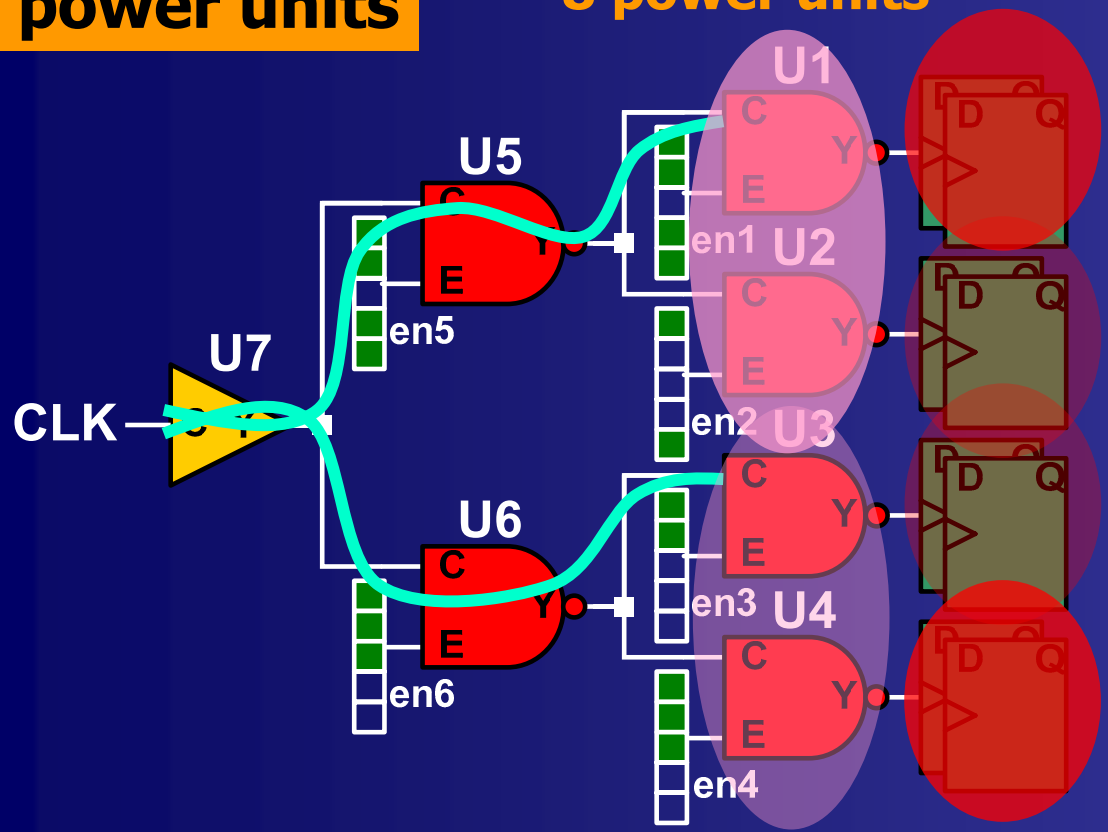
At most ⌊n/2⌋ levels are the "must" level in our anti-aging clock tree

Anti-Aging Clock Tree – an Example

124 power units

8 power units

Aging skew!



40 power units

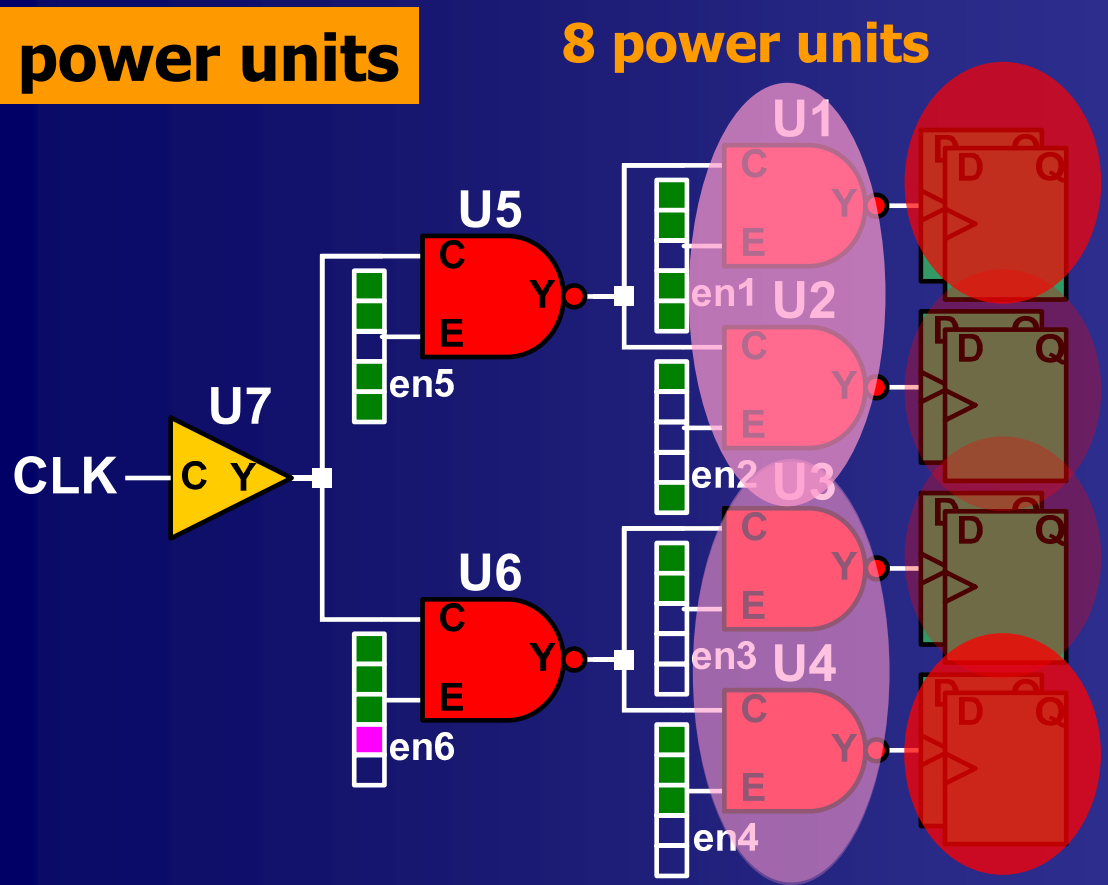
20 power units

20 power units

30 power units

6 power units

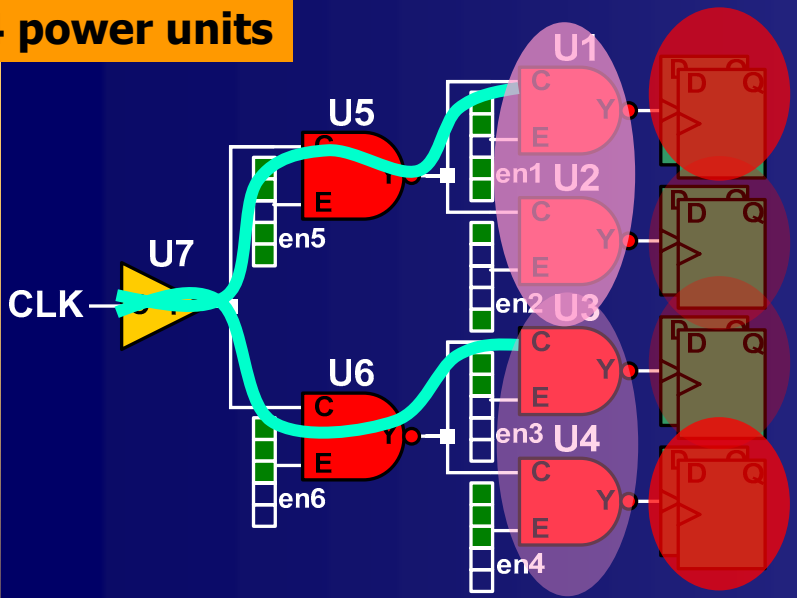
Anti-Aging Clock Tree – an Example



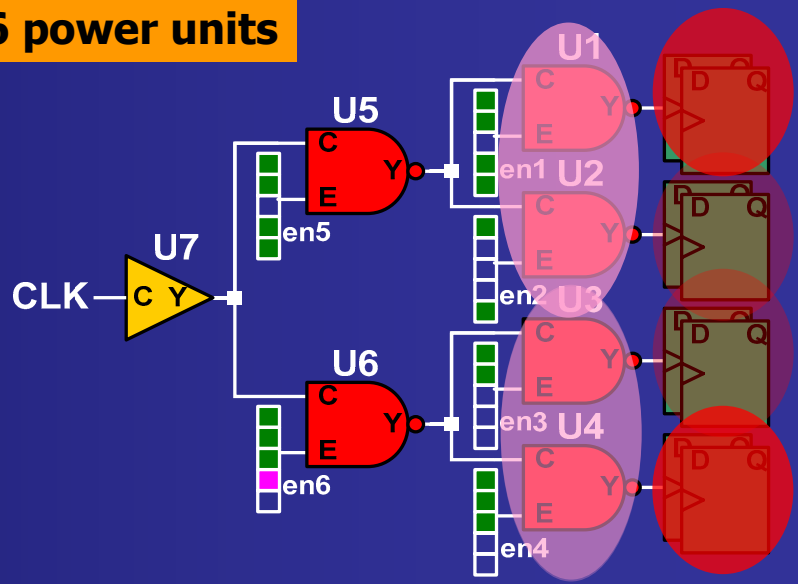
Anti-Aging Clock Tree – an Example

- After ten-year operation, the clock skew of clock tree is still 0 ps. Compared with AND-type anti-aging clock tree, it saves a lot of power consumption.

124 power units

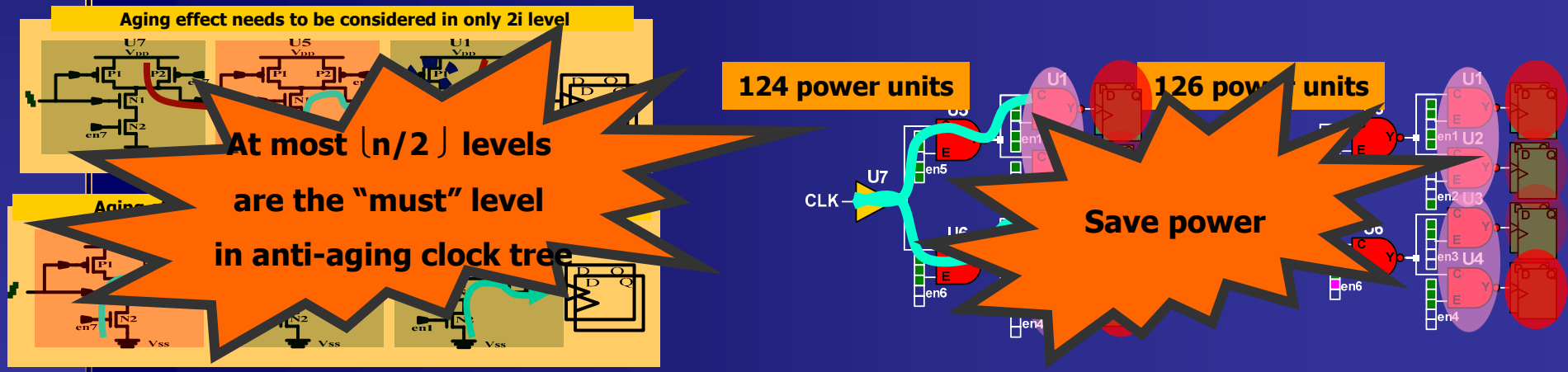


126 power units



Advantages of Anti-Aging Clock Tree

- In worst case, only $\lfloor n/2 \rfloor$ levels need to be considered
- It requires less power consumption to eliminate aging skew
- It is still a type-matching clock tree. Therefore, our anti-aging clock tree has all the benefits of type-matching clock tree.



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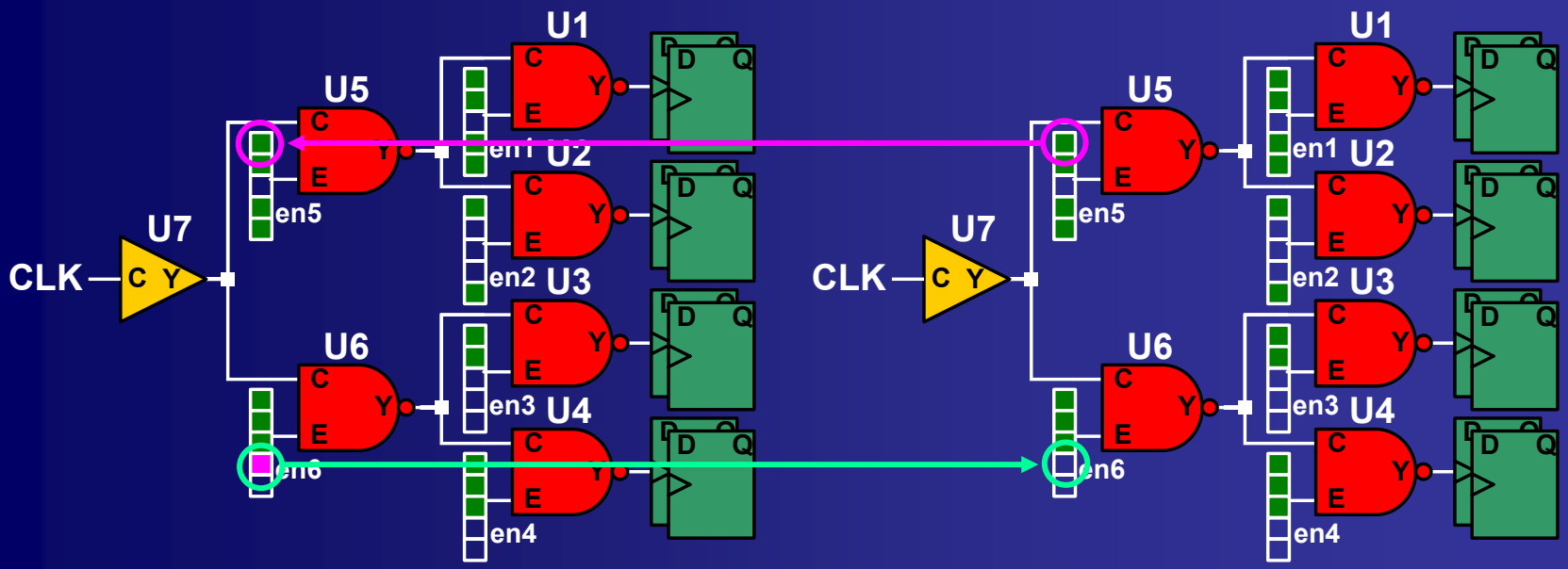
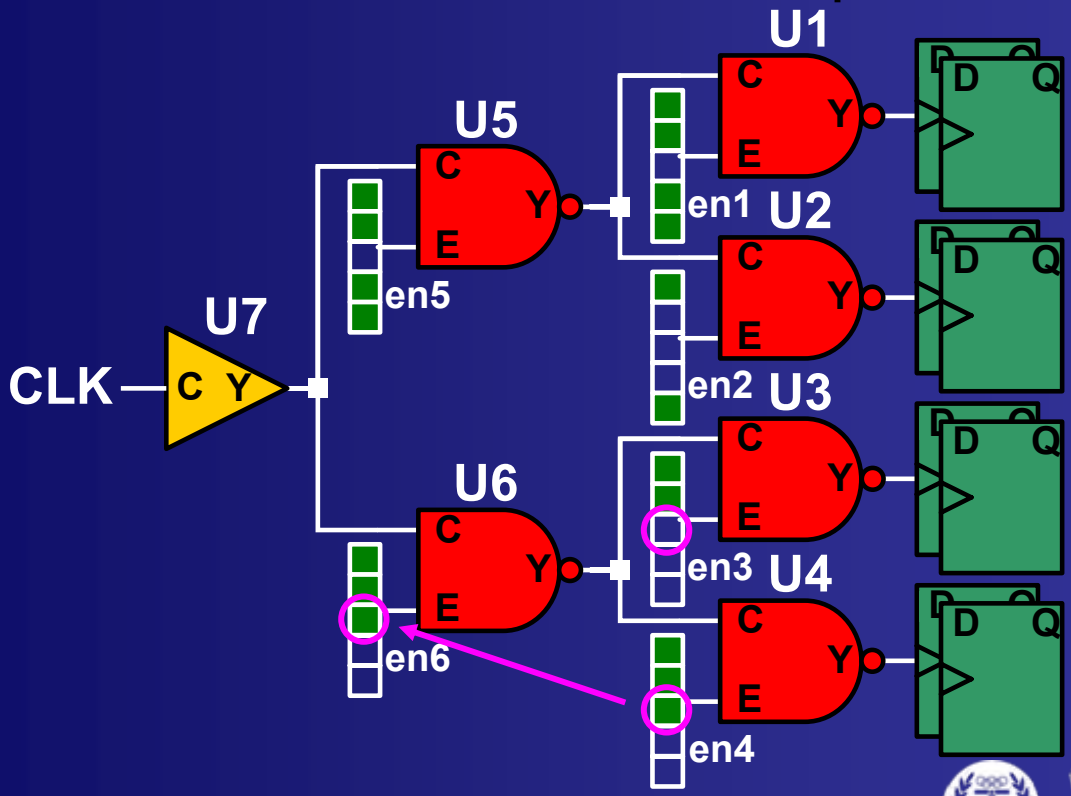
ILP Formulations – Formula 1

- Formula 1 $X_{u,s} \geq a_{u,s}$
  - If clock gate u is active at control step s in the original clock tree, then clock gate u must be also active at control step s in the anti-aging clock tree.



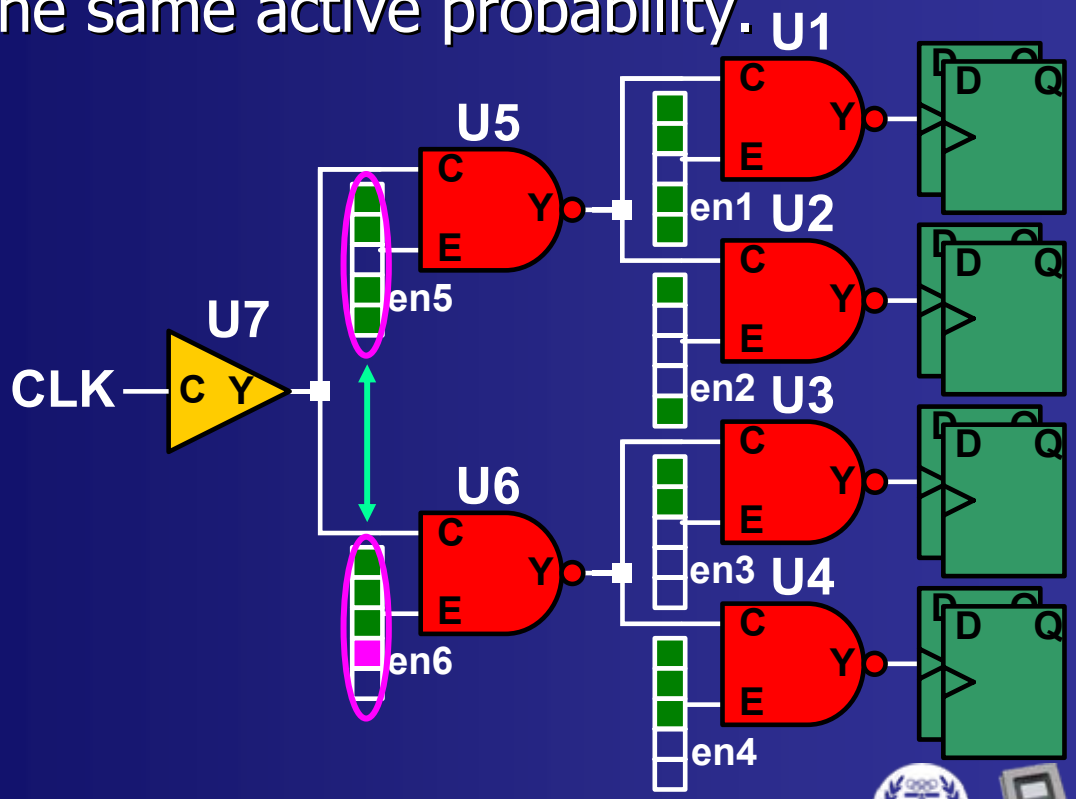
ILP Formulations – Formula 2

- Formula 2 $X_{v,s} \geq X_{u,s}$
  - Consider the anti-aging clock tree. If clock gate u is active at control step s, then its predecessor gate v must be also active at control step s.



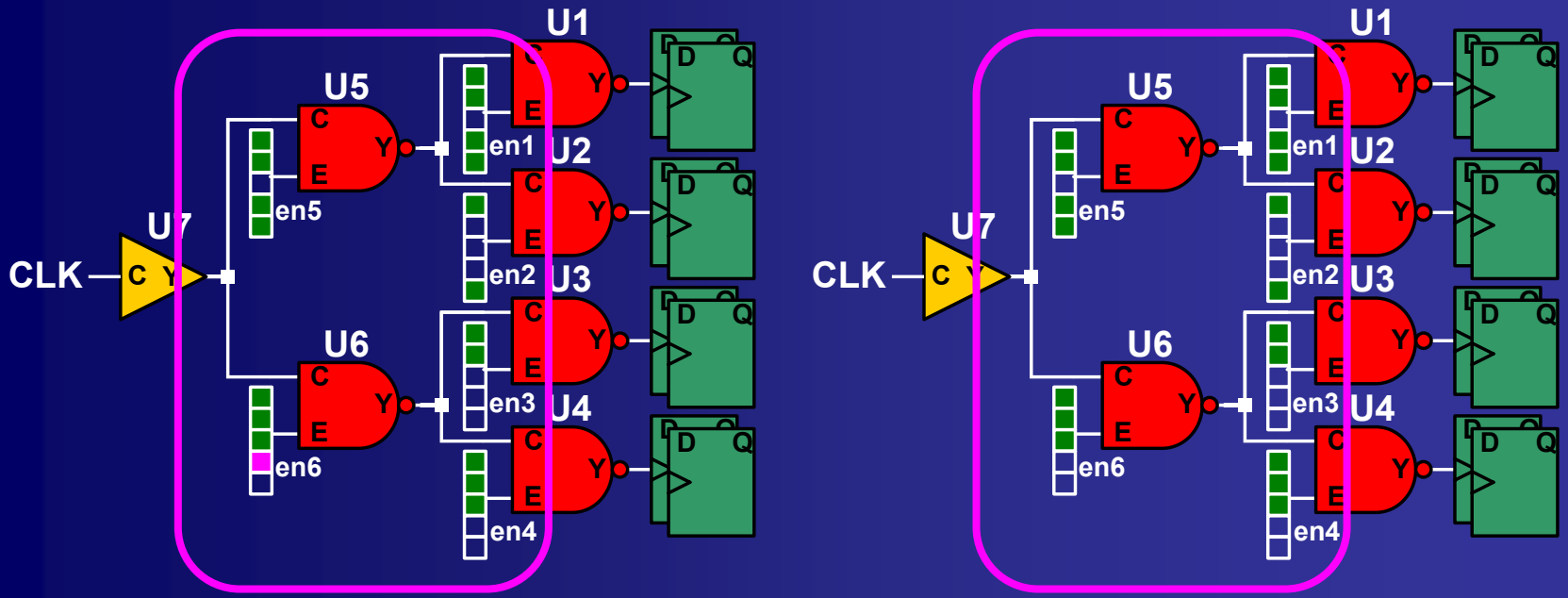
ILP Formulations – Formula 3

- Formula 3 $\sum_{s \in B} X_{u,s} = \sum_{s \in B} X_{v,s}$
  - Consider the anti-aging clock tree. If clock gate u and clock gate v are at the same "must" level, they must have the same active probability.



ILP Formulations for Enable Logics – Objective Function

- Minimization $\sum_{u \in A} \sum_{s \in B} X_{u,s} \times P_{u,s} - \sum_{u \in A} \sum_{s \in B} a_{u,s} \times P_{u,s}$
  - Our objective function is to minimize the power consumption overhead.



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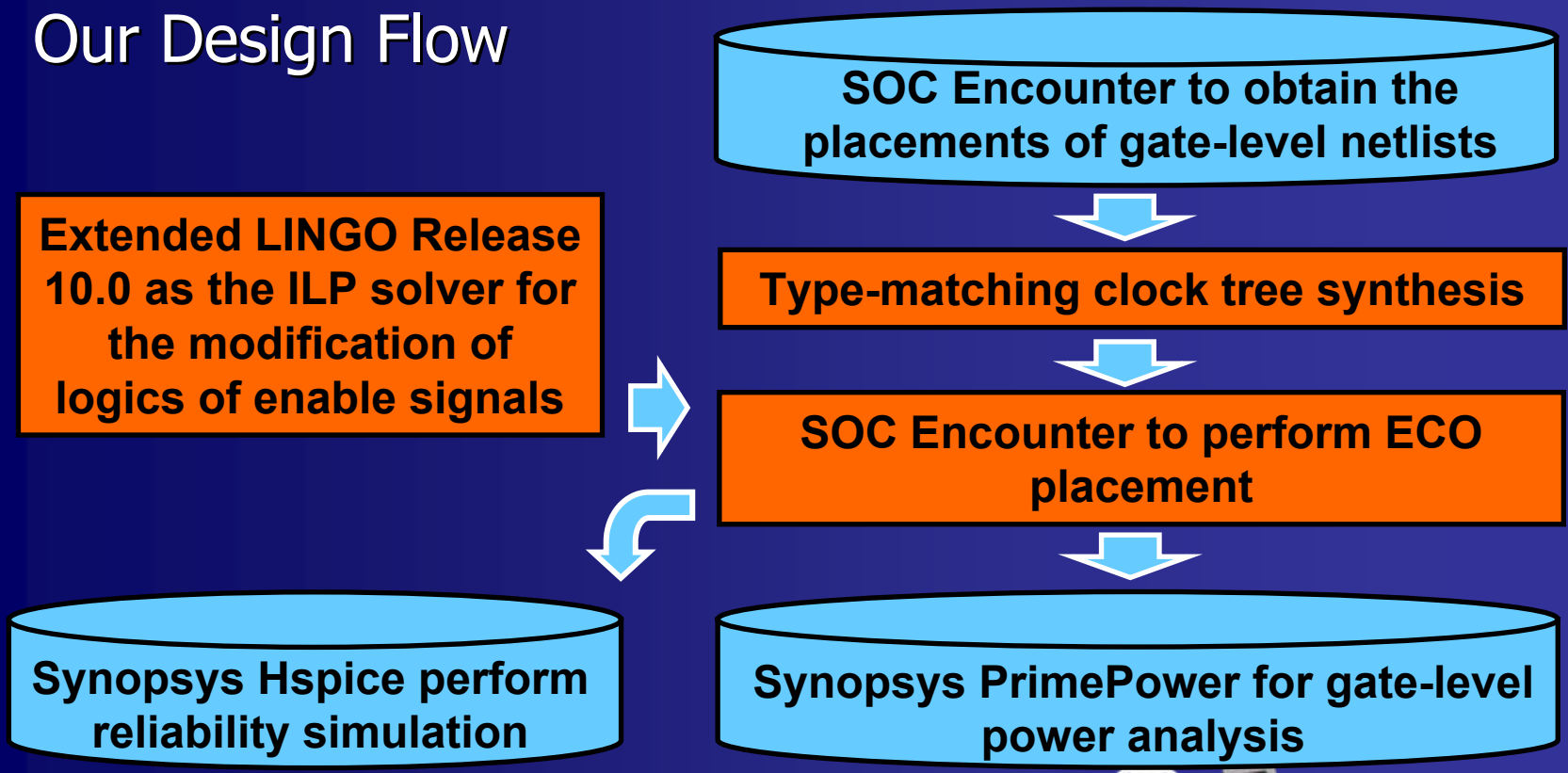
Experimental Results - Design Flow

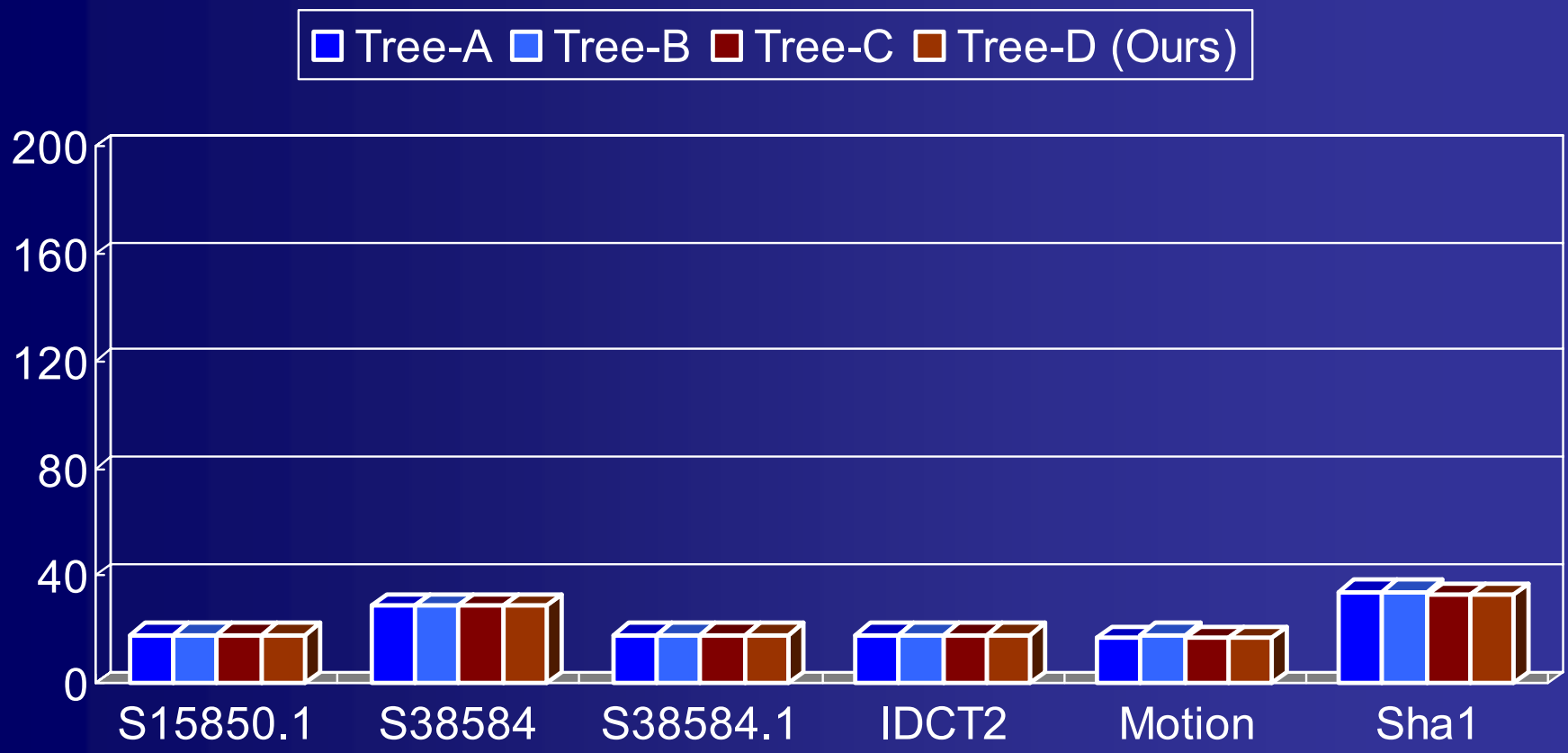
- We use six benchmark circuits, which are targeted to TSMC 0.13 μm process technology, to test the effectiveness of our design methodology.
- Our Design Flow



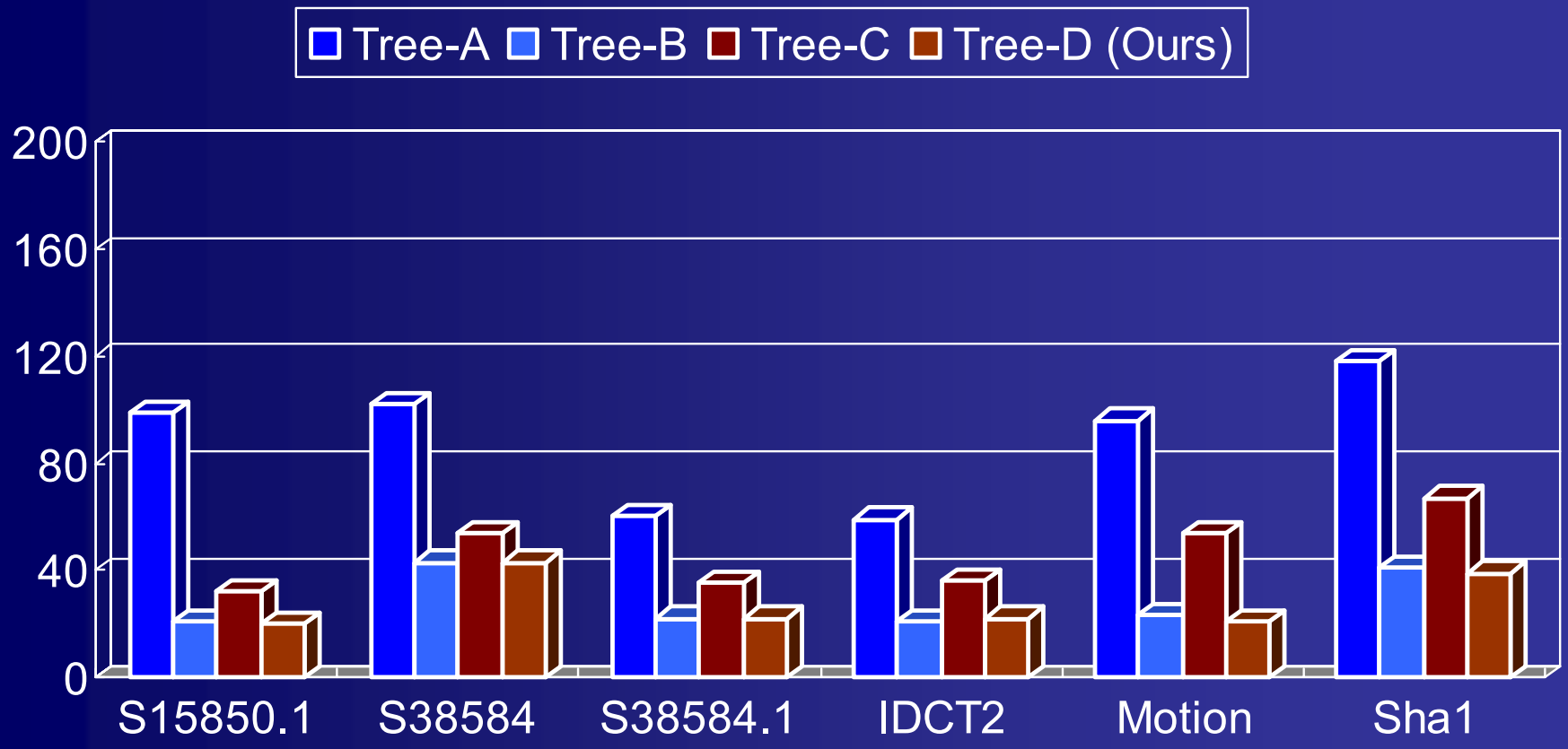
Experimental Results - Comparisons

- We derive the following four clock trees for comparisons.
  - Tree-A
    - The AND-type-matching clock tree.
  - Tree-B
    - The anti-aging AND-type-matching clock tree. Note that this clock tree is the anti-aging version of Tree-A.
  - Tree-C
    - The NAND-type-matching clock tree.
  - Tree-D (our clock tree)
    - This clock tree is the anti-aging version of Tree-C.

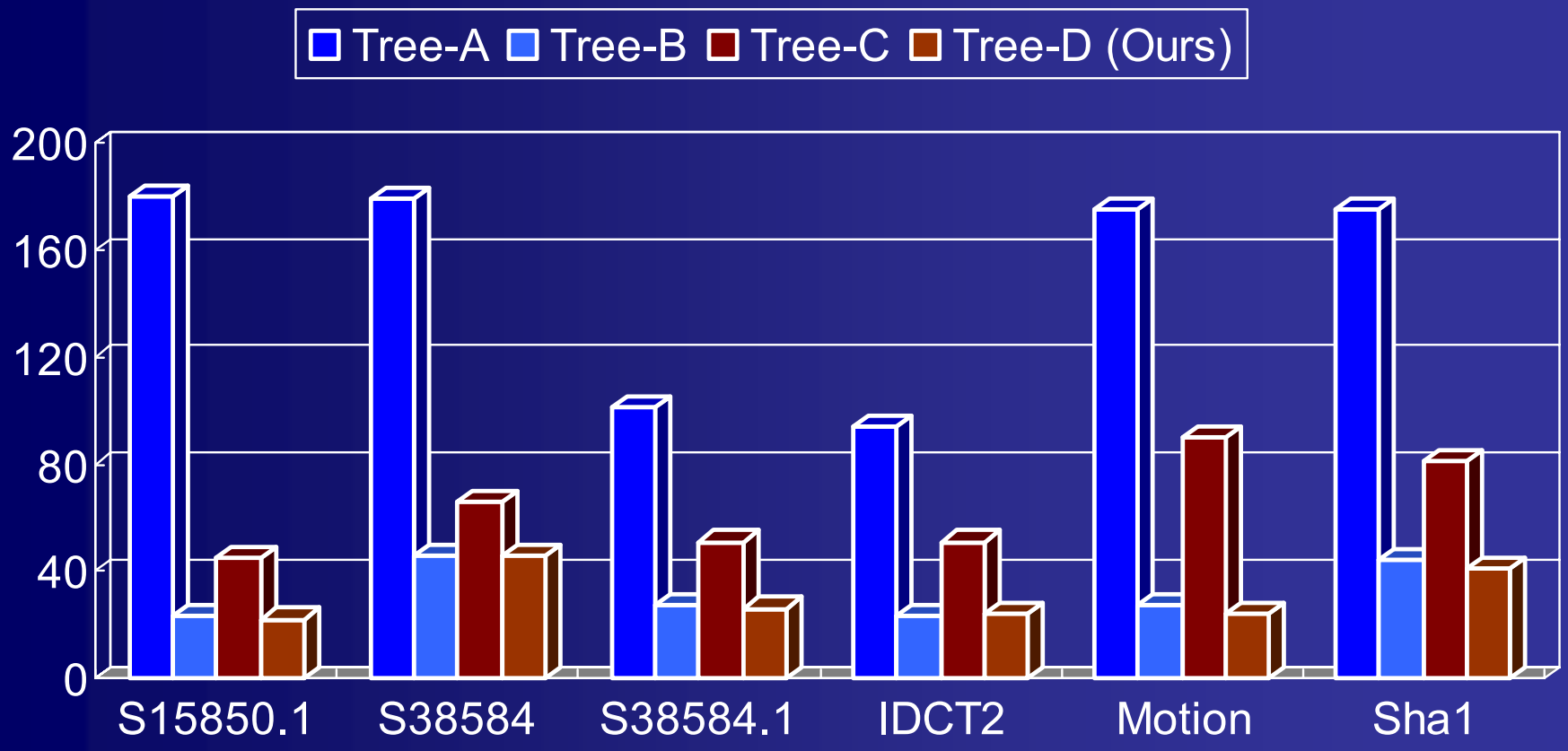

Experimental Results – Original Clock Skew



Experimental Results – Five-Year Clock Skew

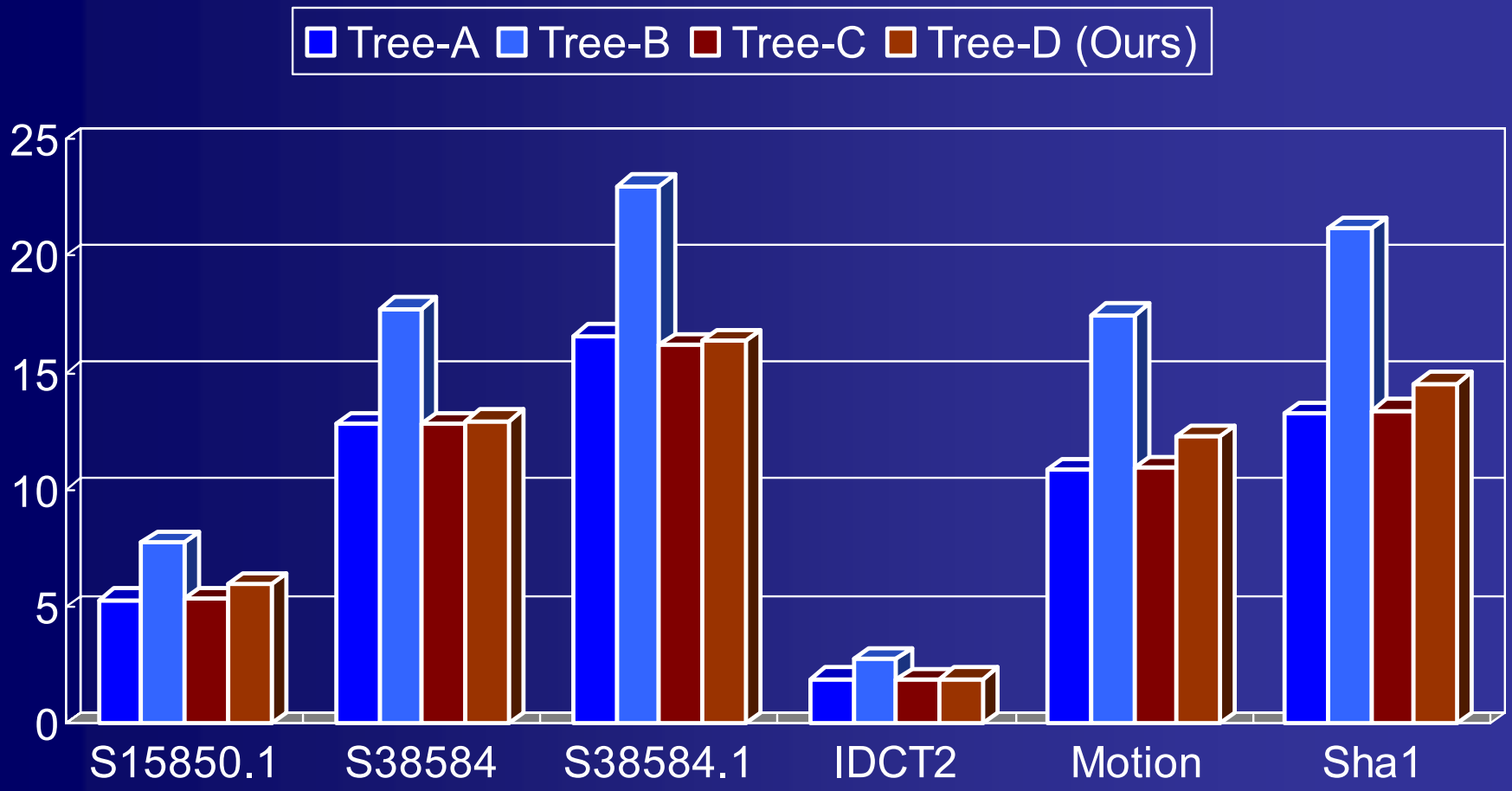


Experimental Results – Ten-Year Clock Skew



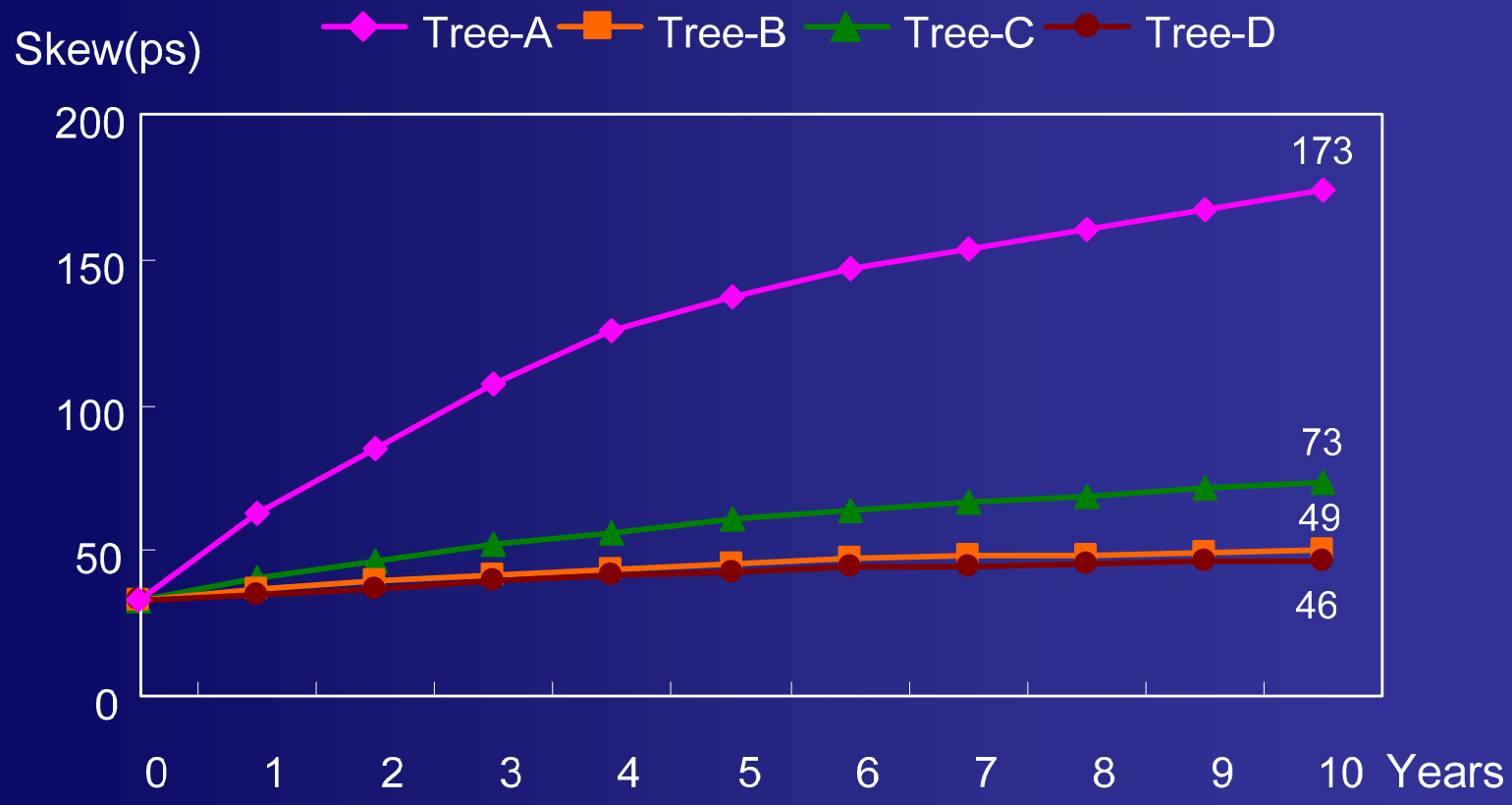
Experimental Results – Power Consumptions

- Power Consumptions of four type trees (μ w).



Experimental Results – Analysis to Circuit S35932

- The slopes of Tree-B and Tree-D are small, while the slopes of Tree-A and Tree-C are large.



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Conclusions

- We present the first attempt for ensuring that the clock skew is always zero during the circuit life.
- Our critical-PMOS-aware clock tree design methodology includes two main aspects.
  - We prove that the number of "must-levels" of NAND-type-matching clock tree is the lower bound that any clock tree can achieve.
  - We propose a 0-1 ILP approach to minimize the power consumption.
- Benchmark data consistently show that our methodology can eliminate the degradation difference with almost negligible power consumption overhead.


Thank you !