Improved Weight Assignment for Logic Switching Activity During At-Speed Test Pattern Generation

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Outline

- Introduction
- Previous works
- Proposed weight assignment scheme
- Experimental results
- Conclusion

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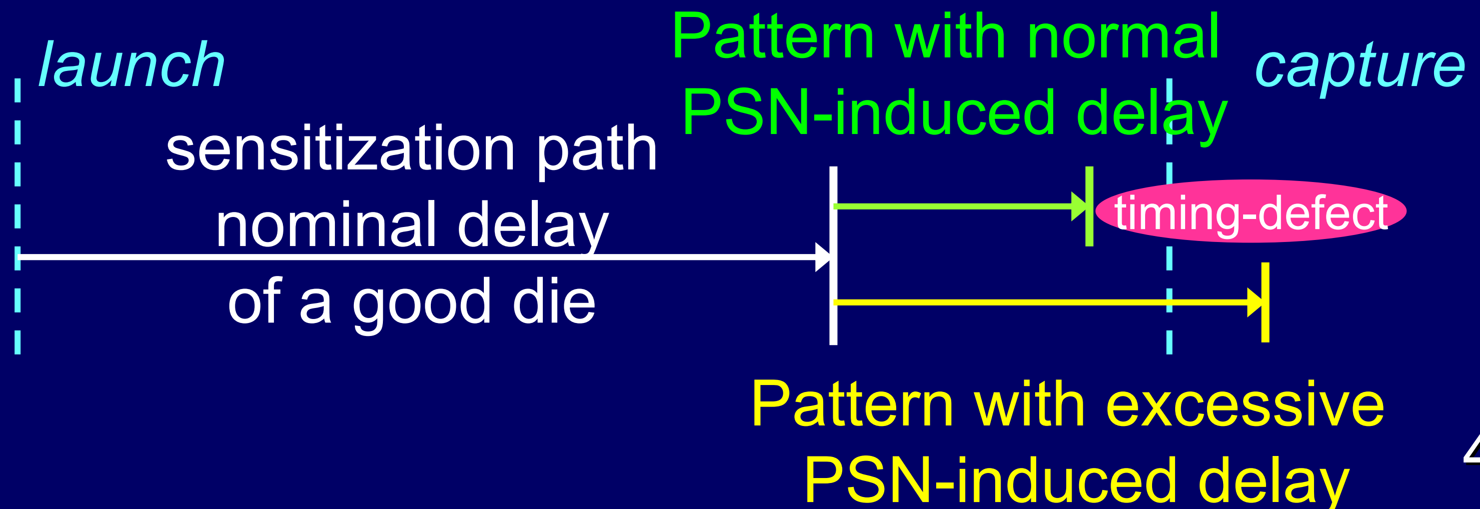
Introduction

- Excessive power supply noise (PSN) in a test pattern's launch cycle may cause a timing-defect-free chip to fail the test
  - Excessive IR-drop → extra gate delay → timing failure → yield loss



Previous supply noise/IR-drop estimation method

- WSA (Weighted Switching Activity) model is commonly used in test pattern generation applications

- WSA (of a circuit) is defined as following

$$WSA = \sum G_i \cdot W_i$$

If Gate i has switching, G_i=1 else G_i=0

W_i = (fanout count of Gate i)+1

→Fast computation time is a necessity in pattern generation applications

Advantage and disadvantage of WSA model

- Advantage
  - Very fast, suitable for test pattern generation application

- Disadvantage
  - Doesn’t correlate well to commercial IR-drop simulator
    - correlation < 0.5
  - No local IR-drop information; hard to guide ATPG to reduce the local IR-drop problem

Contribution

- An improved weight assignment scheme for logic switching events
- Three features
  1. Compute relative IR-drop severity of every gate
  2. Return whole-chip IR-drop severity profile
  3. Better correlation with commercial IR-drop simulators

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Previous works

- Some recent methods also proposed to improve WSA model
  - V. R. Devanathan et al., ITC07
  - N. Ahmed et al., DAC07
  - X. Wen et al., ETS08
- Their methods differ in
  - Weight assignment scheme
  - Adopted timing model
  - How they assess the regional IR-drop severity

Previous weight assignment schemes

- Weight W_i of cell i
  - (Fanout count of cell i) + 1
  - Unit weight (i.e., $W_i = 1$)
  - Loading capacitance of cell i
- In our experiments, they report similar estimation results
  - There is still space for improvement

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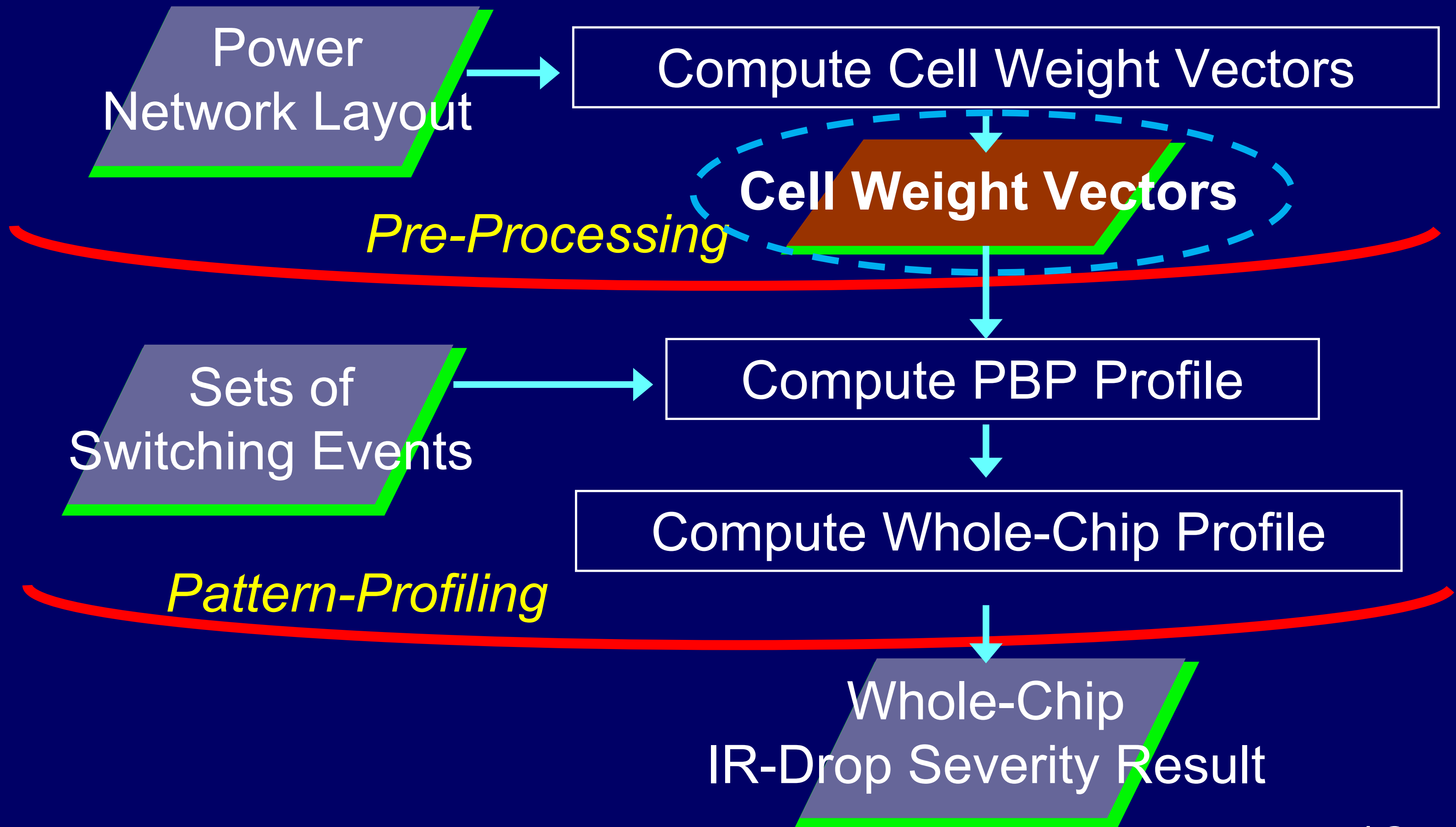
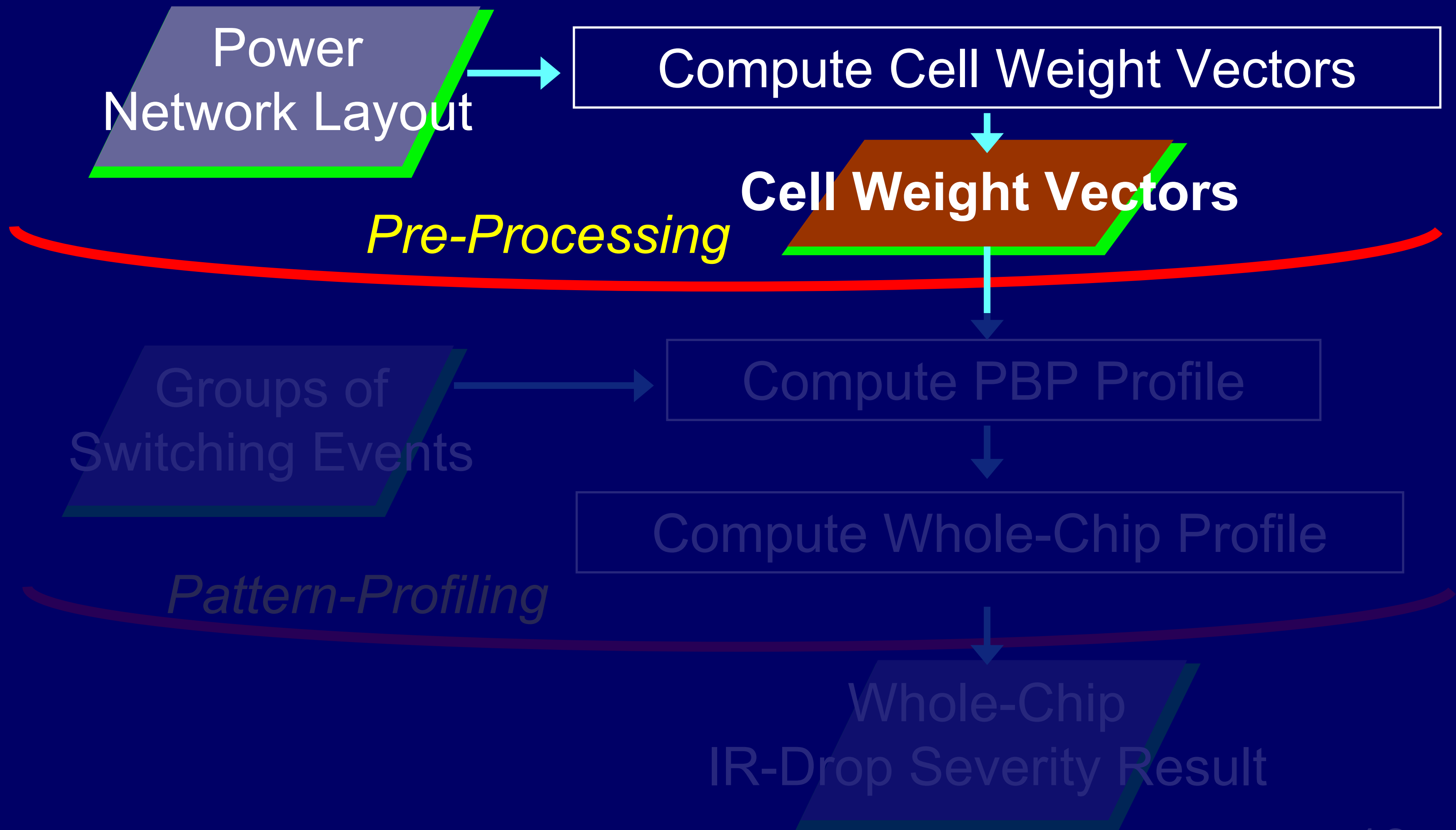
Proposed WSA computation flow

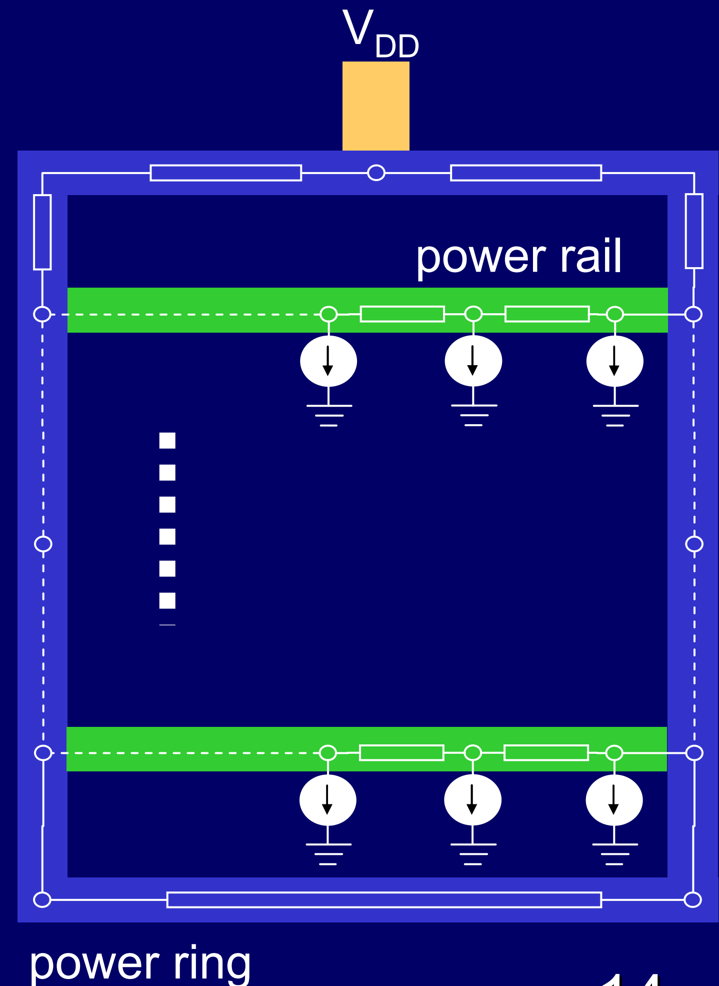


Proposed WSA computation flow



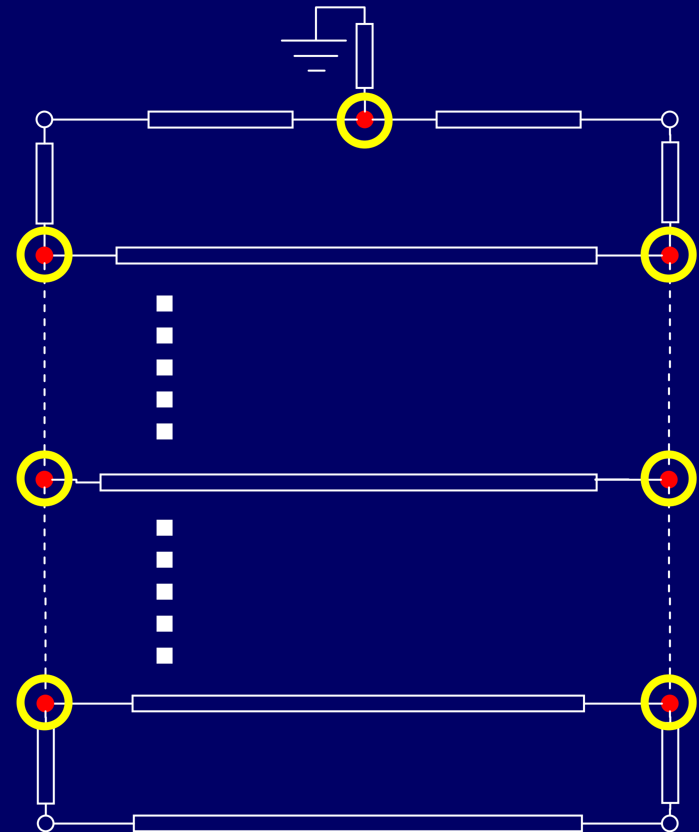
The power network model

- Perform RC extraction from GDS or LEF/DEF
  - Not just physical location
  - Currently, only consider resistance
- Model each cell as a current source



Power branch point (PBP)

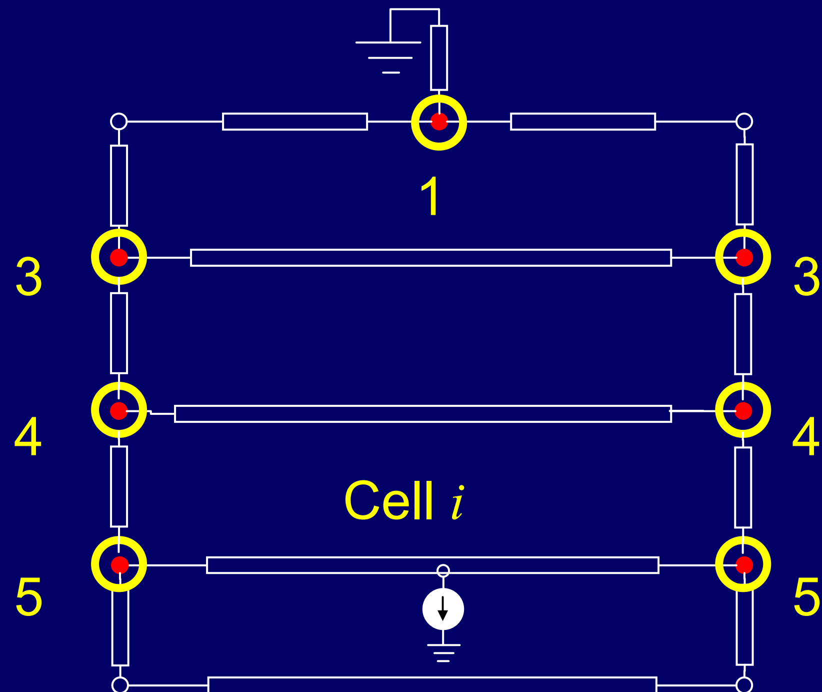
- Nodes with degree > 2
  - After removing all current sources



Weight vector (our key idea!)

- Weight vector $\mathcal{M}_i$ of cell i
  - The estimated IR-drop severity on all PBP's if only cell i switches
  - Use modified nodal analysis (MNA)
- Example 1

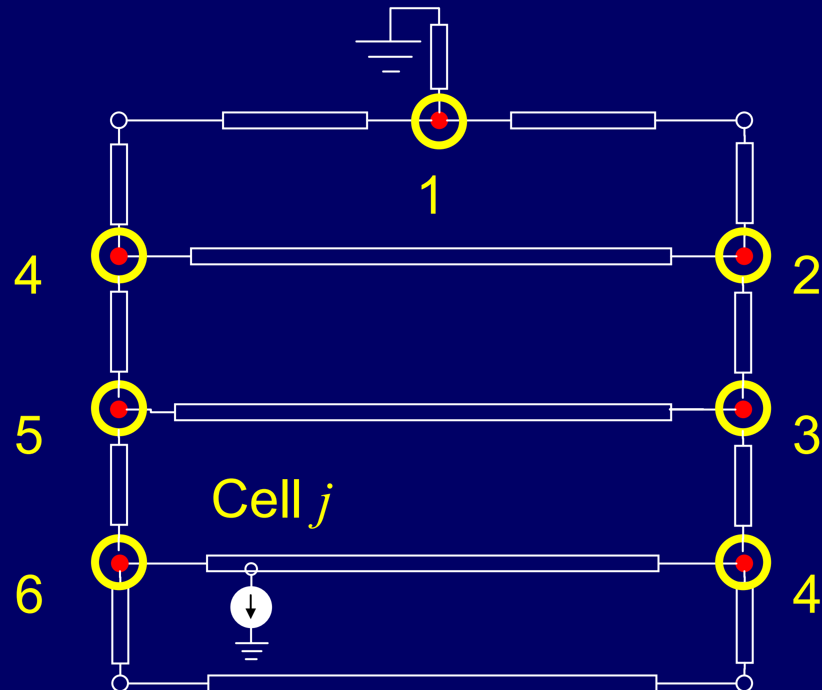
$$\mathcal{M}_i = [5,5,4,4,3,3,1]$$



Weight vector

- Weight vector $\mathcal{M}_i$ of cell i
  - The estimated IR-drop severity on all PBP's if only cell i switches
  - Use modified nodal analysis (MNA)
- Example 2

$$\mathcal{M}_j = [6,4,5,3,4,2,1]$$

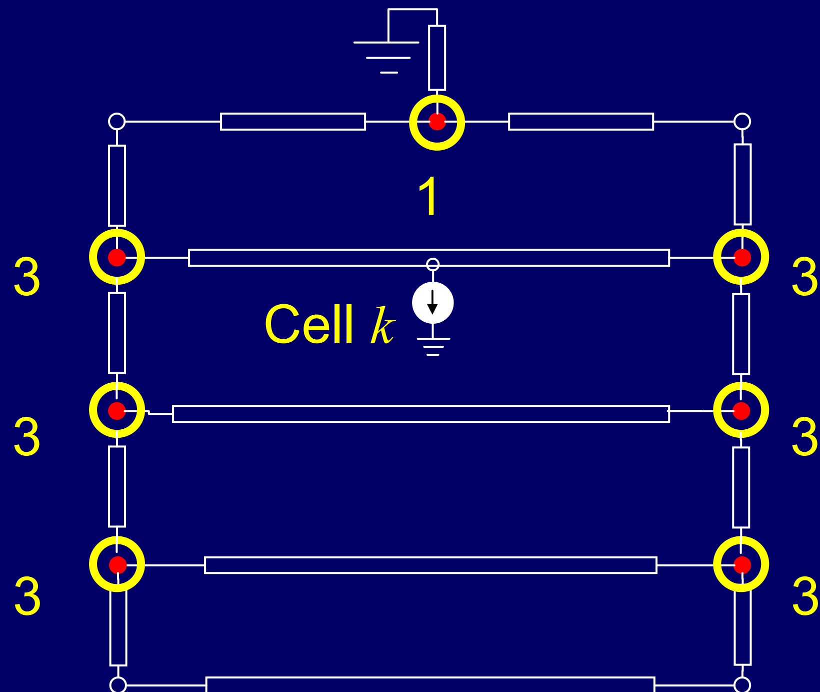


Weight vector

Power network structure and power pins' location affect IR-drop a lot

- Example 3

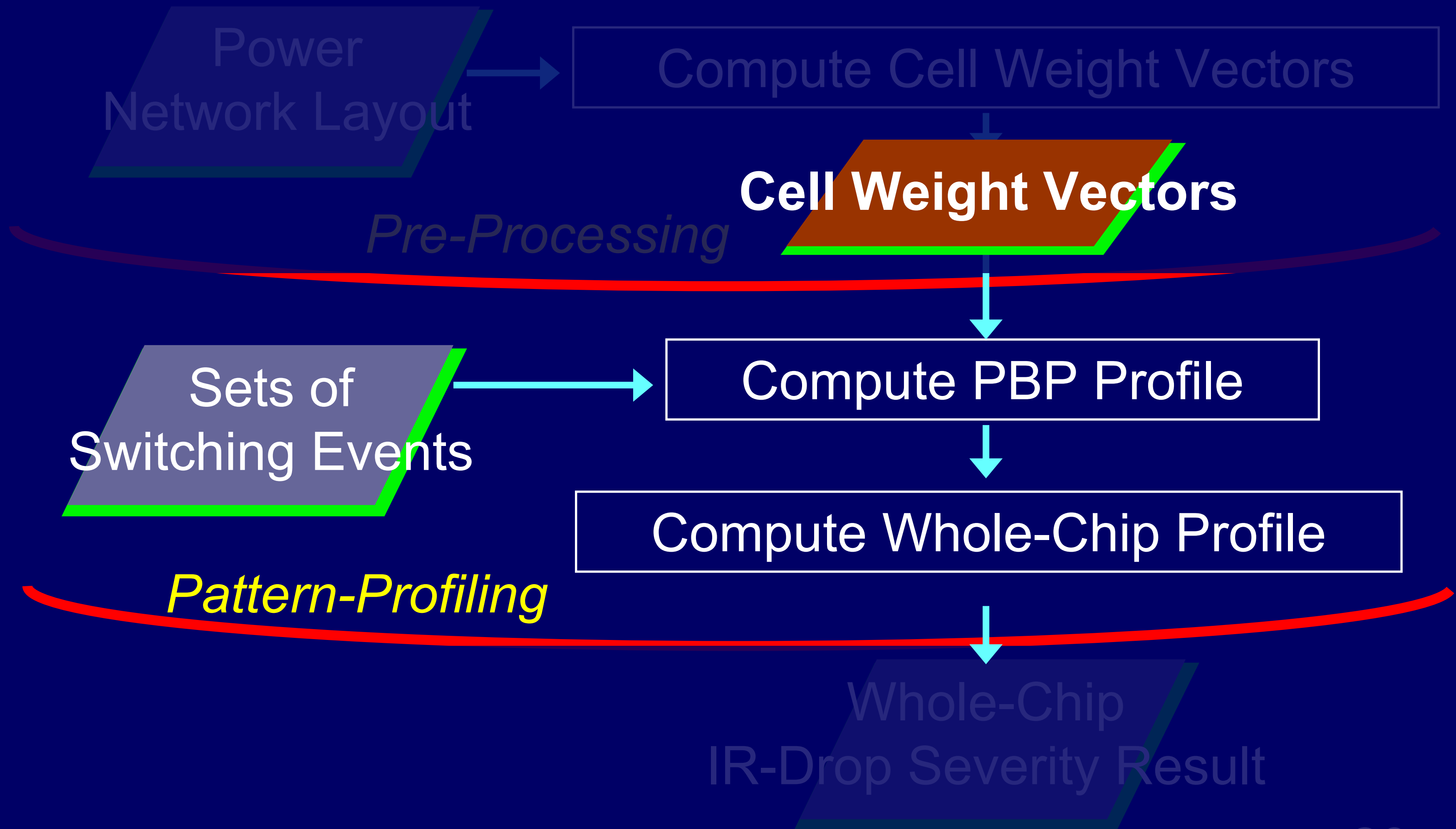
$$\mathcal{M}_k = [3,3,3,3,3,3,1]$$



Summary: weight assignment schemes comparison

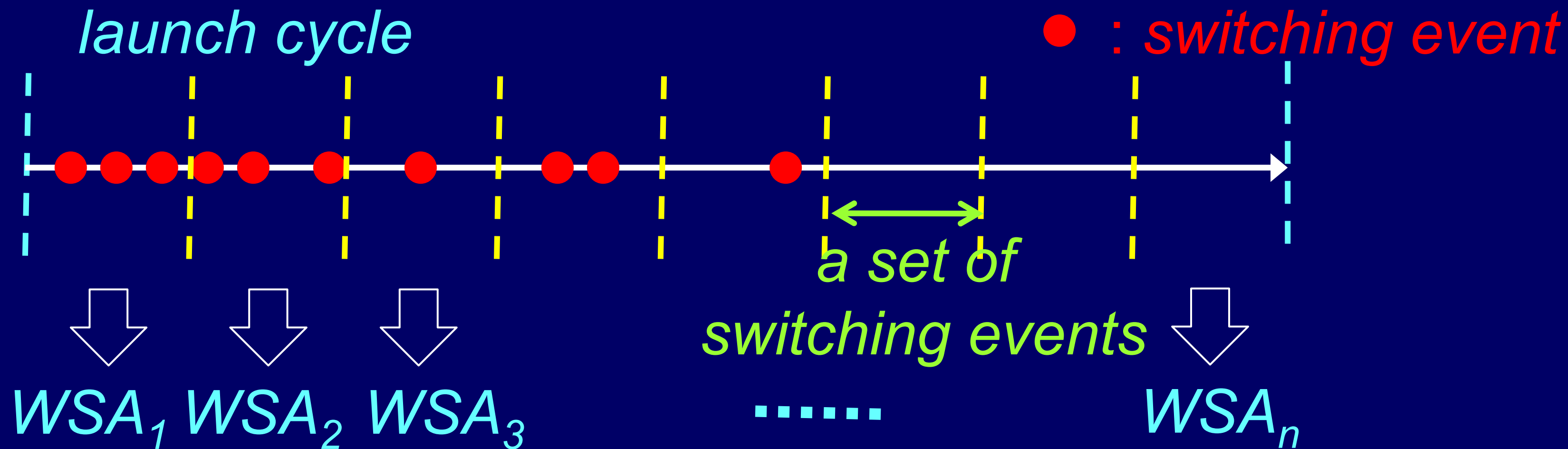
	Previous schemes	**Proposed scheme**
Name	Weight W_i	Weight vector $\mathcal{M}_i$
Storage for weight	O(1)	O(# of PBP's)
Aware of extracted structure?	Not aware	Aware
Aware of VDD's location?	Not aware	Aware
Pre-computable?	Yes	Yes

Proposed WSA computation flow



Sets of switching events

- Divide a clock cycle into several segments
- Compute the WSA of each segment/set
  - Utilize timed logic simulator



Global WSA^{T+}=Max(WSA_1, WSA_2, …, WSA_n)

Compute PBP profile

- Use superposition to estimate the IR-drop on all PBP's w. r. t. a set of switching cells
  - Linear time complexity w.r.t. the number of PBP's

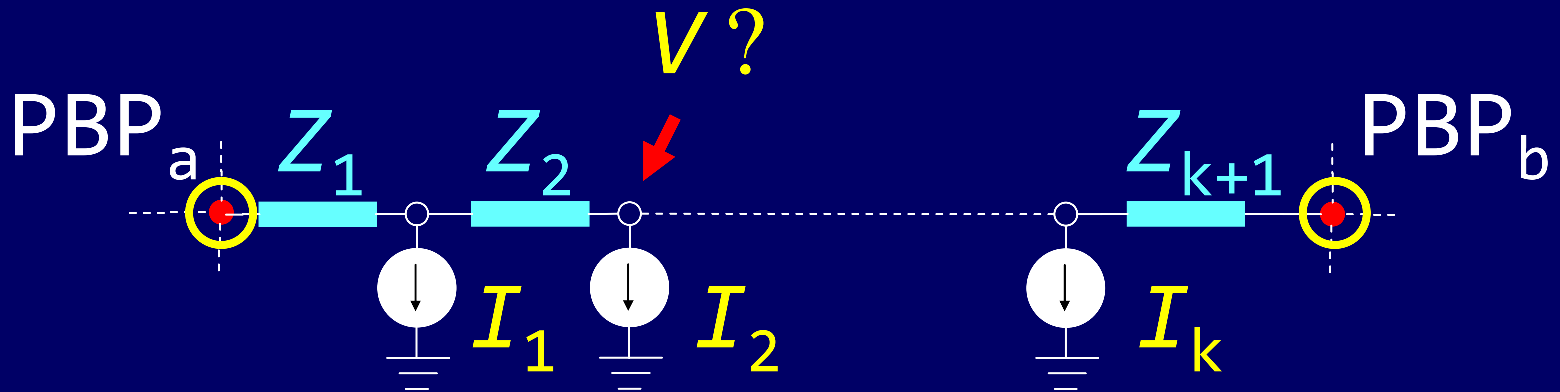
- Example:
  - Three switching cells with weight vectors as

$$\mathcal{M}_{cell_A} = [5,5,4,4,3,3,1]$$
$$\mathcal{M}_{cell_B} = [6,4,5,3,4,2,1]$$
$$\mathcal{M}_{cell_C} = [3,3,3,3,3,3,1]$$

→ resulting PBP profile = [14,12,12,10,10,8,3]

Compute whole-chip profile

- Compute IR-drop severity of inner nodes between any two PBP's
  - MNA can still be used
  - Linear time complexity w.r.t. number of nodes



Proposed WSA computation flow

this model is named as WSA^{WT+}

- Weight improved
- Timing improved

ompute Cell Weight Vectors

Cell Weight Vectors

Compute PBP Profile

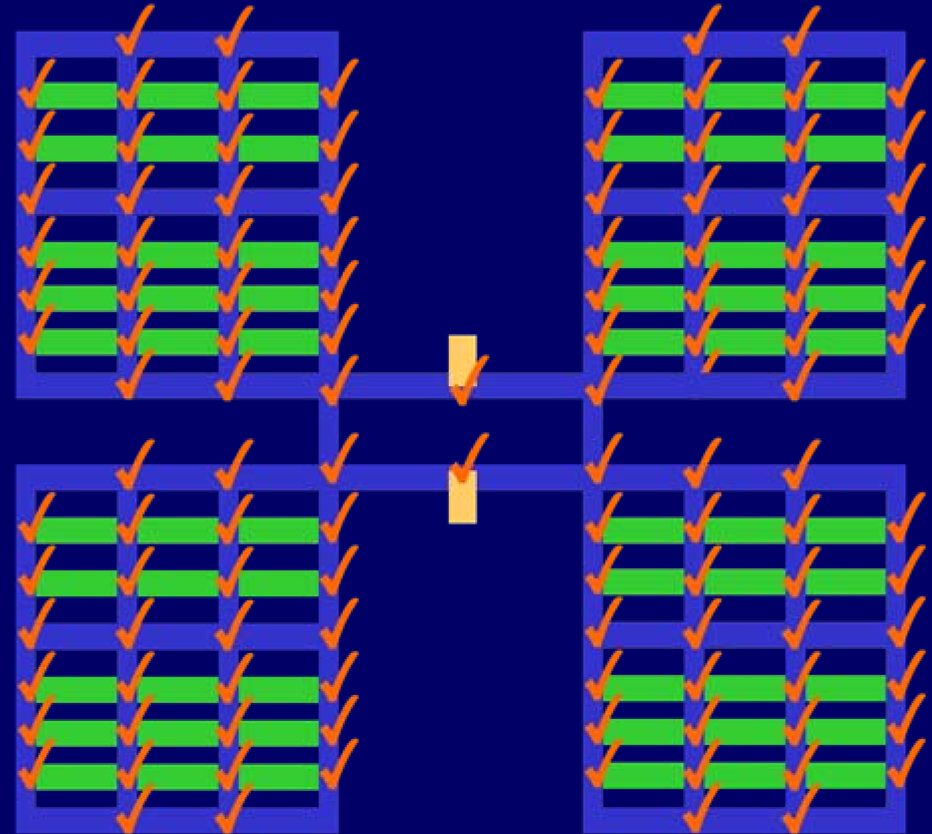
Compute Whole-Chip Profile

Pattern-Profiling

Whole-Chip
IR-Drop Severity Result

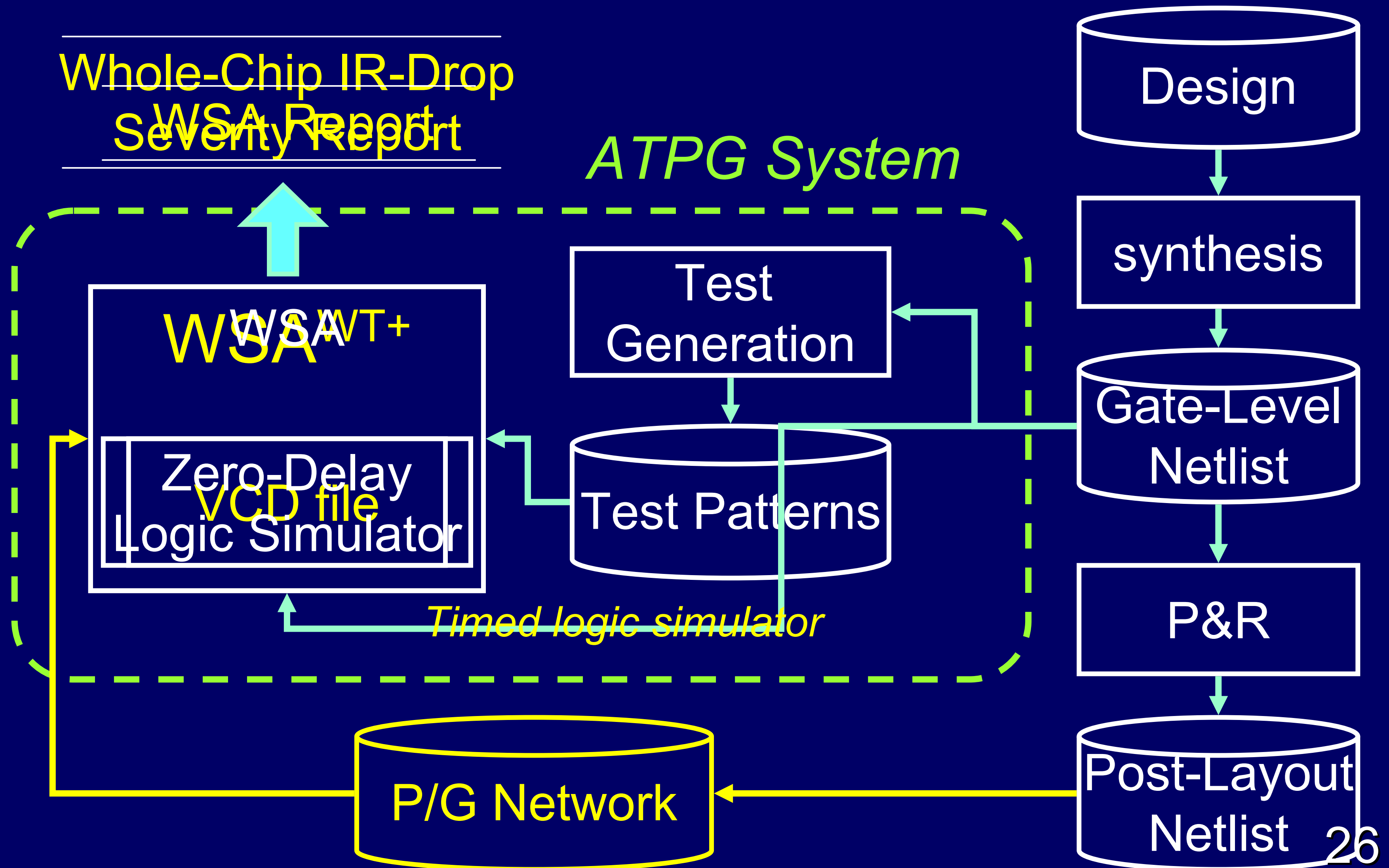
Applicability to other power grid configurations

- Applicable to real cases with very complex and irregular power grid structure



✓ : PBP

Link with existing design flow



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Experimental Setup

- Row-based standard cell design
- Single V_{DD}/V_{SS} pad is used
- Power grid structure is as shown before (no vertical/horizontal stripes)
- TSMC .13 μm cell library
- $V_{DD} = 1.08$ V
- Each standard cell is fed by a single power rail

IR-drop Correlation between WSA (fanout+1) and commercial IR-drop simulator

- Using at speed transition fault test patterns

circuit	correlation coefficient
s5378	0.5500
s13207	0.2998
s15850	0.2771
s35932	0.7462
s38417	0.3647
s38584	0.9787
Ave.	0.5361

Global Peak IR-drop correlation results of WSA^{T+} and WSA^{WT+}

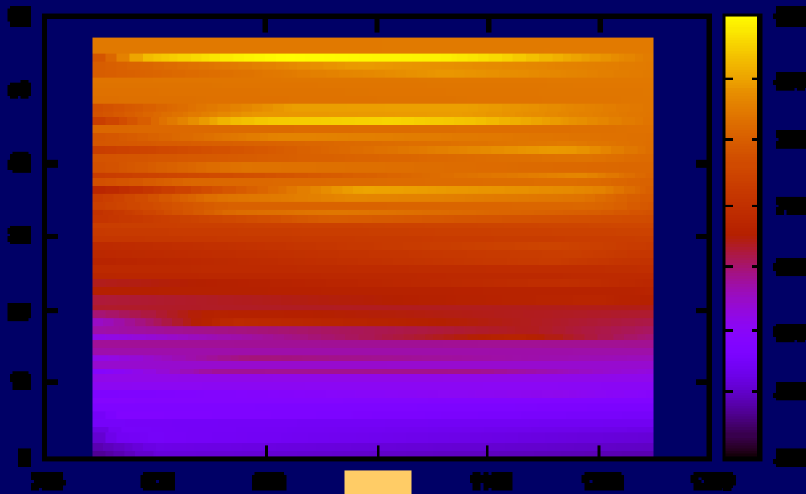
time groups: 1ns

Only our weight assignment scheme can report whole chip IR-drop profile!

				WSA^{WT+} (ours)
				0.8458
				0.8812
				0.9293
				0.8893
				0.9180
s38584	0.9476	0.9115	0.8920	0.9142
Ave.	0.8793	0.7981	0.8768	0.8963

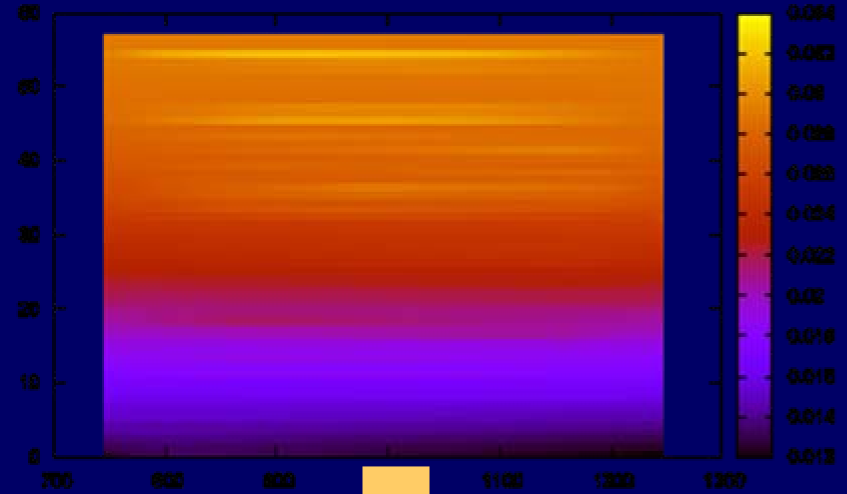
* Use the same VCD file as that in commercial tool

Whole-Chip IR-drop profile



V_{DD}

s38417, WSA^{WT+}



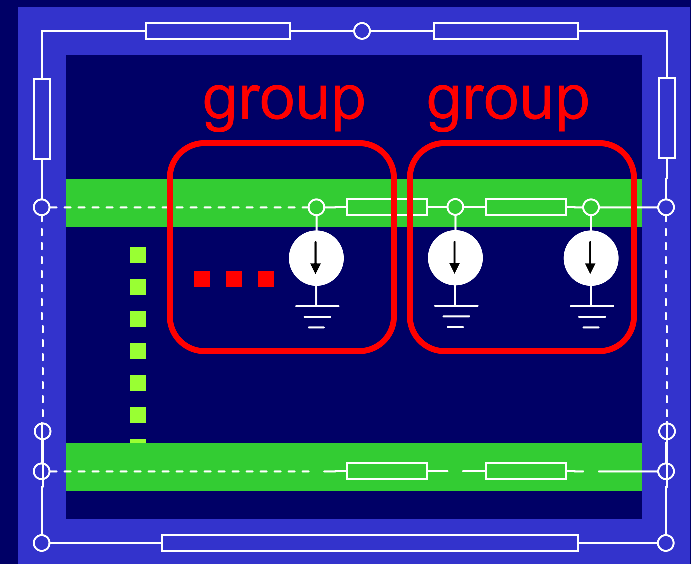
V_{DD}

s38417, commercial tool

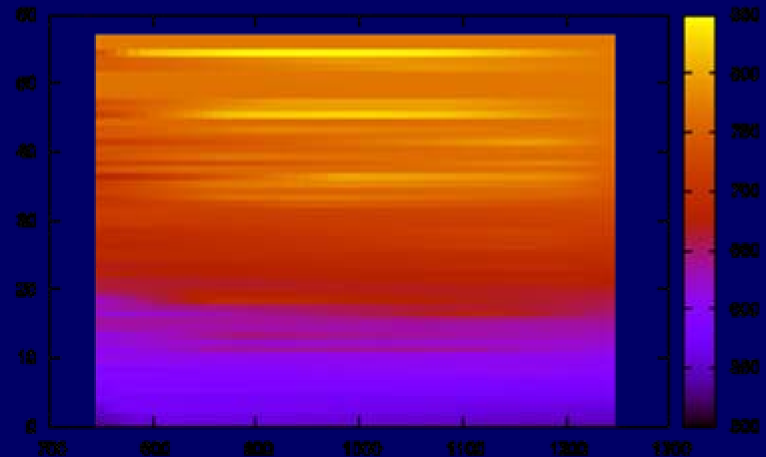
**Note: not in the same scale*

Comparison with Previous Location-Aware Techniques

- Previous techniques group gates according to their location
- Use total WSA of each group to estimate local IR-drop severity



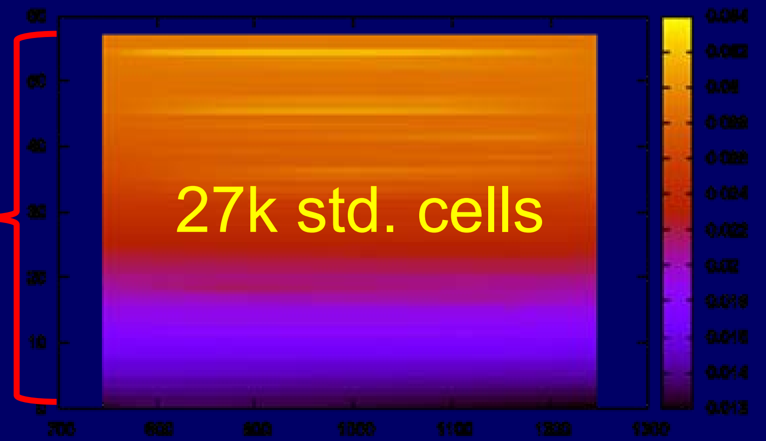
s38417, WSA^{T+}, fanout+1



s38417, WSA^{WT+}

s38417, WSA^{T+}, loading

57
rows



s38417, commercial tool

WSA^{T+} of this gate group

CPU time analysis: s38417

- Pre-processing time (once for all patterns)
  - 87 seconds
- Pattern-profiling time
  - For a test pattern (capture cycle is 20ns)
    - 60 seconds by commercial simulators
    - 0.1 second by WSA^{WT+}
    - 0.05 second by WSA^{T+}

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- A quick and high spatial resolution IR-drop severity estimator
- In the future, we will seek to integrate it into ATPG process and perform experiments on real circuit design