The 15th Asia and South Pacific Design Automation Conference ASP-DAC 2010

Emulating and Diagnosing IR-Drop by Using Dynamic SDF

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January 20, 2010

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Outline

- Introduction
- IR-Drop Analysis
- IR2Delay Database
  - Transition analysis
  - Driving strength analysis
  - IR2Delay database validation
- Diagnosis for Failure Paths
- Experimental Results
- Conclusions and Future Work

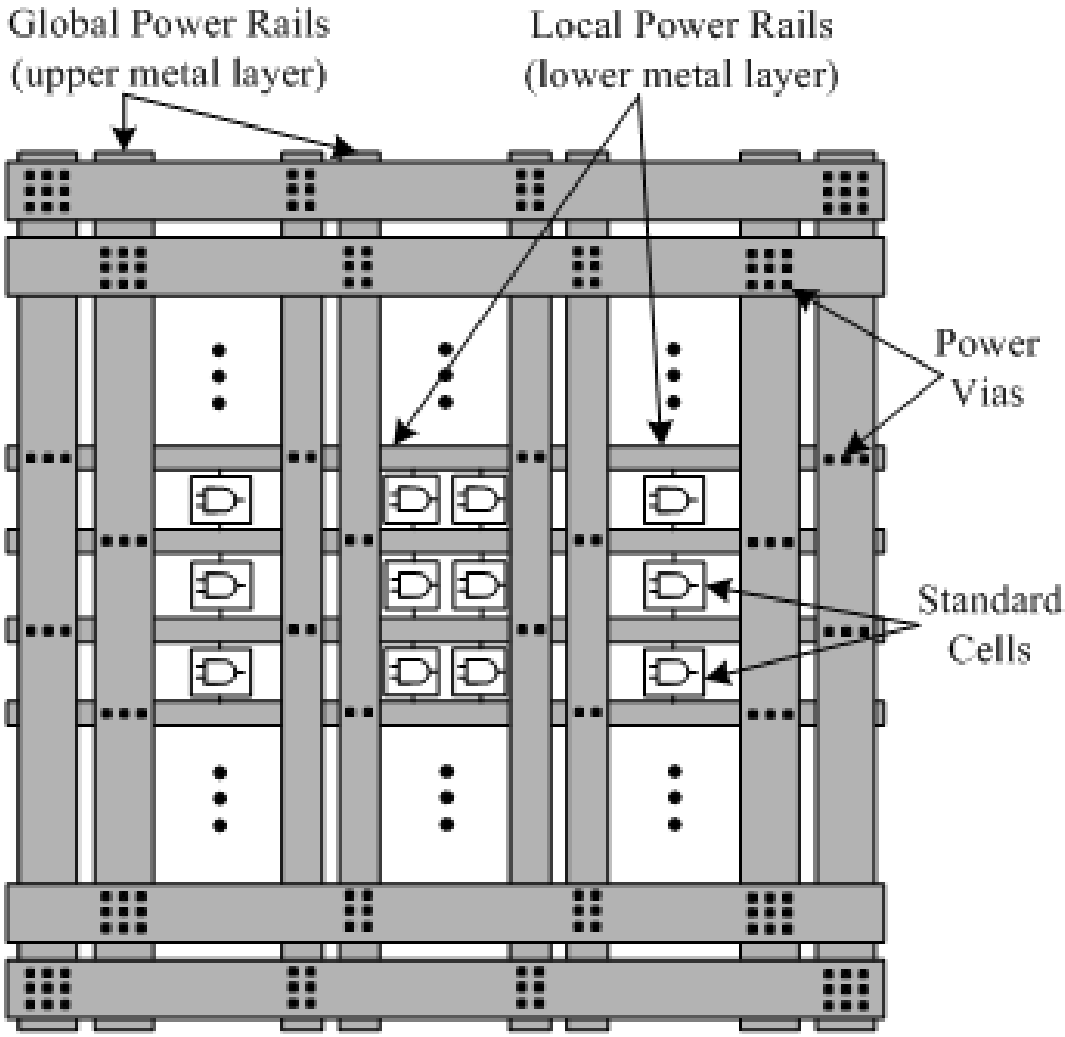
Introduction

- Timing-aware simulation is very important for model VLSI design.
- SPICE simulation
  - Accurate but slow.
  - Incapable of dealing with simulations on large designs.
- Gate-level simulation with SDF annotation
  - Fast but inaccurate.
- Static Timing Analysis tools
  - Pattern-independent.
  - Incapable of dealing with pattern-dependent effects, e.g., IR drop and crosstalk.

Introduction (Cont'd)

- The impact of IR drop and crosstalk is increasing in the latest technologies.
  - Increased transistor scaling.
  - Increased switching and power density.
  - Decreased power supply voltage.
- Pattern-dependent parasitic effects must be taken into consideration for accurate timing analysis.
- We bring IR-drop to our test / diagnosis flow.

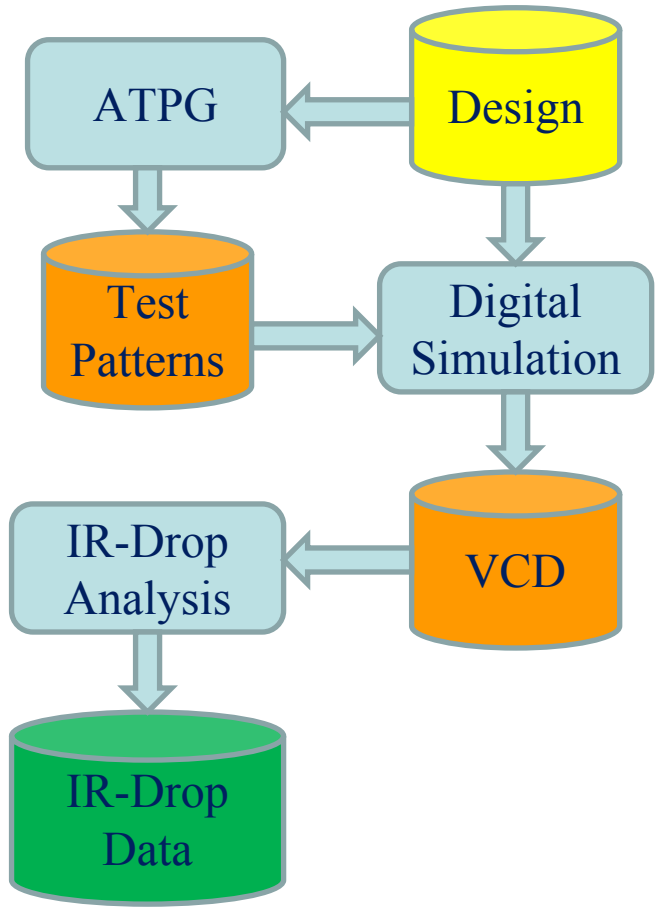
IR-Drop Analysis



A simplified view of PDN (Power Distribution Network).

IR-Drop Analysis

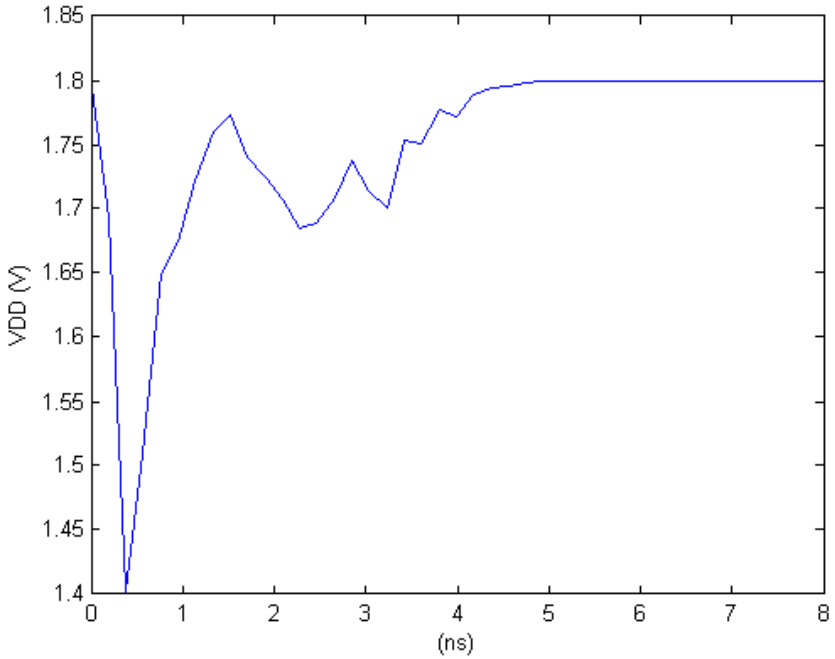
- Pattern-dependent VCD file is used for IR-drop analysis.
  - TDF (Transition Delay Fault) patterns were generated with commercial ATPG tool.
  - VCD file is Dumped by digital simulator.
  - IR-drop analysis is performed with commercial EDA tool.



IR-drop analysis flow.

IR-Drop Analysis

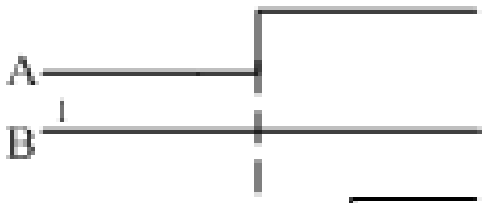
- The IR-drop on a gate is dynamic.
- Average IR-drop in a timing window is used.
  - Start at the launch clock cycle.
  - End point is chosen based on SPICE simulation.
    - Make sure the IR-drop-induced delay is close enough to real dynamic case.

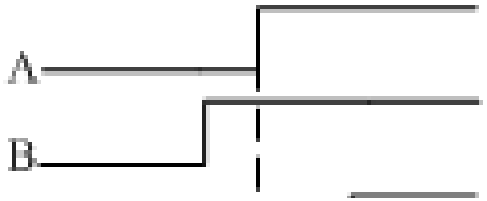


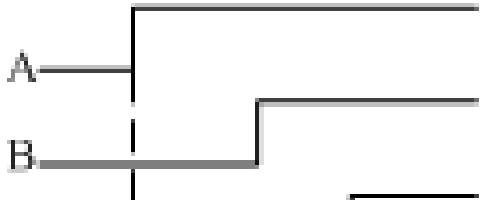
Dynamic IR-drop on a gate during the launch and capture cycles.

IR2Delay Database

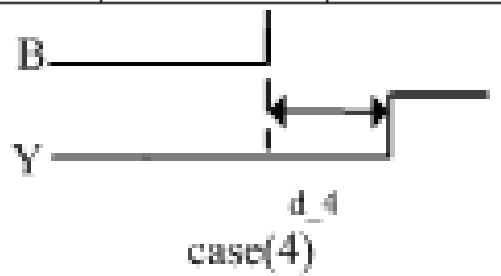
- Different input combinations may result in different gate delays.

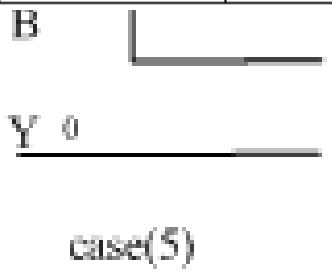


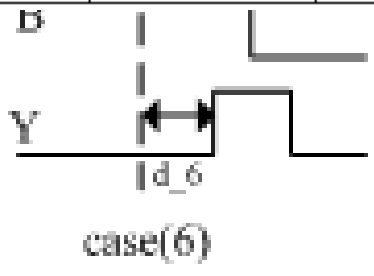


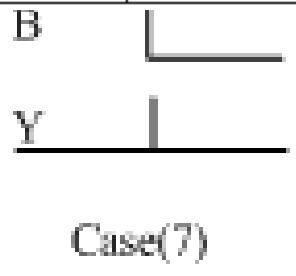


Test case	Case (1)	Case (2)	Case (3)	Case (4)	Case (5)	Case (6)	Case (7)
delay (ns)	0.1288	0.1288	2.132	0.1371	—	0.1288	—







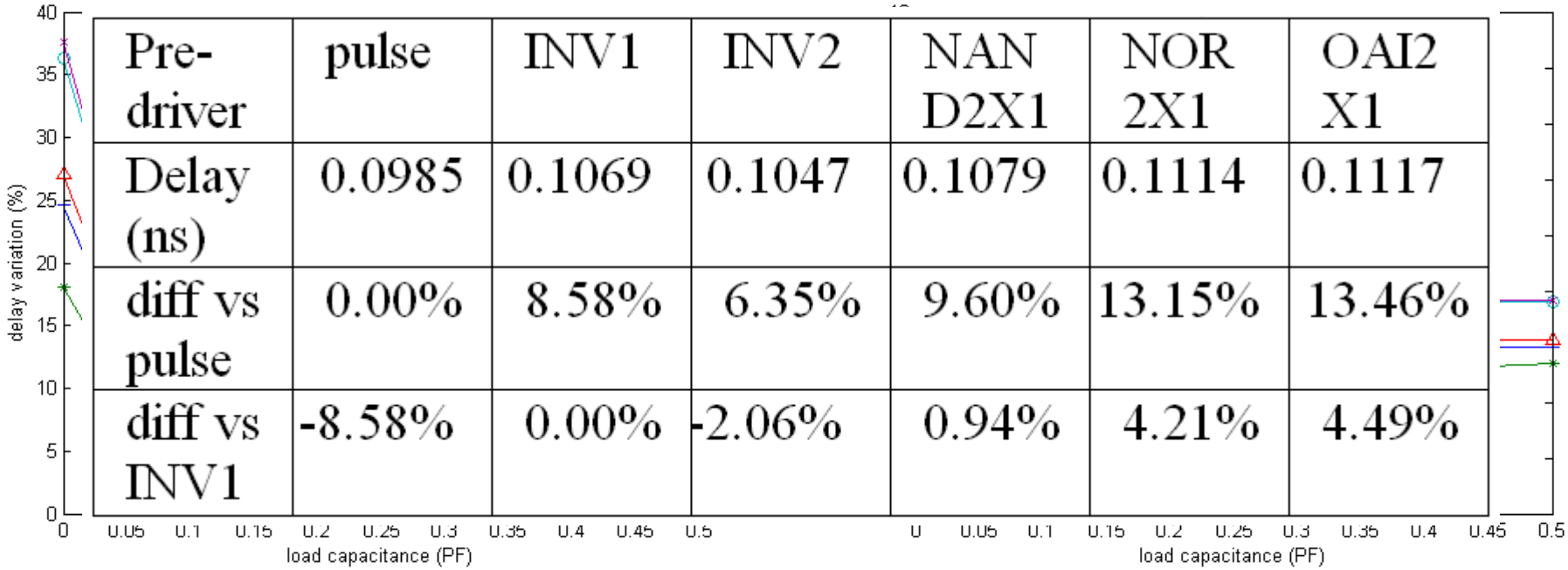


Rising-edge transition propagation of an AND2X1 gate.

IR2Delay Database

- Different driving strength (slew rate) may also result in different gate delays.

Pre-driver	pulse	INV1	INV2	NAN D2X1	NOR 2X1	OAI2 X1
Delay (ns)	0.0985	0.1069	0.1047	0.1079	0.1114	0.1117
diff vs pulse	0.00%	8.58%	6.35%	9.60%	13.15%	13.46%
diff vs INV1	-8.58%	0.00%	-2.06%	0.94%	4.21%	4.49%



(a) (b)

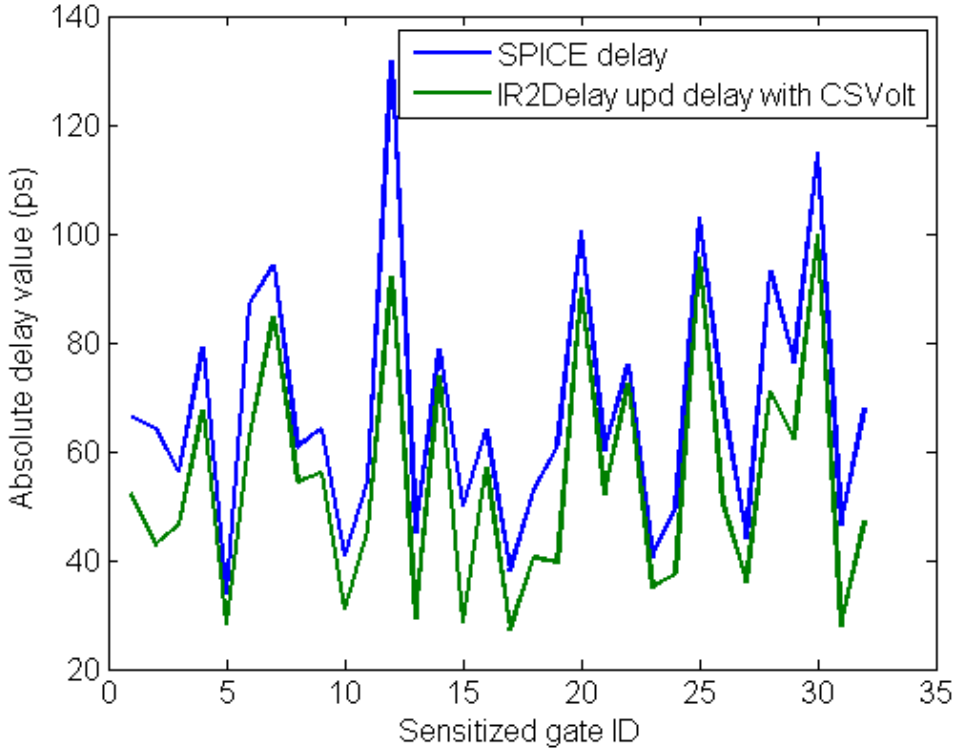
Delay variations of BUFX3 gate when driven by (a) different logic gates vs. pulse source driver and (b) different logic gates vs. INVX1 gate (Vdd: 1.8V, load cap: 0.1PF, rising-edge delay).

IR2Delay Database

- Different power voltage, load capacitance may also result in different gate delays.
- IR2Delay Database is set up based on SPICE simulation, considering
  - different propagation paths, from all input pins to the output pin.
  - different transition direction, including rising and falling transitions.
  - different power voltage.
  - different load capacitance.

IR2Delay Database

- The correlation between the full-SPICE results and our calculated results: 0.947.



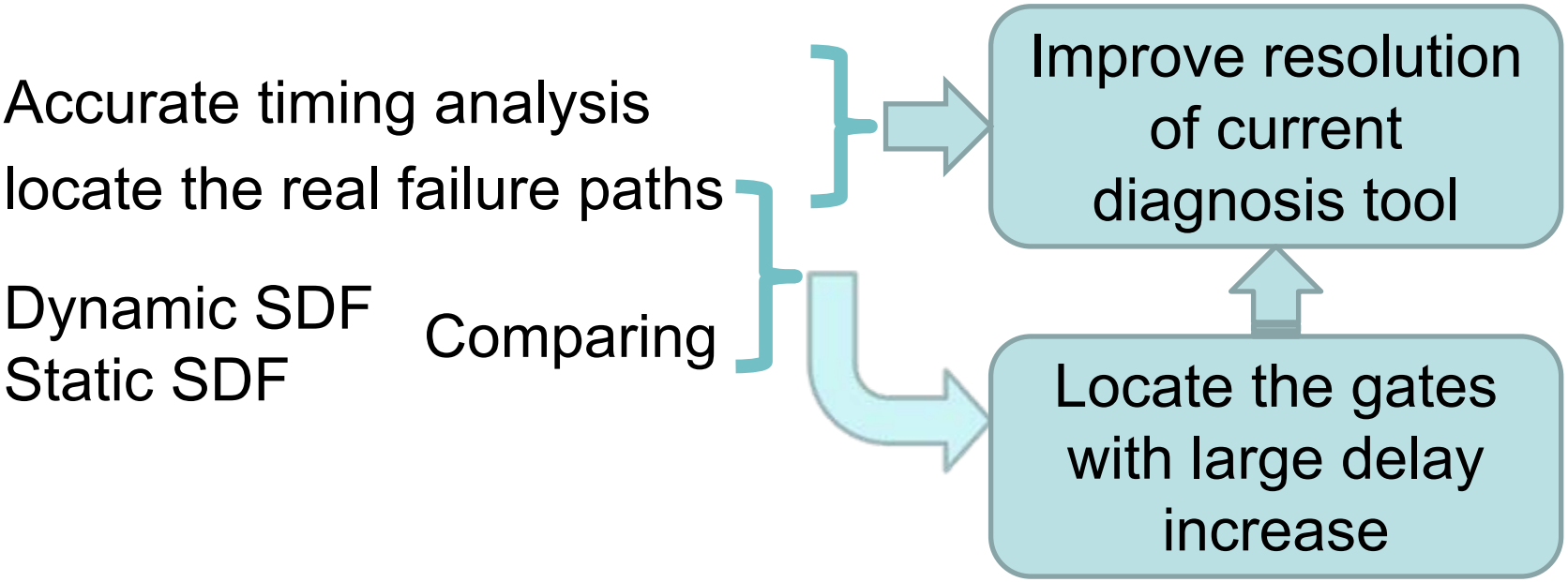
Delay comparison between ADMS results and calculated results with IR2Delay database.

Diagnosis for Failure Paths

- An controlled Experiment:
  - Select at-speed frequency and make sure no failure with the original static SDF.
  - Generate dynamic SDF with IR-drop consideration.
  - Some pattern failed due to IR-drop effect (The only reason of the failures).
- YieldAssist to report suspect failure paths
  - Check the failure bits.
  - Back trace the design.
  - Report all the suspect failure paths that may possible fail the bits.

Diagnosis for Failure Paths

- With the dynamic SDF, we can



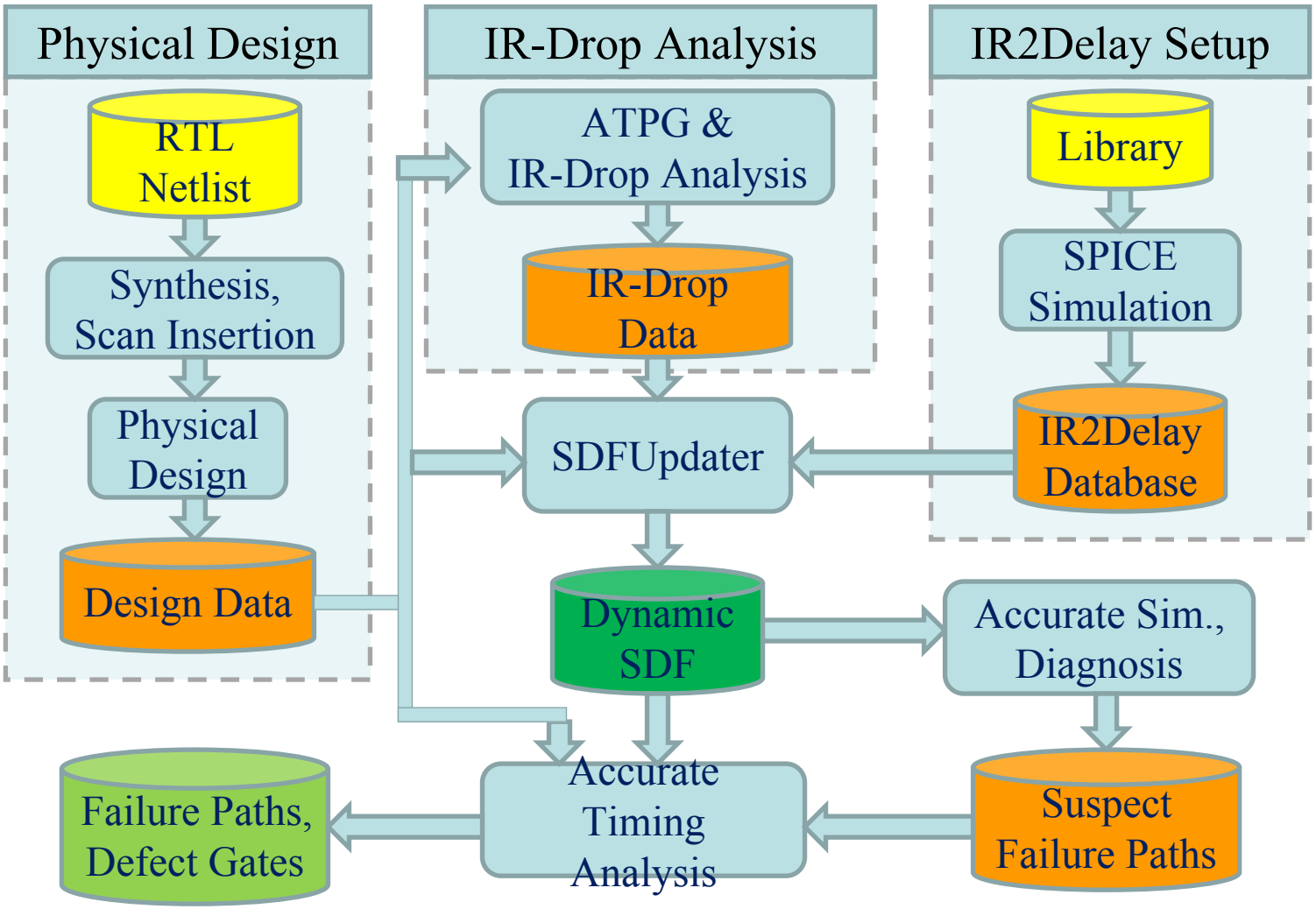
Suspect path #	1	2	3	4
Path length (ns)	7.66	7.56	3.90	3.28

The timing of suspect failure paths for a test pattern, based on IR-drop-aware dynamic SDF file (clock cycle: 7.63 ns). Can tell which path did fail the design.

Experimental Results

- Experimental benchmark: IWLS ac97_ctrl
  - contains 9,656 logic gates and 2,199 flip-flops.
- Use 180nm Cadence Generic Standard Cell Library for synthesis and physical design
  - Typical power voltage: 1.8V.
- Mentor Graphics FastScan for pattern generation
- Mentor Graphics Eldo and ModelSim for SPICE and digital simulation, respectively
- Perl, C/C++ for flow implementation

Experimental Results



The flow for injecting IR-drop effects and generating pattern-dependent SDF files.

Experimental Results

- In the dynamic SDF, the gate delay changes due to IR-drop effects.

Instance / Model		U8701 / AND2X1		U8714 / NOR2X1		U12160 / INVX1
Power volt. (V)		1.59		1.61		1.76
path		A->Y	B->Y	A->Y	B->Y	A->Y
0->1 delay (ns)	Original	0.0716	0.3208	0.0847	0.0693	0.0158
	updated	0.0845	0.3811	0.0946	0.0761	0.0166
	Incr.	18.0%	18.8%	11.7%	9.8%	5.1%
1->0 delay (ns)	Original	0.0560	0.1256	0.0957	0.0873	0.0167
	updated	0.0661	0.1492	0.1068	0.0959	0.0165
	Incr.	18.0%	18.8%	11.6%	9.8%	-1.25%

Profiles of sample gates in experimental benchmark, for a specific test pattern.

Experimental Results

- At-speed frequency is chose based on critical path delay.
  - No failures in the design with original static SDF.
- With dynamic SDF considering IR-drop effect
  - 6 over total 203 patterns are failed.
  - Can tell which gates experience severe IR-drop and larger delay increase.
  - with different guard banding frequency, the failed pattern number would change.
    - Can also be used for efficient guard banding selection against IR-drop failures during design validation.

Experimental Results

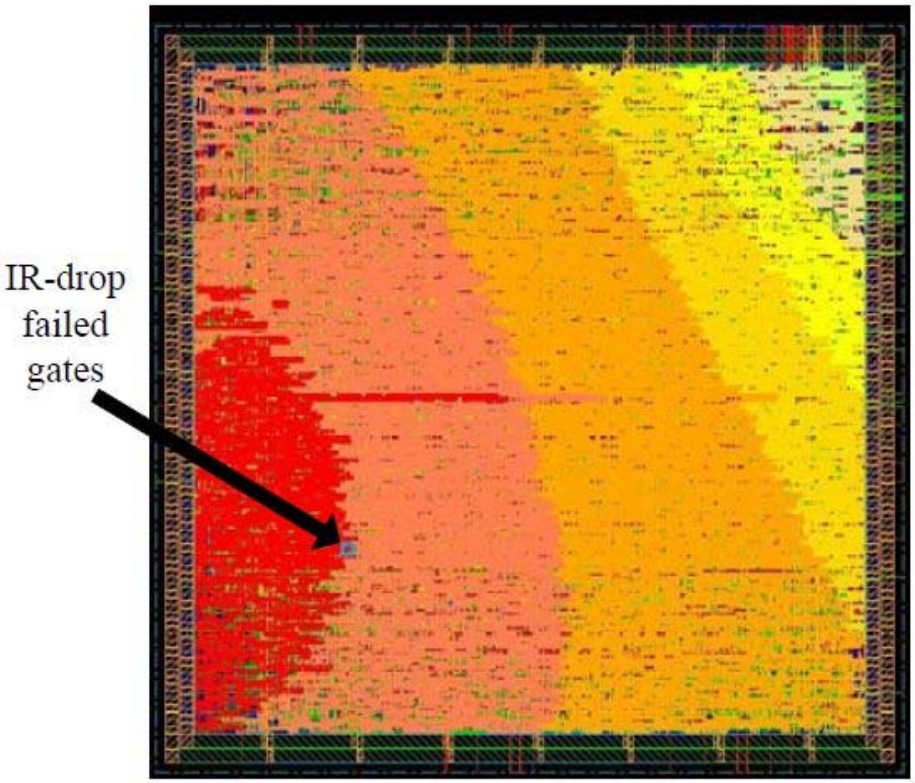
- "X": The end-point transition of the failed paths did not meet the set up time constrain of those flip-flops
- Only couple of gates in the failed paths experience severe IR-drop and large delay increase

Pattern No.	Chain No.	Pin No.	Expected	Simulated
28	17	18	1	X
28	20	22	1	X
79	20	18	0	X
115	17	22	1	X
115	20	18	0	X
167	20	18	0	X

Logs of some failed patterns.

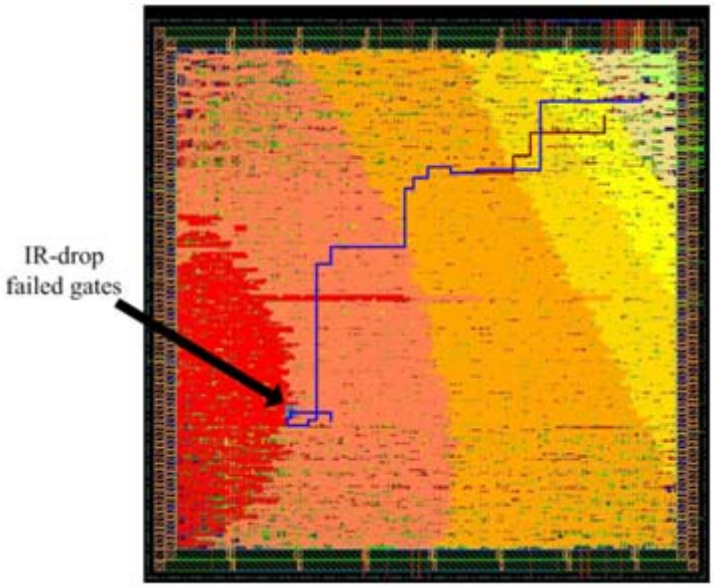
Experimental Results

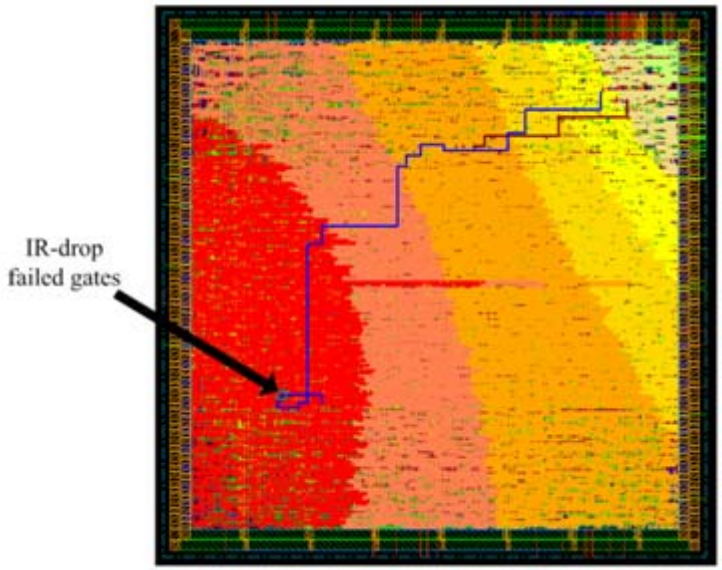
- An example of dynamic SDF application: IR-drop failure diagnosis



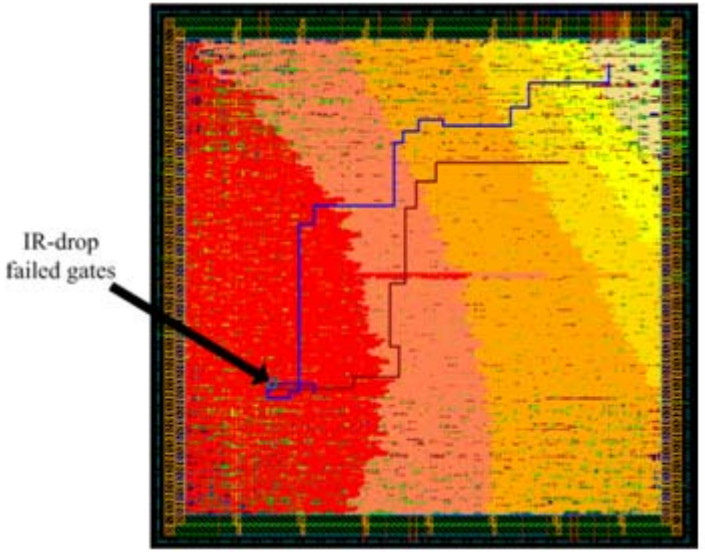
IR-drop plots and failed gates of a test pattern.

Experimental Results





- IR-drop plots and failed gates of 3 sample test patterns
  - The failure paths merged to the same failure bit.
  - The critical path (blue one) failed by all the patterns.
  - The failure gates on the critical path need to be take care.



Conclusions and Future Work

- An efficient IR-drop modeling and injection procedure was presented.
  - SPICE simulation was used for accurately map IR-drop to delay increase.
  - Dynamic SDF was generated for accurate performance evaluation and IR-drop diagnosis.
  - Procedure was validated by experimental results.
- Diagnose IR-drop failures with dynamic SDF.
- For future work
  - Bring crosstalk effects to the current flow to make it crosstalk-aware.

Thanks!