Is 3D Integration an Opportunity or Just a Hype?

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Outline

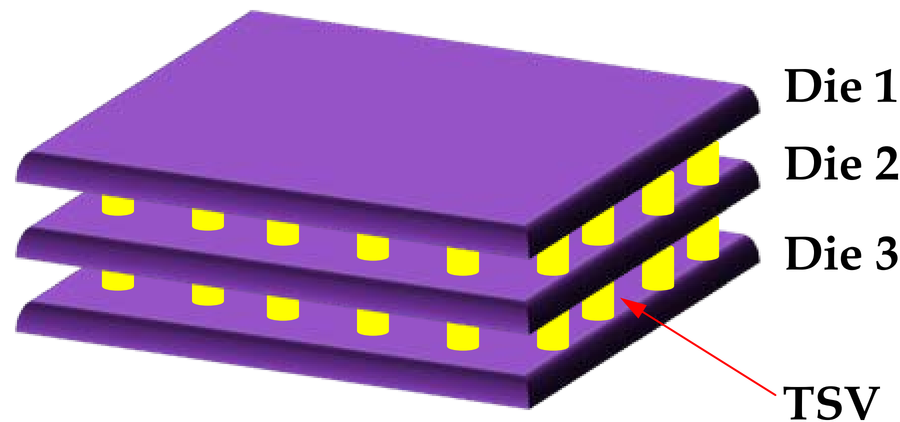
- Introduction
- 3D Integration Technology Using TSV
- Opportunities
- Challenges
- Conclusions

Introduction

- Integrating more and more transistors in a single chip to support more and more powerful functionality is a trend
  - Using 2D integration technology to implement such complex chips is more and more expensive and difficult
- Some alternative technologies attempting to cope with the bottlenecks of 2D integration technology have been proposed
- 3D integration technology using through silicon via (TSV) has been acknowledged as one of the future chip design technologies

3D Integration Technology Using TSV

- 3D integration technology using TSV
  - Multiple dies are stacked and TSV is used for the inter-die interconnection



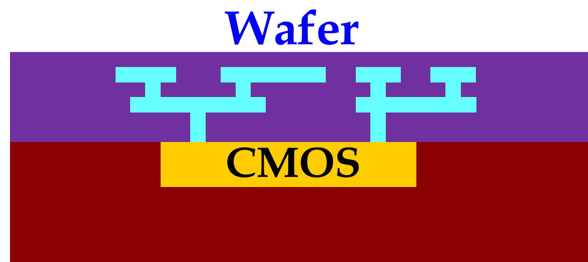
- The fabrication flow of a 3D IC
  - Die/wafer preparation
  - Die/wafer assembly

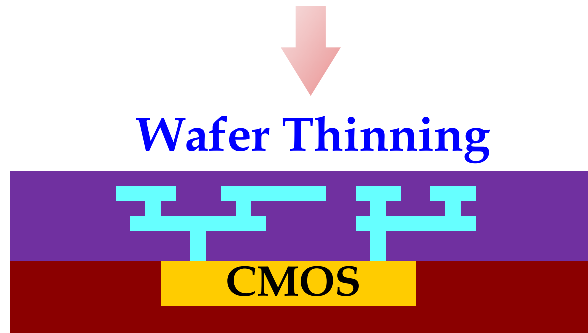
Die/Wafer Preparation

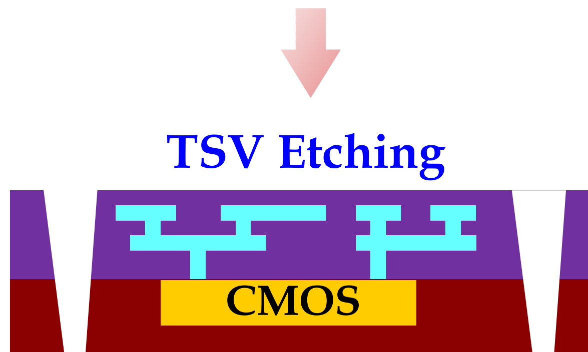
- TSV technologies
  - Via-first, via-middle, and via-last process flows
- Comparison of process flow

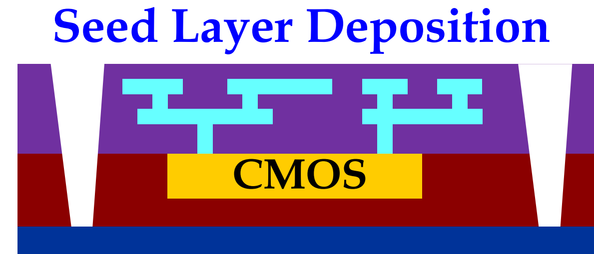
Process Step	Via-First	Via-Middle	Via-Last
TSV Drilling	Phase 1	Phase 1	Phase 3
TSV Insulation	Phase 1	Phase 1	Phase 3
TSV Metallization	Phase 1	Phase 2	Phase 3
FEOL Formation	Phase 2	Phase 2	Phase 1
BEOL Formation	Phase 2	Phase 2	Phase 1
Handler Attachment	Phase 3	Phase 3	Phase 2
Wafer Thinning	Phase 3	Phase 3	Phase 2
Backside Process	Phase 4	Phase 4	Phase 3

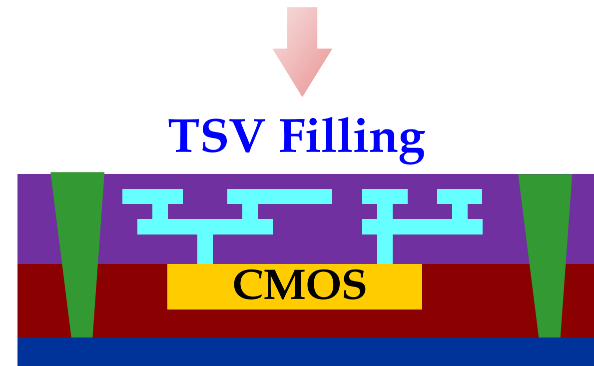
An Exemplary Via-Last Process

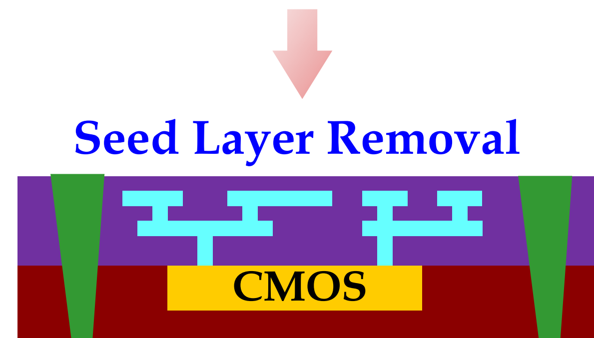








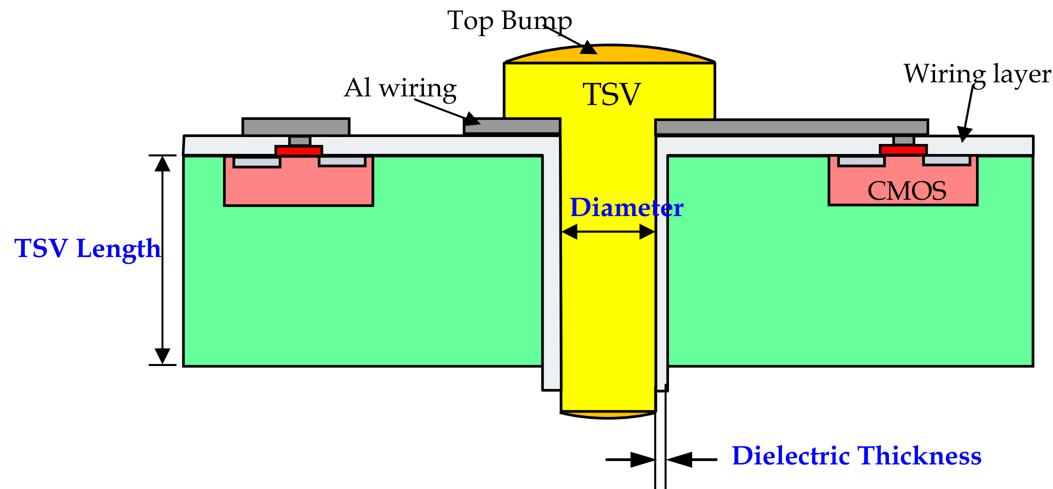




Source: V. F. Pavlidis and E. G. Friedman, "Three-dimensional integrated circuits".

Electrical Characteristics of a TSV

- Capacitance of TSV

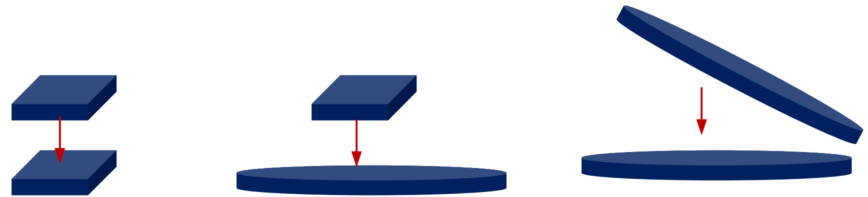


TSV Dia [um]	TSV Diel Thk [nm]	TSV Length [um]	Cap [fF]
5	50	20	239.5
5	100	20	135.2
10	50	20	496.4
10	100	20	288.3

Source: Proceedings of IEEE, pp. 101, Jan. 2009

Die/Wafer Assembly

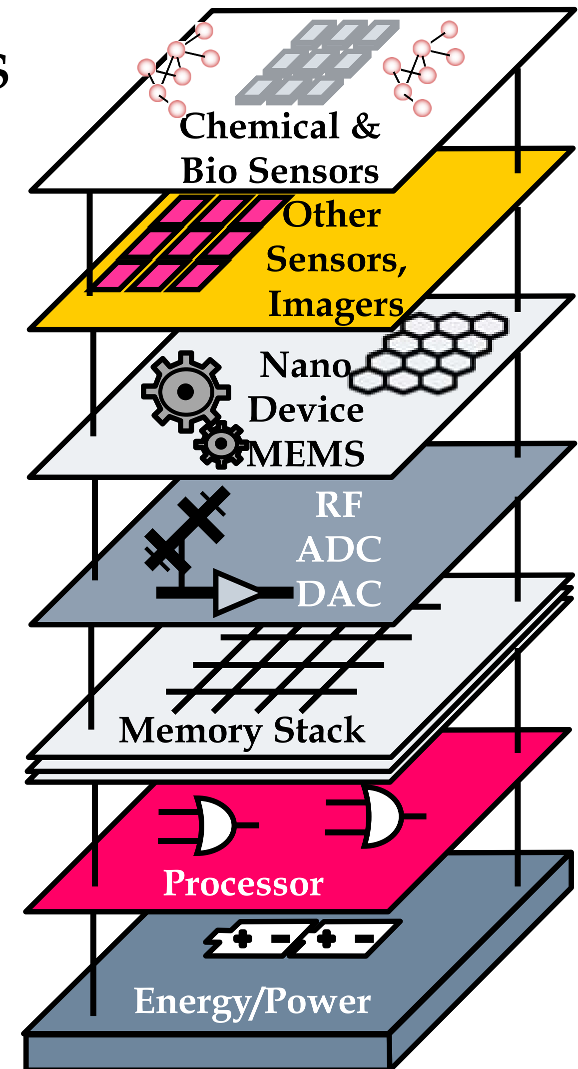
- Bonding technologies for 3D ICs
  - Wafer-to-wafer (W2W), Die-to-Wafer (D2W), and Die-to-Die (D2D)
- Comparison of different bonding technologies



	D2D	D2W	W2W
Yield Flexibility Production Throughput	**High** **High** **Low**	**High** **Good** **Good**	**Low** **Poor** **High**

Opportunities—*Heterogeneous Integration*

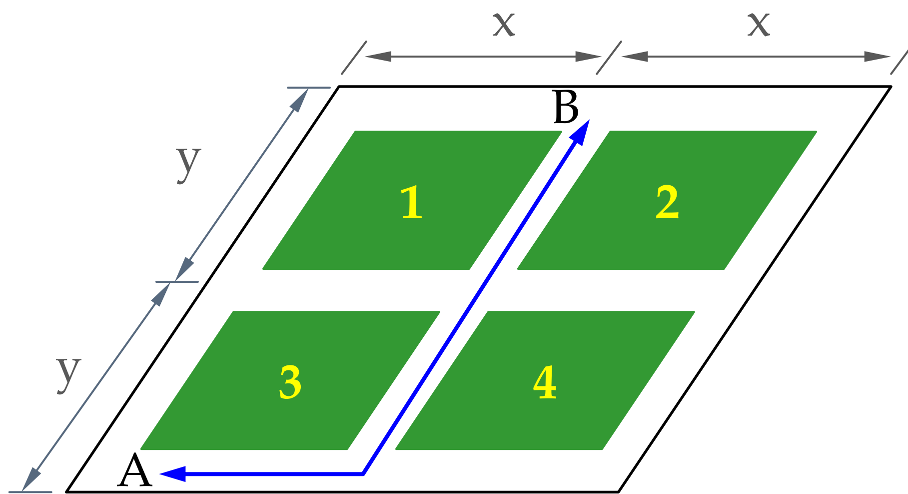
- Combine disparate technologies
  - DRAM, flash, RF, etc.
- Combine different technology nodes
  - For example: 65nm technology and 45nm technology

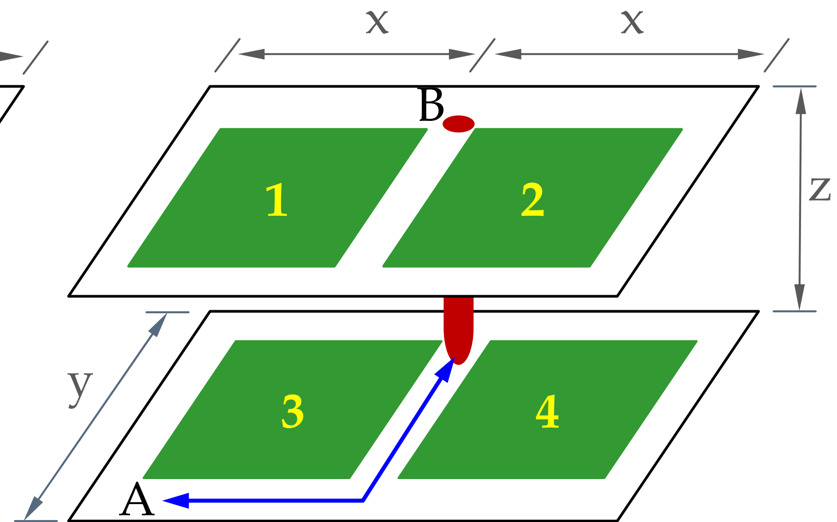


Source: Proceedings of IEEE, Jan. 2009

Opportunities—*High Performance*

- 3D integration technology can reduce the length of the long interconnections using TSV
- For example,

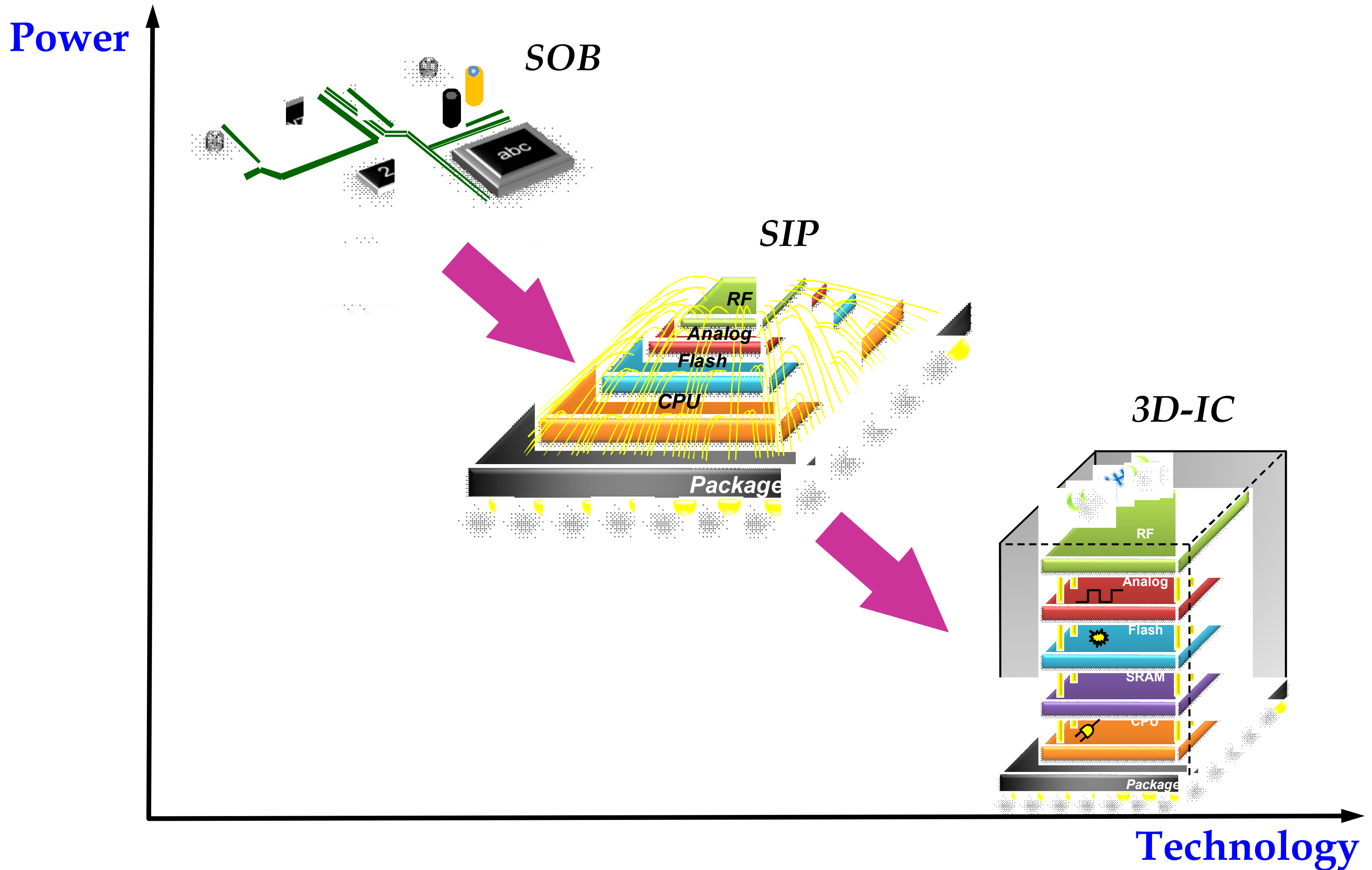




L_{2D}=x+2y

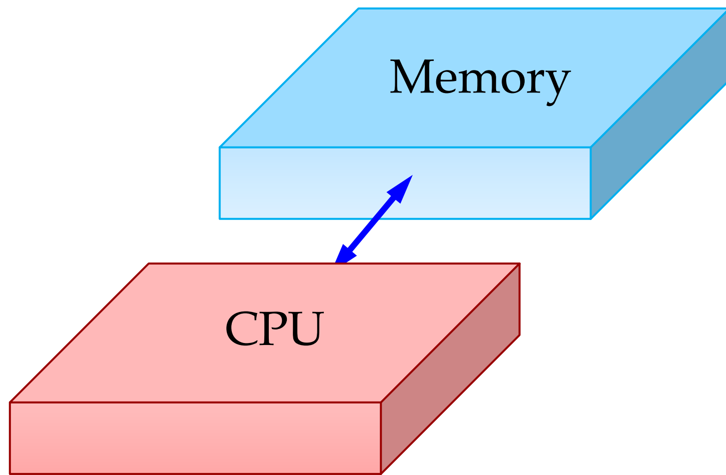
L_{3D}=x+y+z

Opportunities—*Low Power*

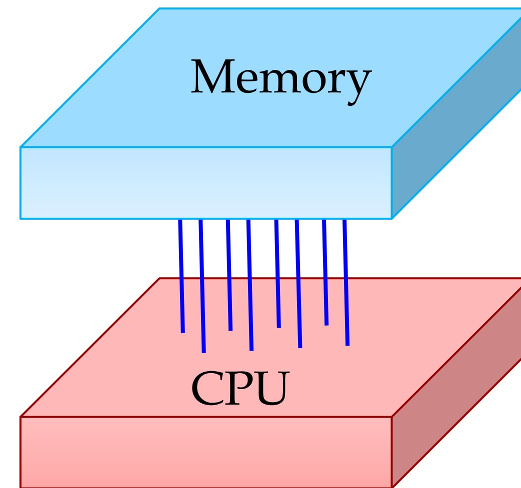


Opportunities—*High Bandwidth*

- 3D IC allows much more IO resources than 2D IC
- For example,
  - Stacking of processor and memory



Bandwidth is limited by IOs



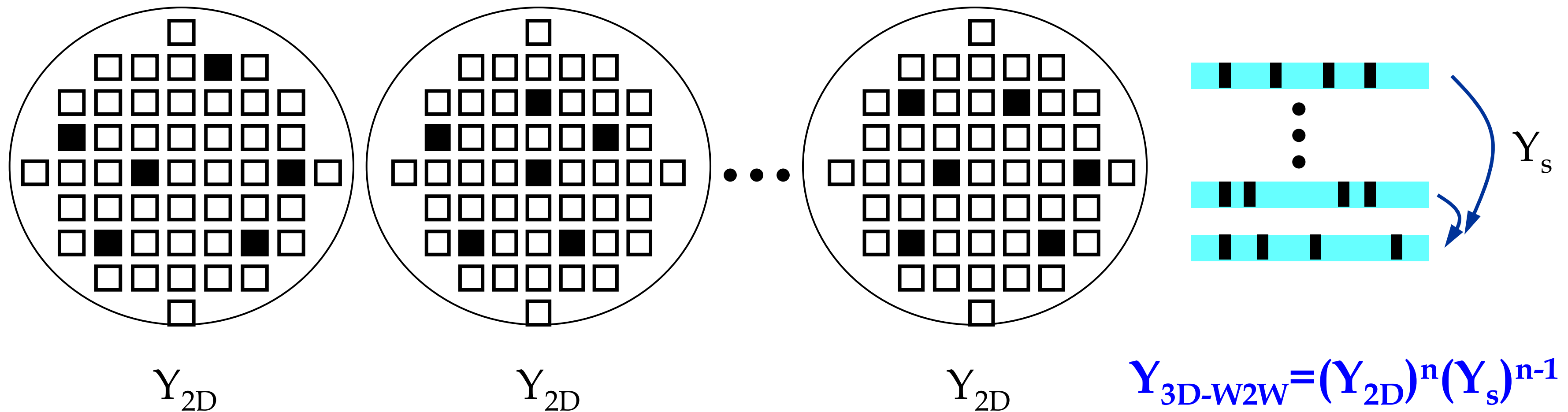
Many TSVs are allowed for high bandwidth transportation

Challenges—*Thermal Management*

- Heat removing of a 3D IC is much more difficult than that of a 2D IC
- Two key elements for thermal management
  - Thermal model
  - Design techniques
- Requirements of a thermal mode
  - High accuracy and low complexity
- Thermal design techniques
  - Thermal TSVs
  - Thermal wires

Challenges—*Yield Management*

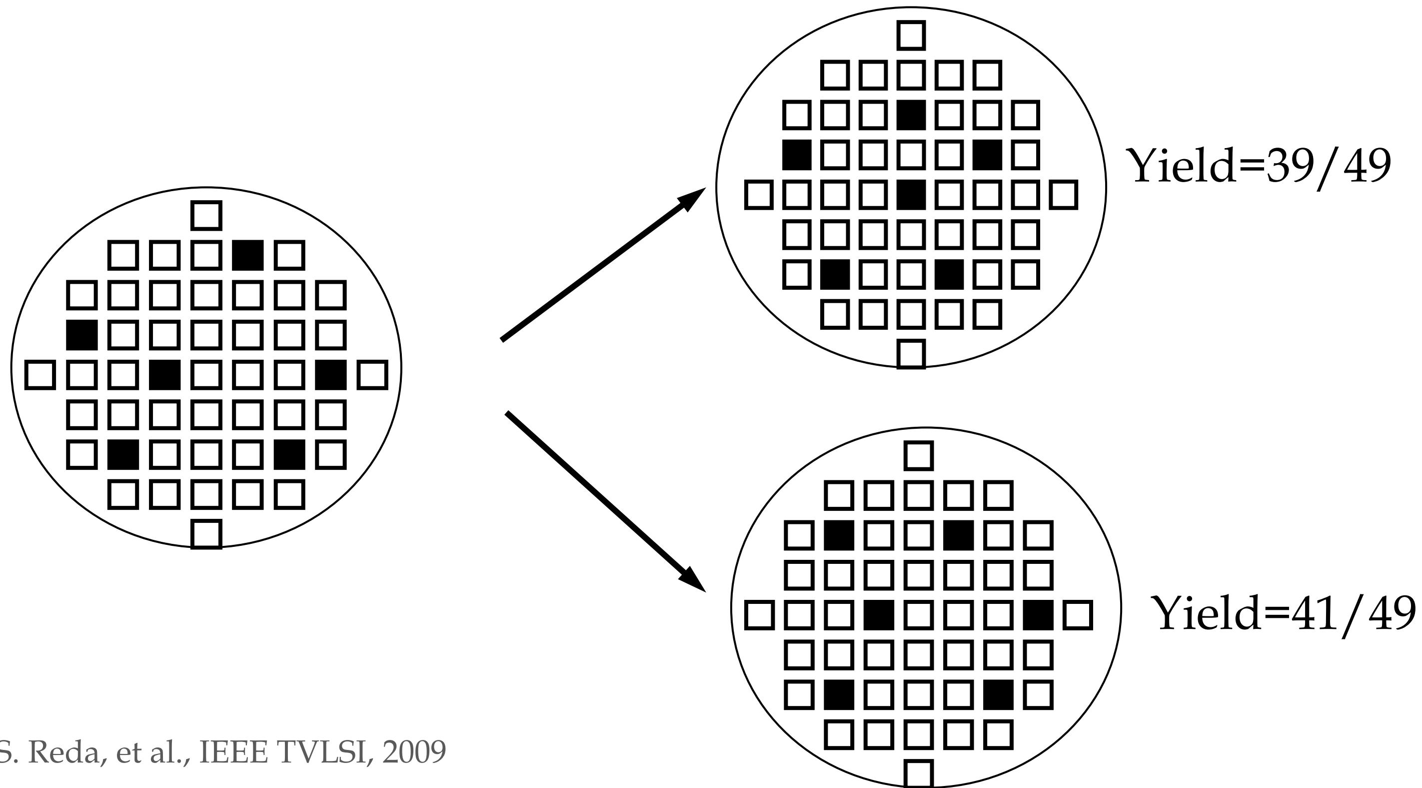
- For W2W bonding technology, the yield of 3D ICs is the product of the yields of multiple die and the yield of stacking process



Source: P. Garrou, C. Bower, and P. Ramm, "Handbook of 3D Integration".

Challenges—*Yield Management*

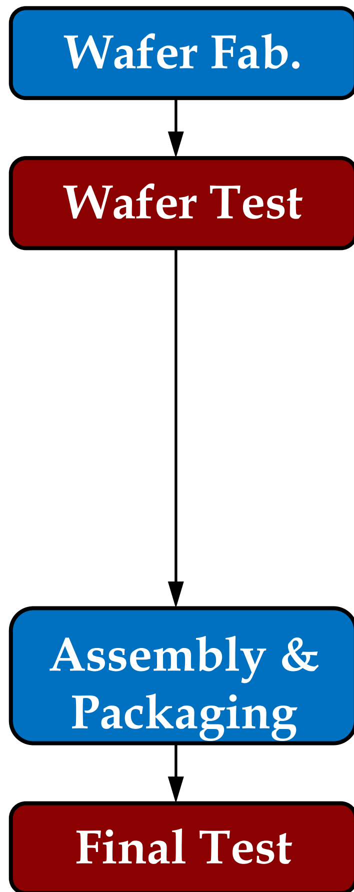
- Effective approach for maximizing the yield of W2W integration is needed



Source: S. Reda, et al., IEEE TVLSI, 2009

Challenges—*Testing*

2D-IC Test Flow



3D-IC Test Flow

Wafer Fab. 1 → KGD Test 1
Wafer Fab. 2 → KGD Test 2
Wafer Fab. n → KGD Test n

Incremental Test:

Stacking 1+2 → KGS Test 1+2
Stacking (1+2)+3 → KGS Test (1+2)+3

Assembly & Packaging → Final Test

KGD: Known-Good Die Test
KGS: Known-Good Stack Test

Source: Dr. Erik Jan Marinissen

Challenges—*Testing*

- KGD
  - Wafer-level KGD for 3D ICs is more difficult than existing KGD approaches for system-in-package (SiP)
  - The number of required test pads must be very small
- KGS
  - DFT methodology should be able to support the incremental test
- Post-bond test (final test)
  - Test optimization
- Furthermore, test optimization and integration for the overall test flow are also an important issue

Challenges—*Technological Issue*

- Although many 3D process technologies have been proposed, some issues should be addressed before 3D technology is mature enough for high-volume manufacturing
  - Alignment accuracy
  - Stacking process should not degrade the performance of the individual dies
  - Wafer thinning
  - High-quality and high density TSVs
  - …

Challenges—*Infrastructure Issue*

- CAD algorithms and tools for 3D IC designs should be developed
  - Efficient solutions that can support the complexity of 3D systems
  - Algorithms that include behavioral models for variety of components are needed
  - 3D IC design rules should be established
  - ….
- Standards
  - Various materials and processing technologies are involved in a 3D IC
  - Die or wafers can come from different IC manufacturers

Conclusions

- 3D integration technology using TSV is one of future design technologies
- It can offer many advantages over the 2D integration technology
- However, there are some challenges should be overcome before volume-production of TSV-based 3D IC becomes possible
- Also, some standards should be developed for 3D integration