Fixed-outline Thermal-aware 3D Floorplanning

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Outline

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Introduction

- 3D Integration: Motivation
  - Improved global Interconnect performance
  - Reduce footprint / Improve packing density
- Challenges for 3D Integration
  - Heat Dissipation / Thermal-aware
  - Reliability
  - Design Complexity – need a new ***floorplan***, placement, routing algorithm

Related Works

- J. Cong, J. Wei, and Y. Zhang, “a *thermal-driven* floorplanning algorithm for 3-D ICs,” in ICCAD, 2004.
- Z.Li and et al., “3d-staf: Scalable temperature and leakage aware floorplanning for three dimensional circuits,” in ICCAD, 2007.
- E. Wong and S.K.Lim, “3d floorplanning with thermal vias,” in ASPDAC, 2007.

Problem Formulation

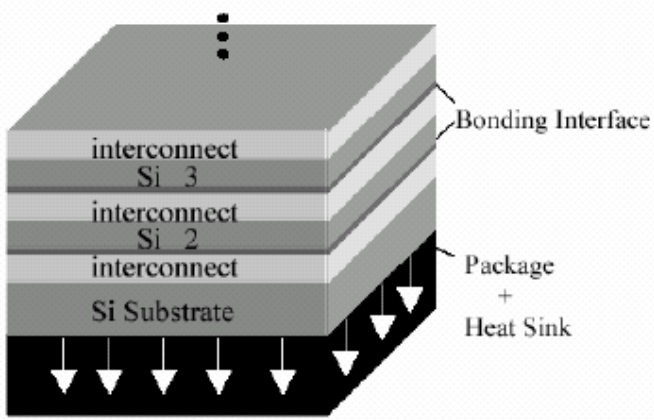
- Thermal-aware fixed-outline 3D floorplanning
  - A set of hard blocks. $(w_i \times h_i)$
  - Let *W, H and L* denote the desired width, height and layer number of the 3D IC.
  - A set of nets
  - Objective : find a coordinate (x_i, y_i, l_i) for the lower-left corner of each block:
    - such that $0 \leqslant x_i \leqslant W - w_i, 0 \leqslant y_i \leqslant H - h_i, 1 \leqslant l_i \leqslant L$ and no two blocks overlap
    - Minimize the wirelength and the peak temperature

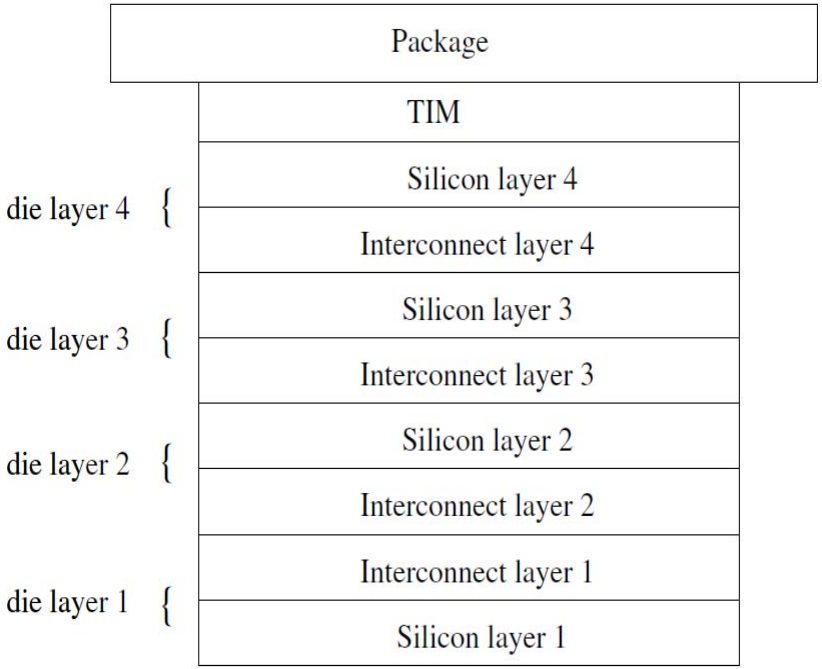
Methodology

- Fast temperature estimation
  - Propose a computationally efficient interpolation-based thermal model
- *Simulated Annealing* is used as the basic searching engine
  - Two-phase Simulated Annealing scheme.
  - 3D floorplan representation by Sequence Pair.
  - Thermal-aware random move.
- Thermal TSV Assignment
- White Space Redistribution

Fast temperature estimation

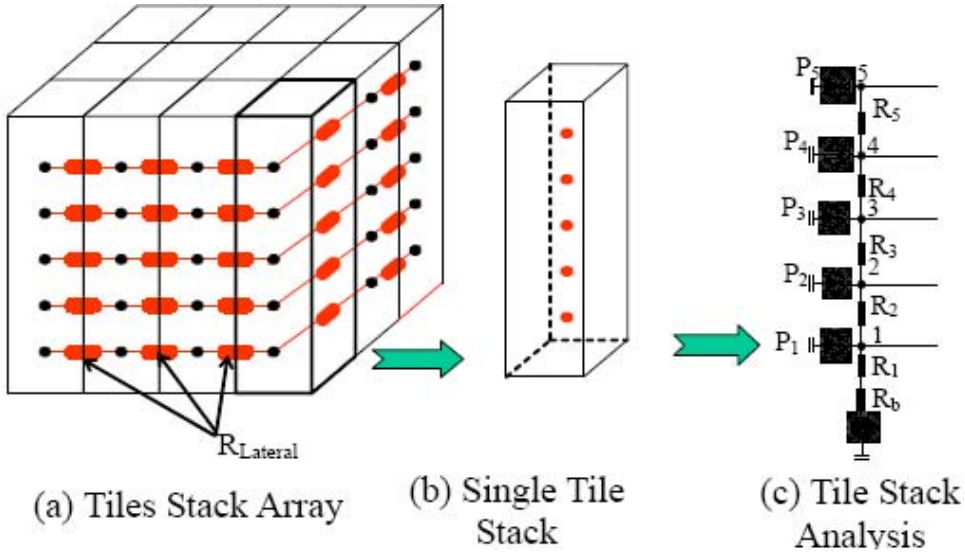
- The Hotspot thermal model is used as the starting point for the detailed model for 3D ICs.
- Technology Assumption
  - 4 layers + TIM + Package





Fast temperature estimation

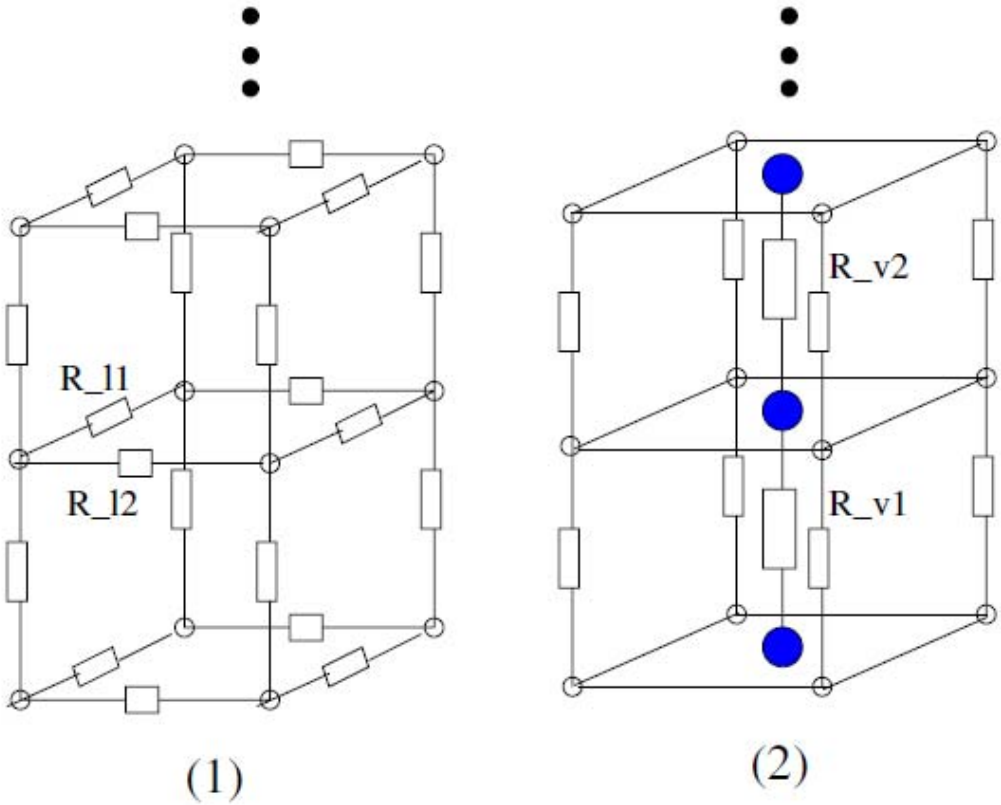
- Simplified Vertical Model
  - closed-form formula: $$T = \sum_{i=1}^{k}(P_i \sum_{j=1}^{i} R_j),$$



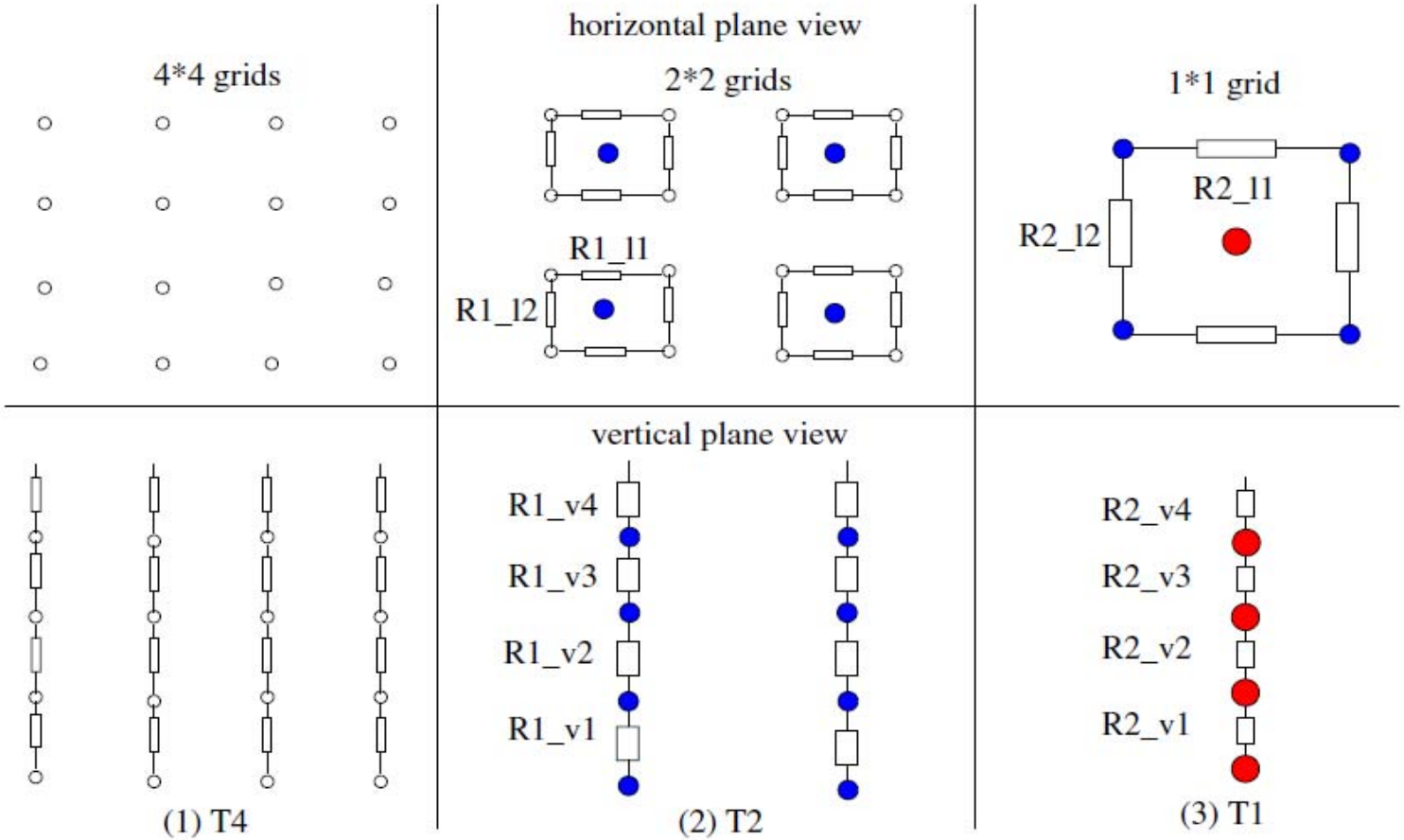
(a) Tiles Stack Array (b) Single Tile Stack (c) Tile Stack Analysis

Fast temperature estimation

- Our interpolation model.
- Example:

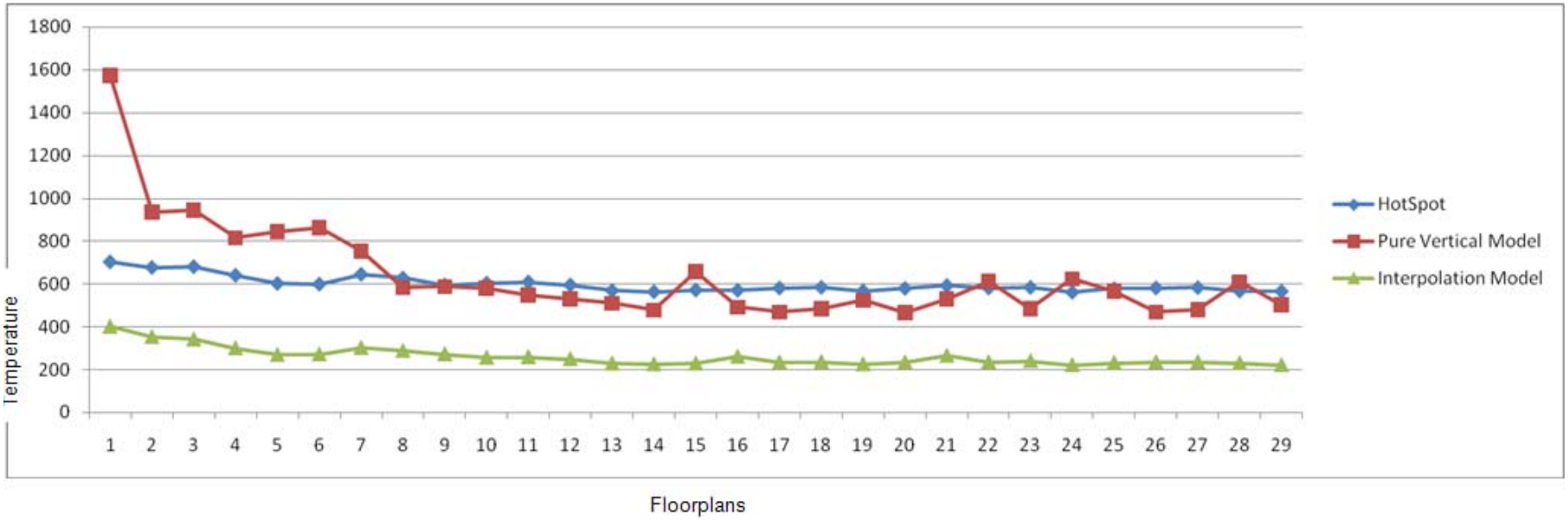


Fast temperature estimation



Fast temperature estimation

- Comparison between two models.



Simulated Annealing

- Two-phase Simulated Annealing
  - First phase:

$$cost = \alpha * narea + \beta * nAR + \gamma * nwl + \eta * c_T,$$

  - Second phase:

$$cost = max(0, (Width - W)) + max(0, (Height - H)) + \eta * c_T.$$

Simulated Annealing

- 3D floorplan representation by Sequence Pair
  - Sequence Pair Group: For each layer i, (α_i, β_i)
  - SP perturbations
    - Rotation
    - Intra-layer perturbations
      - Swap two blocks within a layer in α_i
      - Swap two blocks within a layer in α_i and β_i
    - Inter-layer perturbations
      - Swap two blocks in different a layer.
      - Move a block from layer *i* for layer *j*.
    - Thermal-aware move

Thermal TSV Assignment

- Assumption: TSVs can be inserted in white space region.
- Align white spaces of different layer.

White Space Redistribution

- A lot of white spaces waste, due to the fixed-outline constraints, and lower-left compact in SP evaluation.
- WSR – “repelling” blocks in hot area

Experimental Setup

Experimental results

- results for no temp versus proposed 2-phase algorithm

			No Temp. Consideration			Proposed 2-phase Algorithm		
Circuit	**A.R.**	**WS %**	**Succ. Rate %**	**HPWL**	**Peak Temp.**	Succ. Rate	HPWL	Peak Temp.
n100	**1**	**10**	**100**	**181608**	**453.4**	**100**	201252	**286.3**
n100	**1.5**	**10**	**100**	**179672**	**482.2**	**100**	201928	**287.7**
n100	**2**	**10**	**100**	**186167**	**494.9**	**90**	207032	**284.8**
n100	**2**	**15**	**100**	**177220**	**490.4**	**100**	207838	**241.6**
n200	**1**	**10**	**100**	**327389**	**447.3**	**100**	368415	**311.6**
n200	**1.5**	**10**	**100**	**326248**	**438.3**	**100**	376818	**292.6**
n200	**2**	**15**	**90**	**328851**	**434.2**	**90**	387580	**312.8**
Avg	-	-	-	**1.0X**	**1.0X**	-	1.14X	**0.62X**

Experimental results

- results for proposed 2-phase versus 1-phase

			Proposed 2-phase Algorithm			No Temp. Consideration			No Temp. Consideration		
Circuit	**A.R.**	WS %	Succ. Rate	HPWL	Peak Temp.	**Succ. Rate %**	**HPWL**	**Peak Temp. °C**	**Succ. Rate %**	**HPWL**	**Peak Temp. °C**
n100	**1**	**10**	**100**	201252	**286.3**	**90**	**188327**	**275.6**	**100**	**182237**	**404.9**
n100	**1.5**	**10**	**100**	201928	**287.7**	**90**	**188021**	**275.6**	**100**	**184121**	**409.4**
n100	**2**	**10**	**90**	207032	**284.8**	**20**	**211813**	**240.9**	**90**	**190667**	**361.8**
n100	**2**	**15**	**100**	207838	**241.6**	**100**	**183542**	**262.6**	**100**	**179870**	**383.3**
n200	**1**	**10**	**100**	368415	**311.6**	**100**	**338670**	**309.6**	**100**	**327605**	**402.9**
n200	**1.5**	**10**	**100**	376818	**292.6**	**50**	**371612**	**280.6**	**100**	**325917**	**382.8**
n200	**2**	**15**	**90**	387580	**312.8**	**50**	**371612**	**278.9**	**40**	**360507**	**339.6**

Packing Example

Conclusion

- Propose an approximate thermal model that could be used during 3D floorplanning
- The algorithm also considered thermal TSV assignment, white space redistribution as integral parts of the floorplanning algorithm.
- Results are very promising and show that we are able to significantly reduce the peak temperatures of 3D ICs

Thank You!