Dynamic Power Estimation for Deep Submicron Circuits with Process Variation

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Outline

- Introduction and motivation
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- Algorithm Description
  - Definitions
  - Gate characterization under process variation
  - Power estimation for a switch segment
  - Power estimation for a transition waveform
  - Power estimation for the circuit
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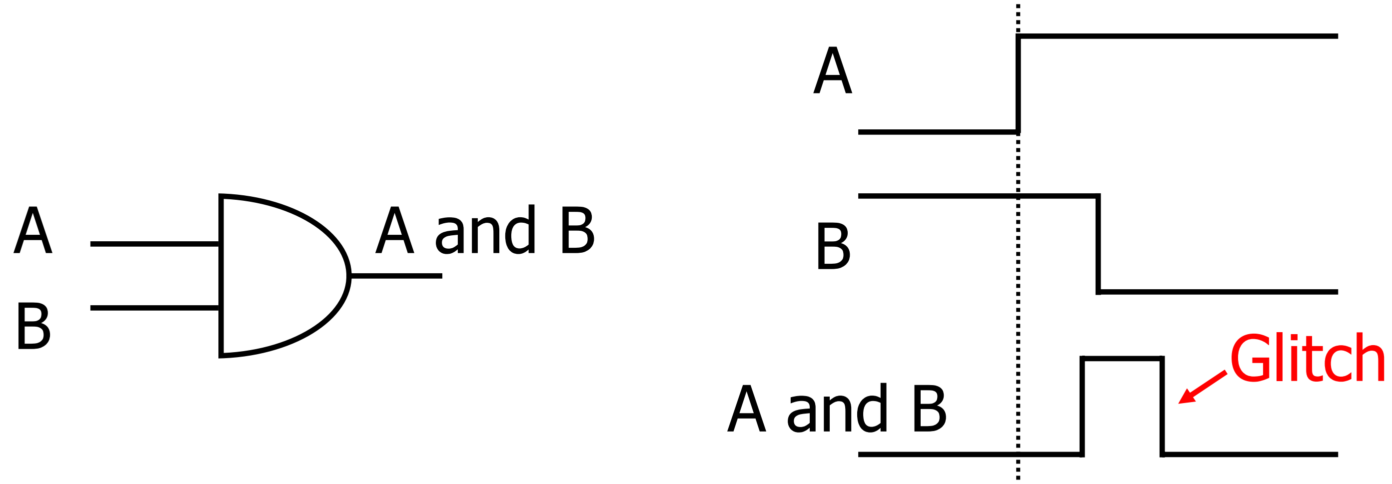
- Conclusions

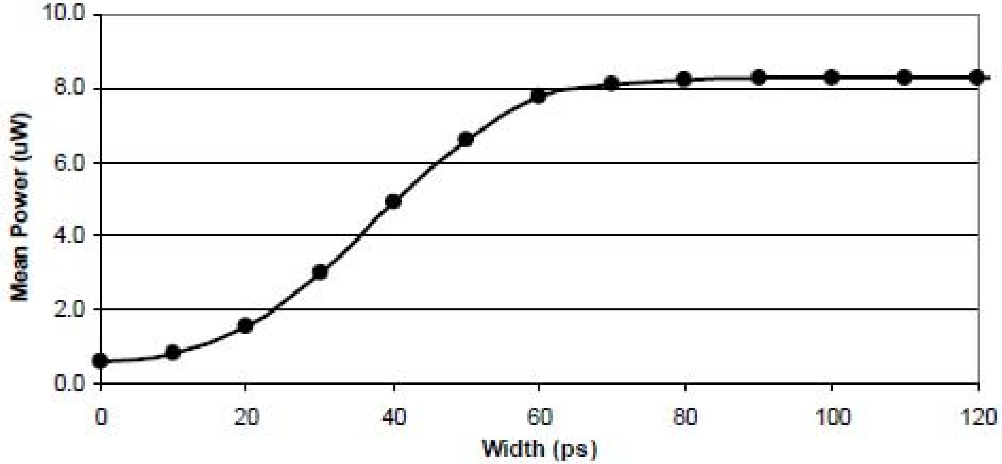
Glitches

- Signal transitions consists of:
  - Functional transitions
  - Spurious transitions (Glitches)

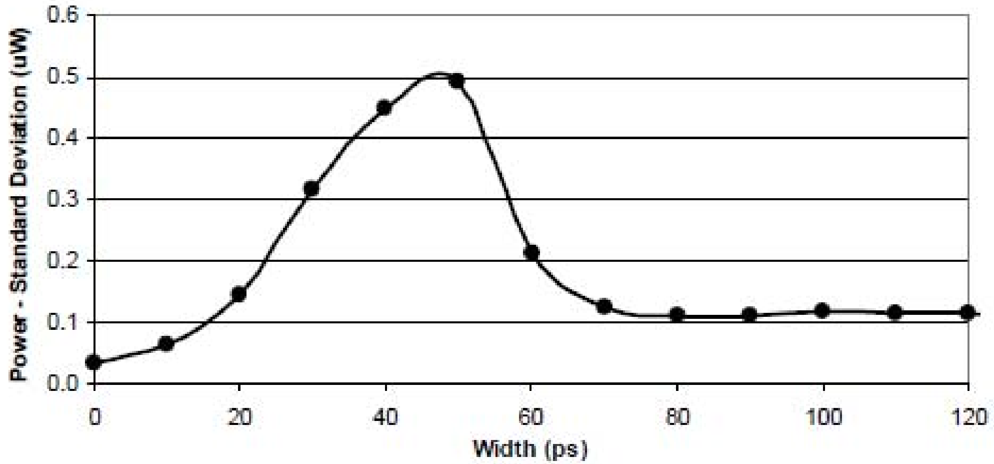


- Glitch transitions can be 4-5X of functional transitions in some data-flow intensive designs [Raghunathan, TCAD'99]
- They can be 20% of total power in FPGAs [Li, TCAD'05]

Dynamic power under process variation



Mean of the dynamic power of a logic gate vs. input glitch width



Standard deviation of the dynamic power of a logic gate vs. input glitch width

5X difference

(e.g., between width 50ps and 100ps)

Related work

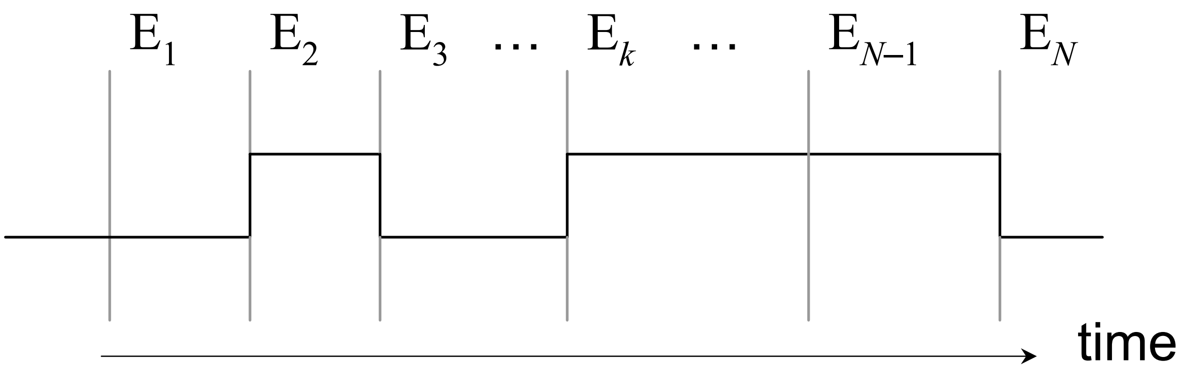
- Circuit power under process variation mainly focused on leakage power
  - [Mukhopadhyay, ISLPED'03], [Rao, TVLSI'04], [Chang, DAC'05], etc.
- Two previous works on dynamic power modeling with process variation
  - [Pilli & Sapatnekar, ISCAS'97]: Pioneer work; didn't estimate variation of dynamic power
  - [Alexander & Agrawal, ISVLSI'09]: only minimum and maximum bounds for delays are considered; no consideration of partial swing transitions

Definition: Transition Event

- A *transition event* at a particular node *n* in the circuit describes a possible transition at that node.
- No distinguishing between 0→1 and 1→0 transitions.
- Represented by three values **(p, t, σ_t)** as follows:
  - p is the probability for the transition to occur.
  - t is the mean of the time of the transition.
  - σ_t is the standard deviation of the transition time.
- For a transition event (0.2, 0.42 ns, 0.21 ns)
  - there is a likelihood of 20% that a transition occurs at a time around 0.42 ns, with a standard deviation of 0.21 ns.

Transition Waveforms

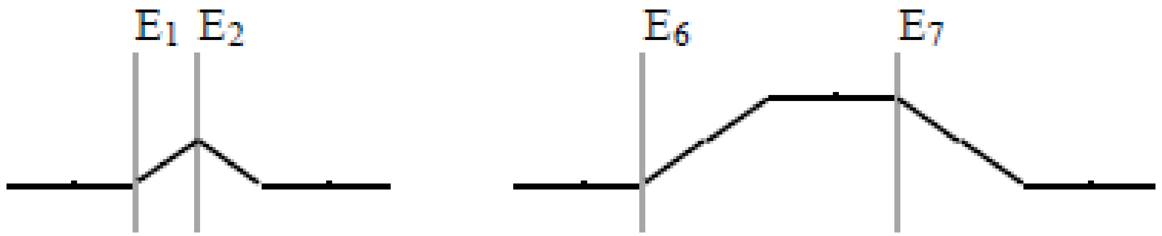
- The set of all transition events for a node are collectively represented by a *transition waveform*
  - $\{(p_1, t_1, \sigma_{t1}), (p_2, t_2, \sigma_{t2}), \ldots, (p_N, t_N, \sigma_{tN})\}$.
  - *N* transition events: $E_1, E_2, \ldots, E_N$
  - The events E_i of (p_i, t_i, σ_{ti}) are sorted according to the increasing order of t_i



In this example, events E_2, E_3 and E_N correspond to actual transitions, while events E_1 and E_{N-1} do not.

Switching Segments

- A *switching segment* is the duration from the beginning of a transition to just before the beginning of the next transition. A switching segment corresponds to exactly one transition.



Switching segment for partial-swing transition (E_1, E_2) and full-swing transition (E_6, E_7).

Algorithm: propagation through a wire segment or a gate

Source: E_S (p_S, t_S, σ_{tS})
Target: E_T (p_T, t_T, σ_{tT})

$$p_T = p_S$$

$$t_T = t_S + d$$

$$s_{tT} = \sqrt{s_{tS}^2 + s_d^2}$$

Wire segment

Input: E_I (p_I, t_I, σ_{tI})
Output: E_O (p_O, t_O, σ_{tO})

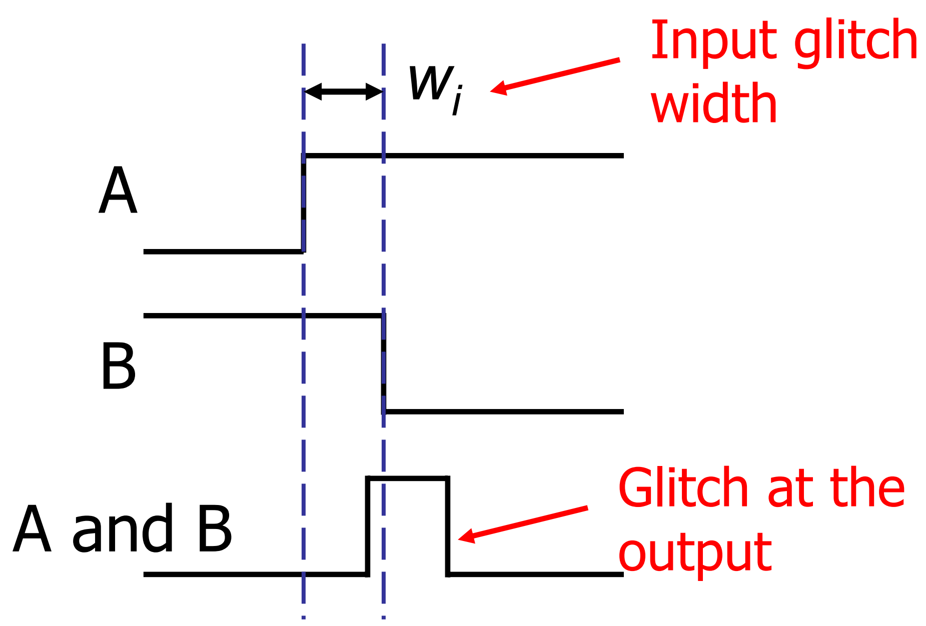
$$t_O = t_I + d$$

$$s_{tO} = \sqrt{s_{tI}^2 + s_d^2}$$

$$p_O = p_I \times P \frac{\partial f}{\partial x_i}$$

Gate

Dynamic power for an input glitch width



- $DPower(w_i)$ is a random variable due to
  - variation in the load capacitance
  - variation in the gate delay from different inputs to the output

Gate power characterization

- Gate Characterization under
  - different input glitch widths (20 different widths, from 0ps to 190ps)
  - different load capacitances
- Build look-up tables
  - Look up and interpolate the mean $\mu_C(w_i)$ and standard deviation $\sigma_C(w_i)$ of dynamic power for a given w_i and a given load capacitance.

Compute probability for w_i

Discretize the width into w_0, w_1,…, w_L.
The probability that $w = w_i$ is:

$$\Pr\{w = w_i\} = \frac{1}{s_w\sqrt{2p}} \exp\left(-\frac{(w_i - m_w)^2}{2s_w^2}\right)$$

Normalize this probability as follows:

$$PN_i = \frac{\Pr\{w = w_i\}}{\sum_j \Pr\{w = w_j\}}$$

Compute the mean of the dynamic power for a switch segment

For each w_i, we can look-up and interpolate the corresponding mean power $\mu_C(w_i)$ and standard deviation $\sigma_C(w_i)$

$$\mu_C(w_i) = E\left[DPower(w) \,\middle|\, w = w_i\right]$$

$$\sigma_C(w_i) = \sqrt{E\left[\left(DPower(w) - \mu_C(w_i)\right)^2 \,\middle|\, w = w_i\right]}$$

The overall (unconditional) mean dynamic power μ_{DP}

$$\mu_{DP} = E\left[DPower(w)\right] = \sum_i PN_i \times \mu_C(w_i)$$

Compute the standard deviation for a switch segment

The overall (unconditional) standard deviation σ_{DP} is

$$\sigma_{DP} = \sqrt{E\left[\left(DPower(w) - \mu_{DP}\right)^2\right]}$$

$$E\left[\left(DPower(w_i) - \mu_{DP}\right)^2\right] = \left(\mu_C(w_i) - \mu_{DP}\right)^2 + \sigma_C(w_i)^2$$

$$\sigma_{DP} = \sqrt{\sum_i PN_i \times \left[\left(\mu_C(w_i) - \mu_{DP}\right)^2 + \sigma_C(w_i)^2\right]}$$

Compute dynamic power for a gate

For a gate with the transition waveform
$\{(p_1, t_1, \sigma_{t1}), (p_2, t_2, \sigma_{t2}), \ldots, (p_N, t_N, \sigma_{tN})\}$.

$$m_{DPgate} = \sum_{i=1}^{N-1} \sum_{j=i+1}^{N} Pr(i,j) \cdot m_{DP}(i,j)$$

$$s_{DPgate} = \sqrt{\sum_{i=1}^{N-1} \sum_{j=i+1}^{N} Pr(i,j) \cdot s_{DP}(i,j)^2}$$

$$Pr(i,j) = p_i \cdot p_j \cdot \prod_{k=i+1}^{j-1} (1 - p_k)$$

Dynamic power for the circuit

- Assume that the power for the gates are independent random variables of normal distribution, the total dynamic power is:

$$m_{DPcircuit} = \sum_{\text{all gates}} m_{DPgate}$$

$$s_{DPcircuit} = \sqrt{\sum_{\text{all gates}} s_{DPgate}^{2}}$$

Experiment Settings

- We used a 45nm Nangate FreePDK45 Generic Open Cell Library
- We introduced 20% random variation of normal distribution to four process parameters
  - W_g, L_{eff}, T_{OX} and *na*
  - Similar variation is added to the unit R and C for wires
- 10000 Monte Carlo samples, each with 1000 clock cycles

Dynamic power estimation vs. HSPICE–based Monte Carlo simulation

	Dynamic Power (μ W)				**Differences (%)**	
	HSPICE		Our Model			
	mean	σ	mean	σ	**mean**	σ
Circuit 1	2.649	0.2346	2.719	0.2479	–2.64	–5.67
Circuit 2	3.094	0.3816	2.961	0.3996	4.30	–4.72
Circuit 3	3.481	0.3865	3.514	0.4114	–0.95	–6.44
Circuit 4	3.186	0.3371	3.097	0.3539	2.79	–4.98
Circuit 5	4.491	0.4829	4.664	0.4970	–3.85	–2.92
Average of Absolute Differences					**2.91**	**4.95**

Runtime comparison

	HSPICE (hours)	Our Model (seconds)	**Speed-up ($\times 10^6$)**
Circuit 1	1692	2	3.0
Circuit 2	1824	2	3.3
Circuit 3	4326	2	7.8
Circuit 4	6120	2	11.0
Circuit 5	9776	2	17.6
Average			**8.5**

Results for ISCAS89 circuits

	Dynamic Power		Runtime (sec)
	Mean (mW)	σ (%)	
C1355	1.10	36.7	8
C1908	2.56	16.8	11
C2670	4.24	16.1	43
C3540	6.86	34.0	40
C432	0.85	20.5	4
C499	1.01	32.5	7
C5315	10.46	19.0	90
C6288	20.16	24.4	64
C7552	13.42	17.2	119
C880	1.02	27.4	8

Conclusions

- We presented a novel dynamic power estimation method for circuits with process variation
- Our estimation takes into account the difference between partial-swing and full-swing glitches
- We obtained high accuracy estimates, with average errors of 3% for the means and 5% for the standard deviations
- Our estimation is also very fast, more than six orders of magnitude comparing to SPICE-Monte Carlo
- Future work includes consideration of the correlation among the process parameters

Thank You