Resilient Design in Scaled CMOS for Energy Efficiency

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Resilient platforms

Resiliency framework

Applications
Programming System
OS
VM
Firmware
Microcode
Microarchitecture
Circuit & Design

Resiliency for performance, efficiency & reliability

Resilient platform features
- Error detection
- Fault diagnosis
- Fault confinement
- Error correction
- System recovery
- System adaptation
- System reconfiguration

Less recovery overhead
Lower error rate
Less silicon overhead
Dynamic adaptation & reconfiguration

Adapt & reconfigure for **best** power-performance
Voltage-frequency range limiters

Vmax/Fmax limiters
- Reliability
- Thermals
- Power delivery

Vmin limiters
- Circuit functional failures
- Soft errors
- Steep frequency roll-off
- Aging

Reliability & functional failures limit range
Voltage-frequency margins

- **V variation**
  - Voltage vs. Frequency
  - IR drop
  - Inductive droops
  - Load line variations

- **T variation**
  - Voltage vs. Frequency
  - Nominal T
  - Worst T

- **Aging**
  - Voltage vs. Frequency
  - Nominal
  - Worst

- **Path activity**
  - Voltage vs. Frequency
  - Nominal
  - Worst
Multi-voltage cache

Array Vmin

Cumulative fail rate

Array voltage

Worst die Vmin

Nominal array Vmin

SER, erratic bits

Vmin

Density

6T SRAM

Multi-V

6T SRAM

8T+ cell

LLC density

Push active Vmin limit to Vmax

uP Core

\[ V_{\text{CORE}} = \sqrt{1.2V} \]

\[ V_{\text{CORE}} = \sqrt{0.7V} \]

\[ V_{\text{CORE}} = \sqrt{0.6V} \text{ (standby)} \]

\[ V_{\text{LLC}} = 1.2V \]

Embedded level shifters for wordline & write drivers minimize area & power overhead
Dynamic multi-voltage cache

6T SRAM cell

<table>
<thead>
<tr>
<th></th>
<th>Read</th>
<th>Write</th>
<th>Retention</th>
</tr>
</thead>
<tbody>
<tr>
<td>NX</td>
<td>Weak</td>
<td>Strong</td>
<td></td>
</tr>
<tr>
<td>NPD</td>
<td>Strong</td>
<td>Weak</td>
<td>Balanced</td>
</tr>
<tr>
<td>PPU</td>
<td>Strong</td>
<td>Weak</td>
<td>Balanced</td>
</tr>
</tbody>
</table>

Wordline underdrive for read

Dynamic voltage collapse for write

Array to WL differential supply noise tracking

Pulse width control

45nm dynamic multi-V testchip

Transistor count: 6.2M
Chip Area: 0.91mm²
Vcc: 1.1V-0.7V
Testing interface: membrane probe card

MIN cell

Source: Intel

VWL(V)

Relative Single Bit Fails

0.7 0.8 0.9 1 1.1

1.0E+10 1.0E+08 1.0E+06 1.0E+04 1.0E+02 1.0E+00

26X less fails
Cache reconfiguration

Reduce cache size @ low V/F by eliminating failing words/bits

Word disable

Failing words

Bitmap of failing words

1-bit ECC

Word disable

Bit fix

10-bit ECC

Source: Intel

<table>
<thead>
<tr>
<th></th>
<th>Vmin (mV)</th>
<th>Density</th>
<th>Capacity</th>
<th>Latency (cycles)</th>
<th>IPC</th>
<th>EPI</th>
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<tbody>
<tr>
<td>Conventional</td>
<td>660</td>
<td>1*</td>
<td>1*</td>
<td>L1: 3</td>
<td>1*</td>
<td>1*</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>L2: 20</td>
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<tr>
<td>32KB L1</td>
<td>500</td>
<td>0.92</td>
<td>0.5</td>
<td>4</td>
<td>0.95</td>
<td>0.5</td>
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<tr>
<td>Word disable</td>
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<tr>
<td>2MB L2</td>
<td>500</td>
<td>1</td>
<td>0.75</td>
<td>23</td>
<td>0.95</td>
<td>0.5</td>
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<tr>
<td>Bit fix</td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

* Normalized reference value

Source: Intel
Low-voltage logic design

Narrow muxes
No stack height > 2

Robust flip-flops

Robust level converters

Design & technology optimizations to balance range, performance & efficiency

Efficiency: MIPS/Watt

Improve range

Impact max performance

Efficiency: MIPS/Watt

Improve range

& efficiency

Performance

Performance
Low-voltage motion estimation engine

- **Multi-Vcc design**
  - 65nm CMOS
  - 70K transistors
  - Die area ~1mm²

- **Wide V-F range**

- **412 Gops/Watt @ 320 mV!**

- **Functional down to 240 mV!**
Dynamic V & F adaptation

Environment-aware dynamic adaptation
- Adapt F/V to V/T change → reduce V/T margin
- Adapt F/V to aging → reduce aging margin

Prototype chip in 90nm

Source: Intel
Resilient circuits

- Detect errors in critical path FFs
- Propagate error signals
- Correct errors by re-execution
- Feedback to adaptive V/F

65nm resilient circuits testchip
Resiliency experiments

Response to voltage droops

- Conventional Design:
  - 21% Throughput Gain
  - 37% Power Reduction

- Resilient Design:
  - 21% Throughput Gain
  - 37% Power Reduction

Source: Intel
Summary

• Resilient platforms offer better performance, energy efficiency and reliability

• Resiliency, dynamic adaptation and reconfiguration will be critical in scaled CMOS

• Logic and memory design innovations will be needed to keep pushing the voltage scaling limits