A New Method to Improve Accuracy of Parasitics Extraction Considering Sub-wavelength Lithography Effects

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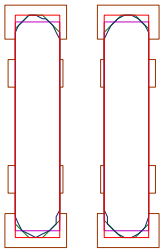
- Motivation
- Impacts of Pattern Rounding on Parasitics
- A Novel Fully Model-Based Ret-Aware LPE Method
- Shape Approximation
- Parasitics Extraction with Shape Approximation
- Summary and Conclusions

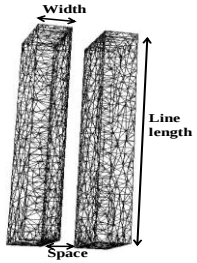
Motivation

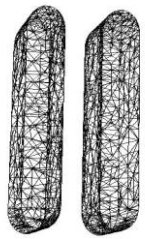
- Limited optical lithography resolution
  - Min. Half Pitch = $k_1 \cdot \lambda$ / NA, $k_1 \geq 0.25$
  - 45-nm HP node, λ = 193 nm, NA = 1.35 (water), k_1 = 0.31
- Even with strong RETs, line end rounding and corner rounding still inevitable
  - Q1: How much does this affect parasitics?
  - Q2: Can the effect be full-chip extracted efficiently?

Impacts of Pattern Rounding on Parasitics

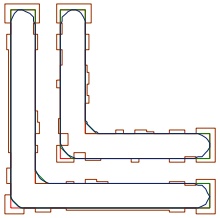
- FreePDK 45 design rules, M1 Pitch = 130 nm, line length 2P – 5P, Mentor Calibre OPC, Silvaco Clever

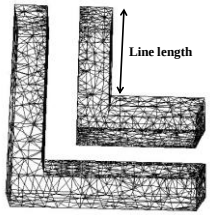


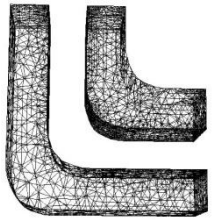




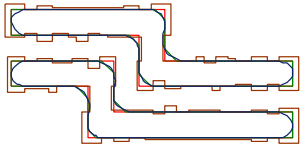
Parallel lines
C: 6 to 3 %
R: 4.4 to 5%

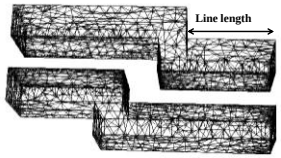


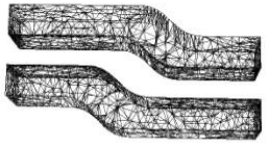




Parallel L-shaped Lines
C: 4 to 2.6 %
R: 4.8 to 2%



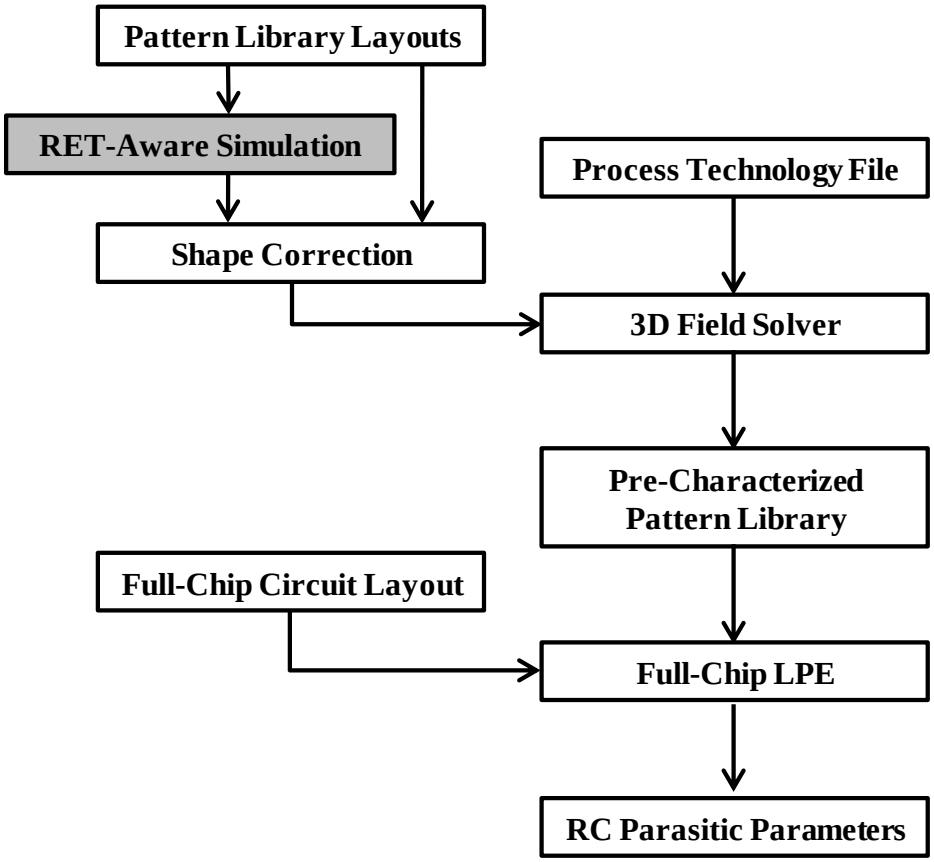




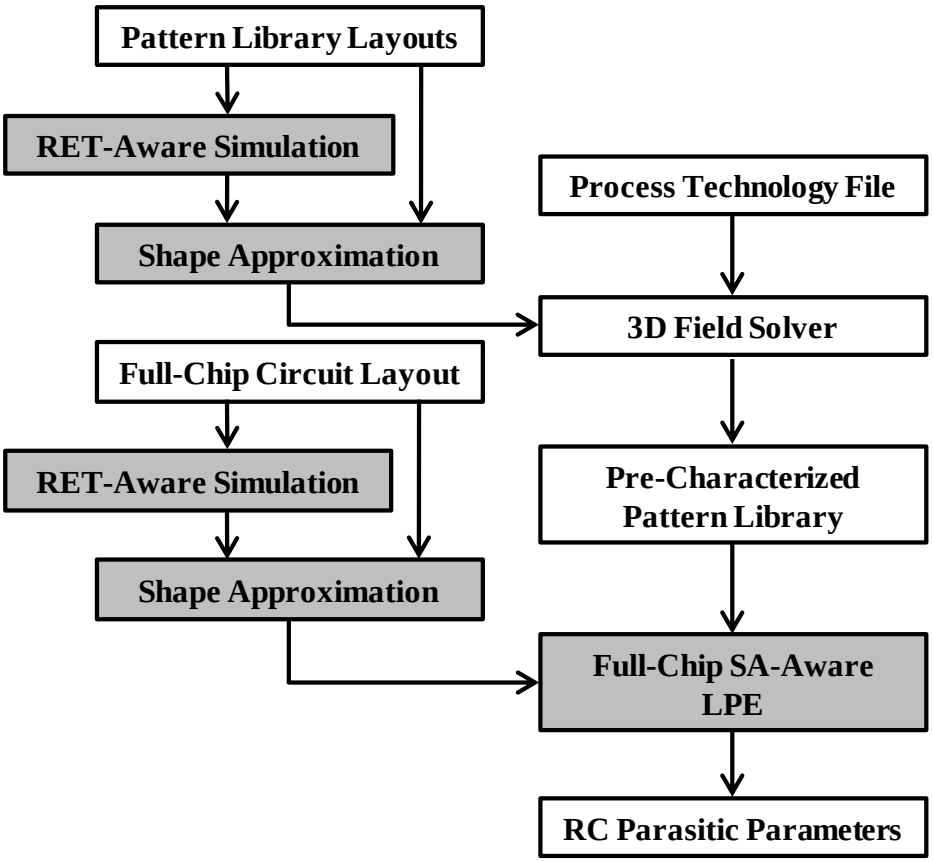
Parallel Z-shaped Lines
C: 4.8 to 3 %
R: 6 to 3.3%

A Ret-Aware Layout Parameter Extraction (LPE) Method with Shape Correction

- Zhou et al., ASPDAC 2007
- SC approximates post-RET contours with edge biases on drawn layouts
  - Rounding NG
- Full-chip drawn layouts compared with SC-corrected pattern libraries
  - Litho. proximity NG

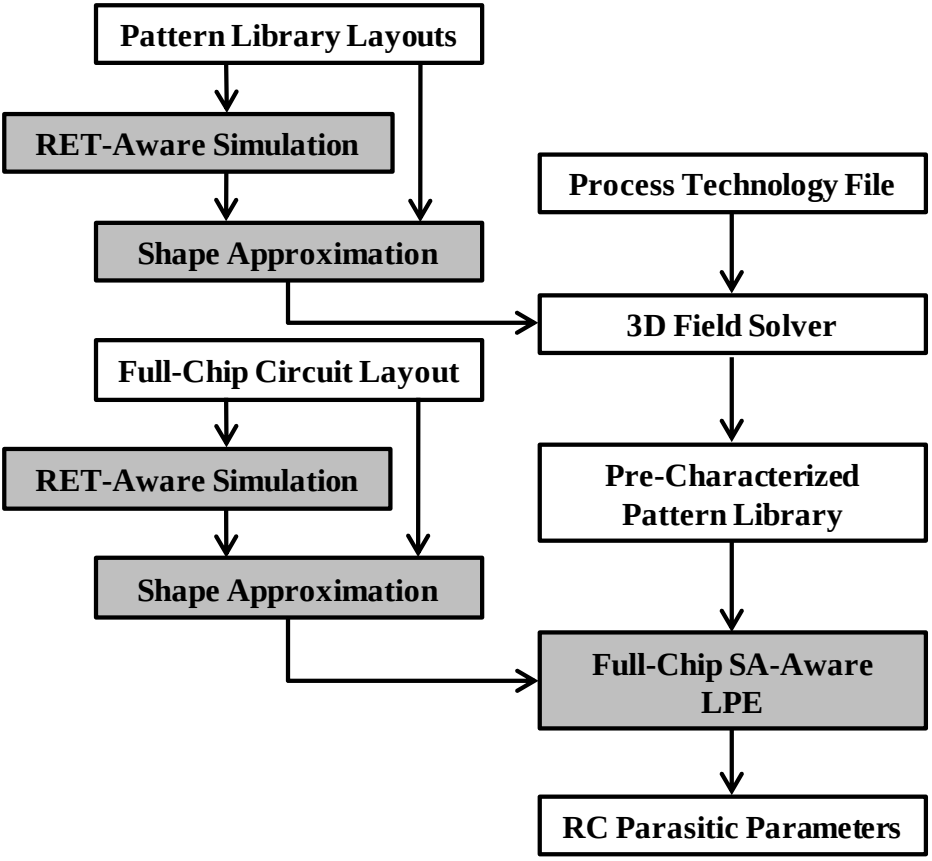


A Fully Model-based Ret-Aware LPE Method with Shape Approximation

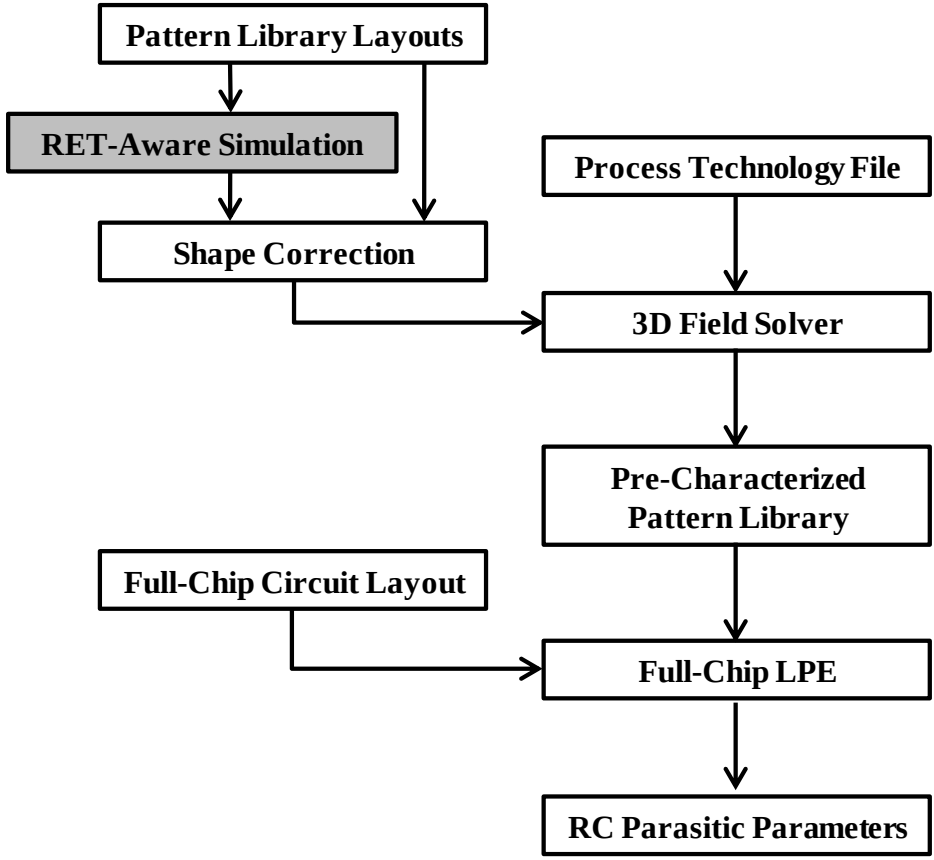


- Tsai et al., ASPDAC 2010
- SA approximates post-RET contours with edge biases on corner-patched drawn layouts
  - Rounding OK
- Full-chip post-RET contours also SA'ed, compared with SA-aware pattern libraries
  - Litho. proximity OK

ASPDAC 2010 vs. ASPDAC 2007 RET-Aware LPE Flows

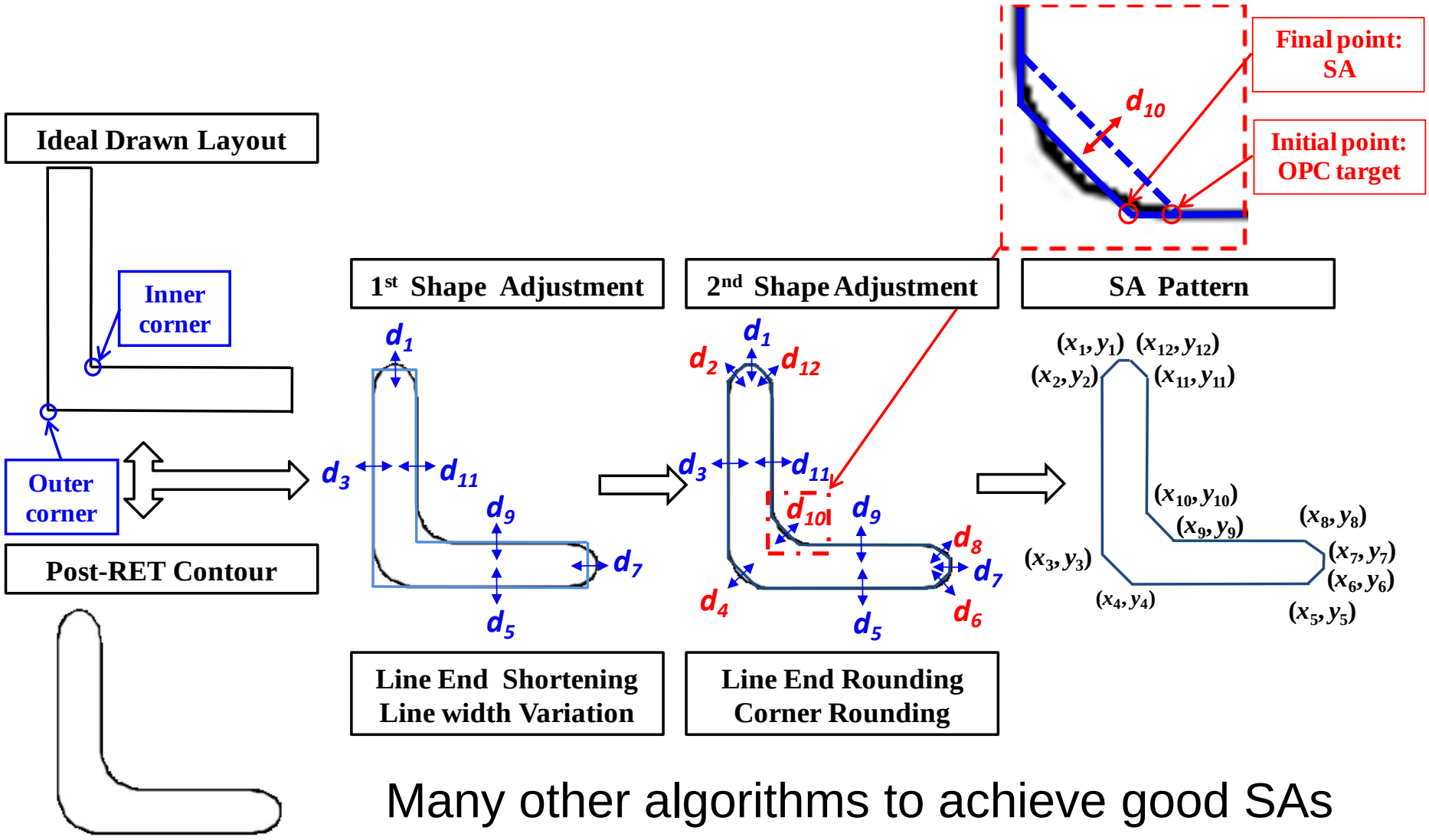


Tsai et al., 2010 (Fully model-based library and LPE)



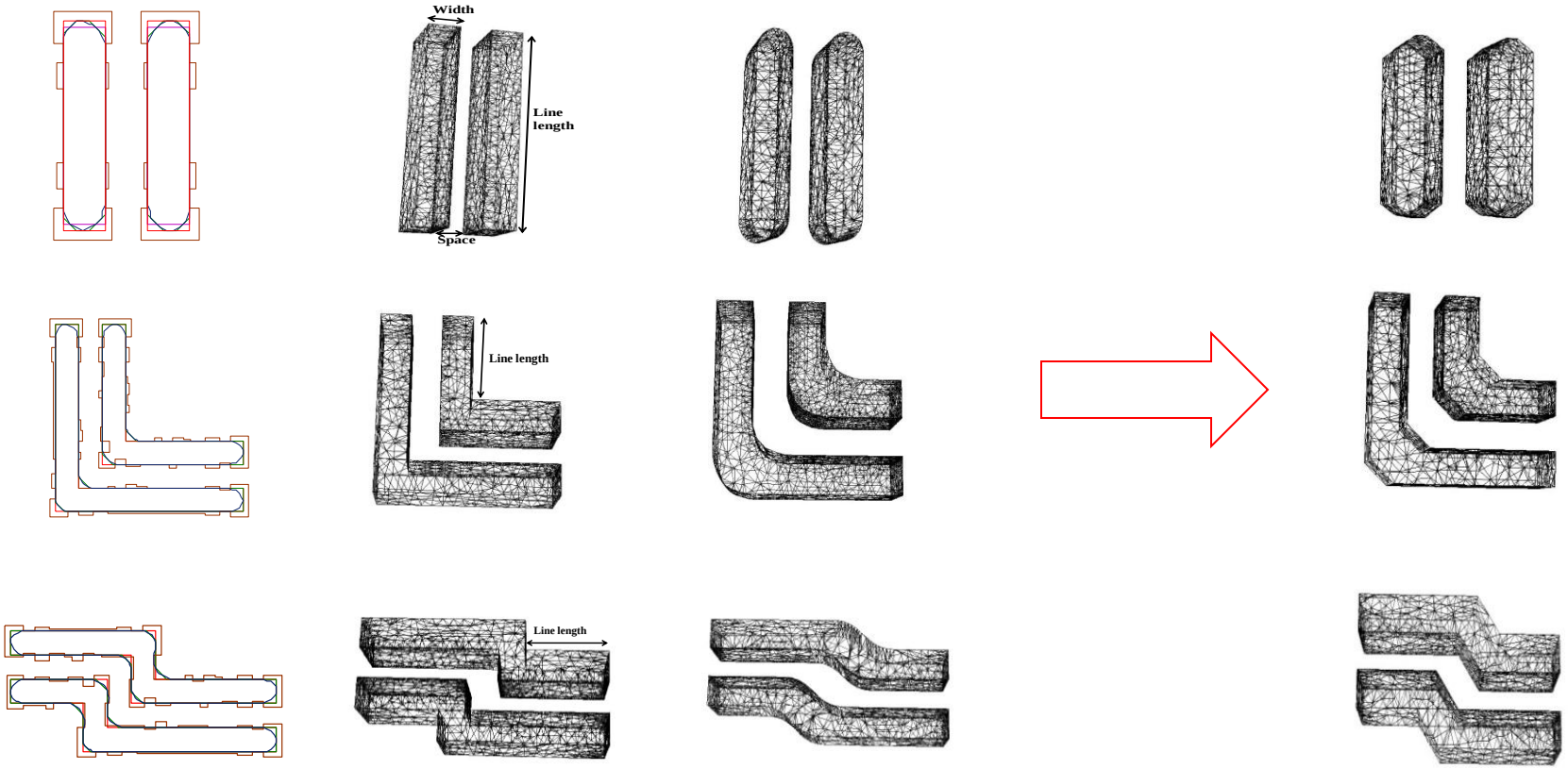
Zhou et al., 2007 (Model-based library)

One Shape Approximation Algorithm



Many other algorithms to achieve good SAs (see paper)

3D Structures Generated by Shape Approximation



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Capacitance and Resistance of Parallel I-shaped Lines

	Capacitance ($\times 10^{-16}$ F)				Resistance (Ω)			
Length (P)	OPC	Ideal (%)	SC (%)	SA (%)	OPC	Ideal (%)	SC (%)	SA (%)
2	0.22	5.6	1.86	0.94	0.50	4.58	1.56	0.93
2.5	0.28	5.45	1.92	0.73	0.63	5.48	2.19	0.27
3	0.32	4.41	1.57	0.85	0.76	4.82	2.13	0.98
3.5	0.37	4.76	1.23	0.42	0.90	4.13	1.84	0.91
4	0.42	3.71	1.67	-0.64	1.03	4.46	2.45	0.73
4.5	0.49	3.84	1.42	-0.88	1.16	4.65	2.85	0.89
5	0.52	2.94	1.34	-0.22	1.29	4.63	3.02	0.81

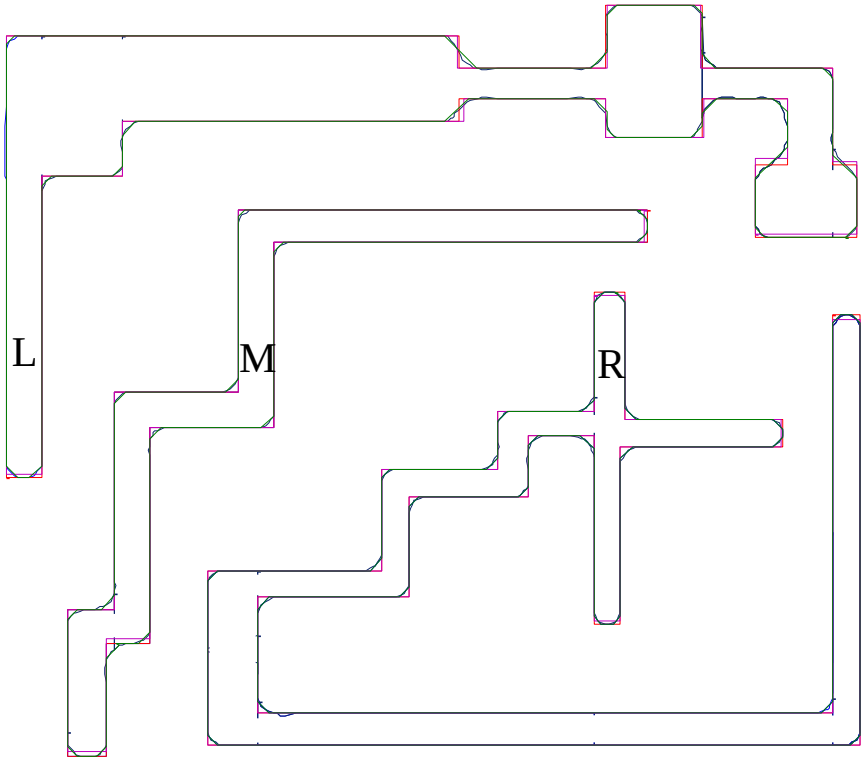
Capacitance and Resistance of Parallel L-shaped Lines

	Capacitance ($\times 10^{-16}$ F)				Resistance (Ω)			
Length (P)	OPC	Ideal (%)	SC (%)	SA (%)	OPC	Ideal (%)	SC (%)	SA (%)
2	0.56	4.12	4.12	0.01	1.06	4.84	4.84	0.95
2.5	0.67	4.18	4.18	0.29	1.32	3.78	3.78	0.52
3	0.80	2.61	2.61	0.25	1.59	3.02	3.02	0.41
3.5	0.90	3.17	3.17	0.36	1.85	2.77	2.77	0.61
4	1.02	2.49	2.49	0.15	2.10	2.48	2.48	0.38
4.5	1.12	2.78	2.78	0.11	2.38	2.05	2.05	0.45
5	1.24	2.57	2.57	0.22	2.64	1.94	1.94	0.35

Capacitance and Resistance of Parallel Z-shaped Lines

	Capacitance ($\times 10^{-16}$ F)				Resistance (Ω)			
Length (P)	OPC	Ideal (%)	SC (%)	SA (%)	OPC	Ideal (%)	SC (%)	SA (%)
2	0.54	4.77	4.77	-0.5	1.26	6.12	6.12	1.21
2.5	0.65	5.18	5.18	-1.21	1.52	5.89	5.89	1.01
3	0.77	3.34	3.34	-0.76	1.77	5.44	5.44	0.87
3.5	0.87	4.43	4.43	-0.96	2.05	4.62	4.62	0.75
4	0.98	3.59	3.59	-0.78	2.29	4.63	4.63	0.76
4.5	1.09	3.65	3.65	-0.87	2.57	3.51	3.51	0.94
5	1.21	3.13	3.13	-0.44	2.78	3.28	3.28	0.62

Relative Capacitance Extraction Errors vs. Post-OPC Contour of a 2.2 μm × 1.9 μm Random Layout



	Capacitance ($\times 10^{-16}$ F)			
Pair	OPC	Ideal (%)	SC (%)	SA (%)
C_{LM}	0.76	2.5	0.89	0.063
C_{MR}	0.63	2.8	1.26	0.47
C_{LR}	0.30	3.2	1.32	0.29

Summary and Conclusions

- An efficient fully model-based RET-aware full-chip LPE method proposed
  - Full-chip post-RET litho. simulation: sub-wavelength proximity effects accurately quantified
  - Shape approximation: line end rounding and corner rounding distortions better handled
  - 3D field solvers: pattern library characterization
  - LPE techniques for non-Manhattan features: SA-patched layouts should be handled (ongoing)
- A step forward to a fully model-based electrical-performance-aware design for manufacturability (e-DFM) flow.

Acknowledgement

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