# A GLOBAL INTERCONNECT REDUCTION TECHNIQUE DURING HIGH LEVEL SYNTHESIS

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# Outline

- Introduction
- Motivating Example
- Interconnect Reduction By Using Idle FUs
- Experimental Results
- Conclusion

# Interconnect in VLSI design



- Global interconnect problem in VLSI design
  - Latency and power consumption in 35nm node [Meindl'03]
    - Gate : 2.5 ps
    - 1 mm wire : 250 ps

    

    100 times difference
  - 50% of dynamic power of Intel microprocessor results from interconnect switching [Magen'04]

# Our Approach



- Proposed interconnect assignment algorithm that uses idle FUs for data delivery
  - Use functional units as interconnect components as well as metal wires
  - Incorporated placement information for accurate interconnect length estimation
  - Solved the interconnect assignment problem by network flow formulation

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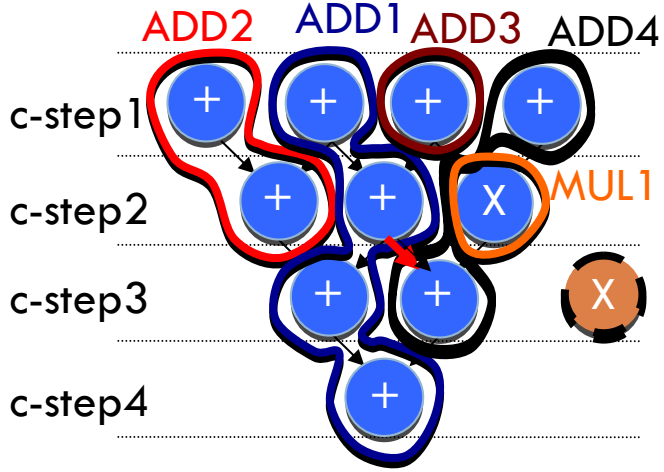
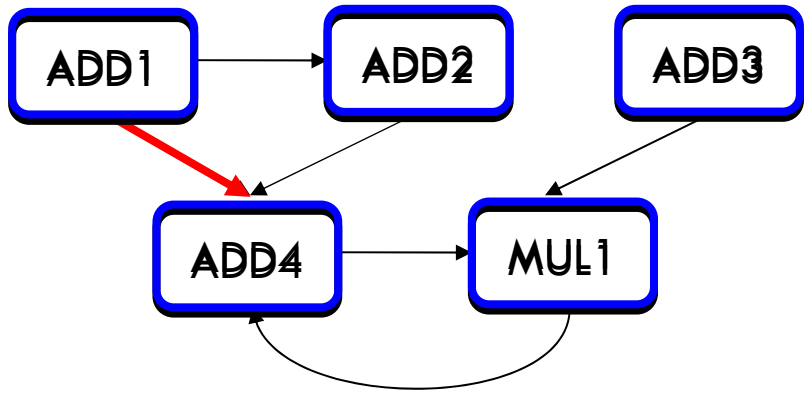
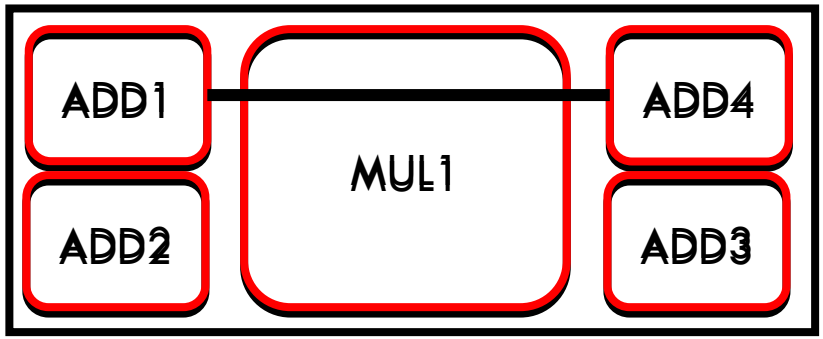
# Motivating Example



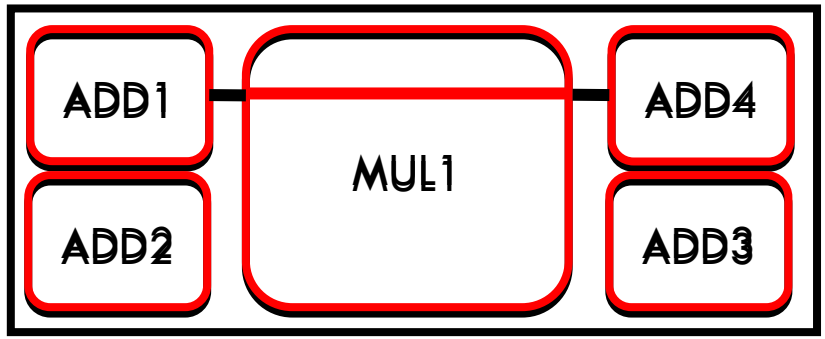

(a)




(b)




(c)




(d)

# Challenges



- How to find idle FUs which reduce wirelength of global interconnects
- How to avoid timing violation

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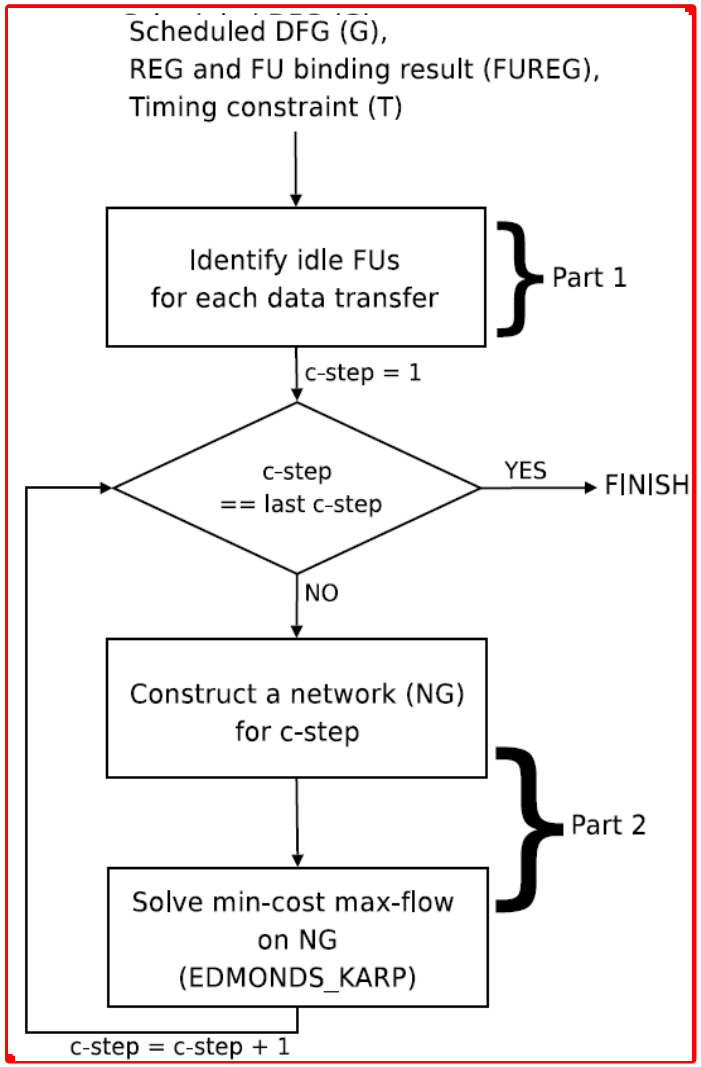
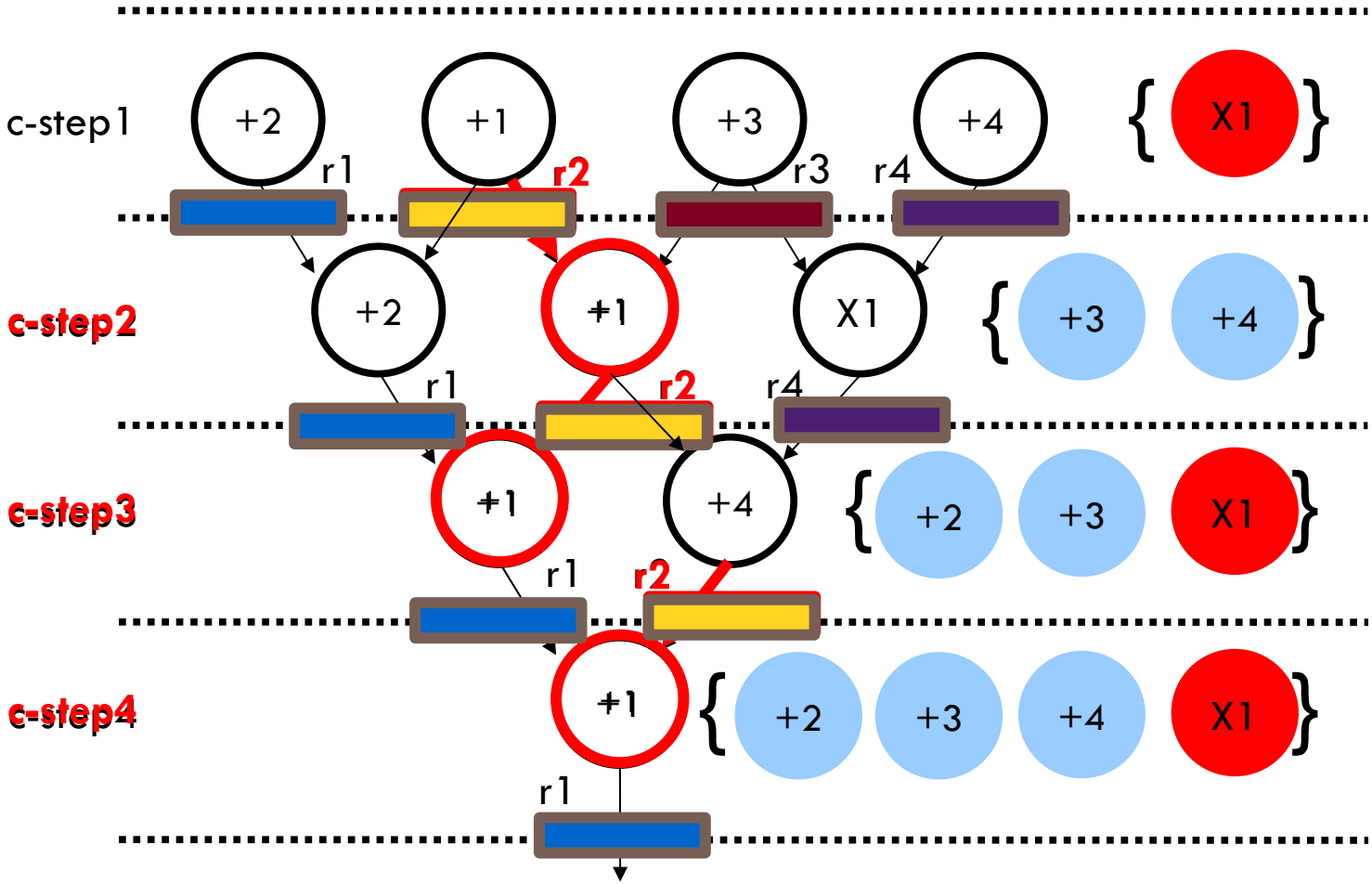
# Our Heuristic





# Part 1 – Identification of Idle FUs





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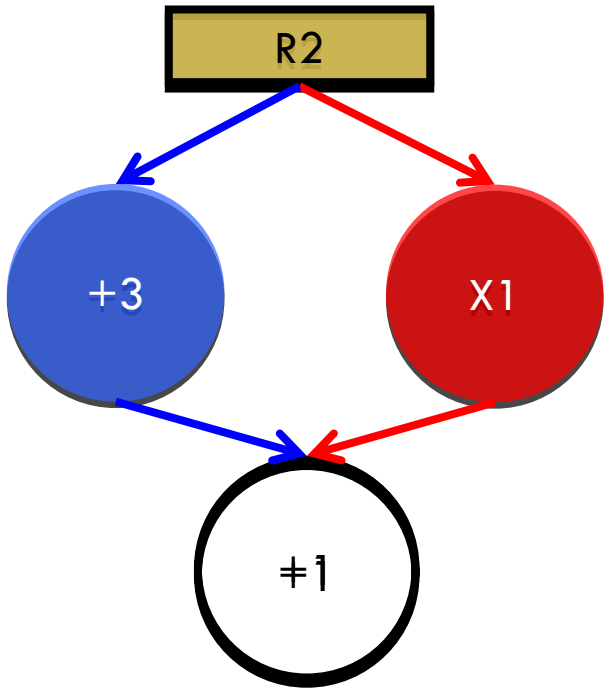

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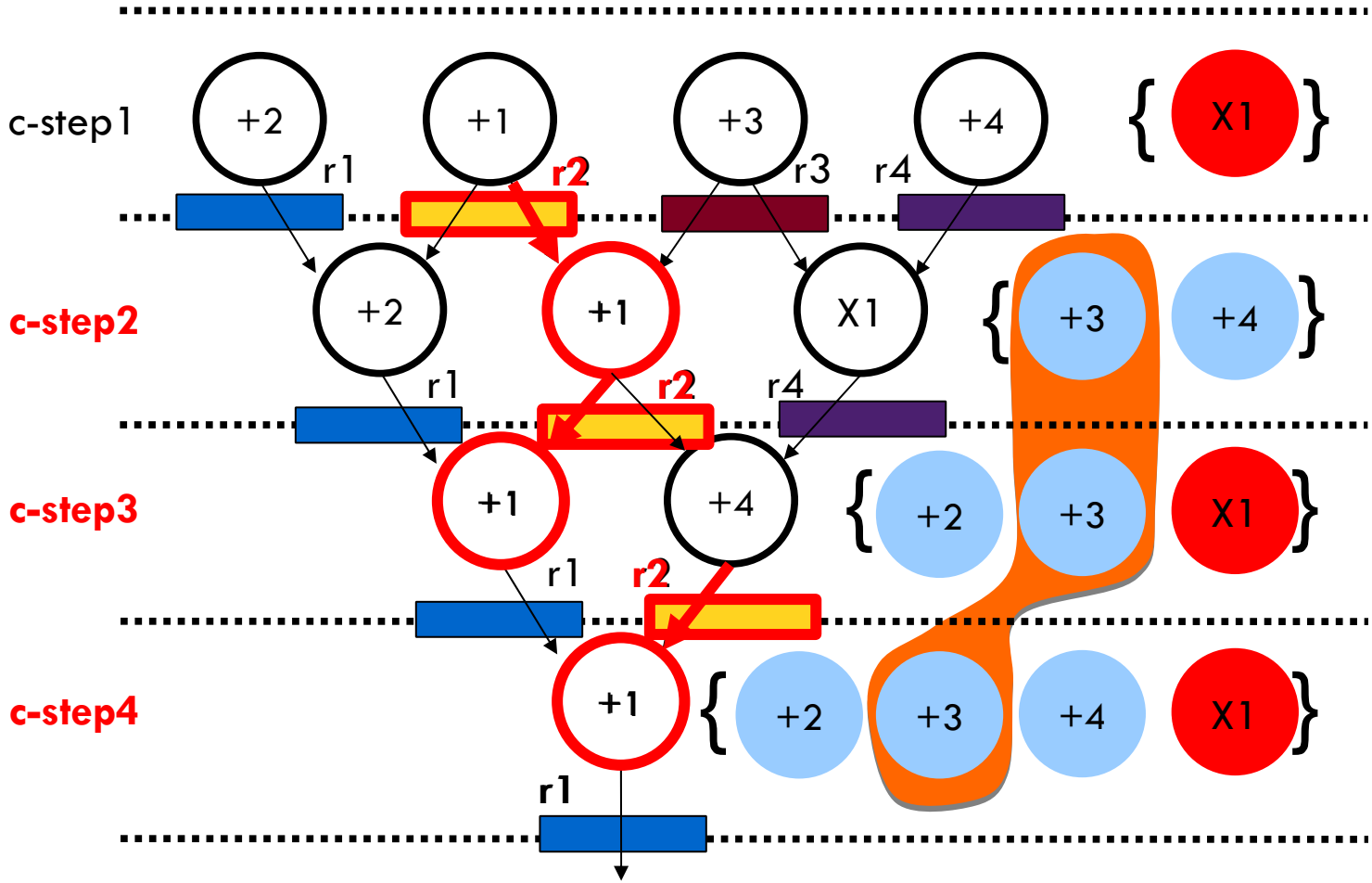
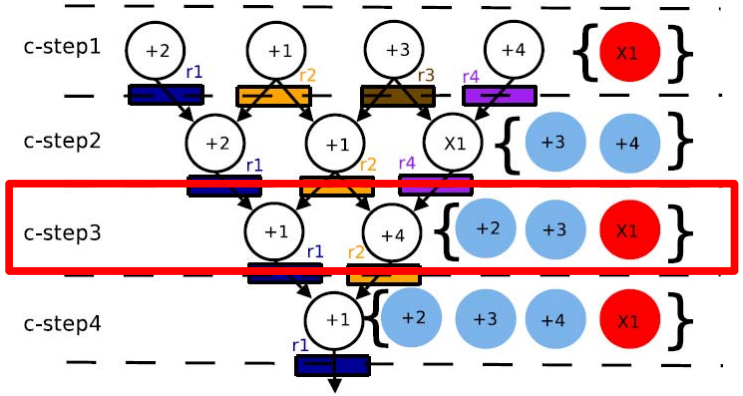


# Part 2 – Interconnect Assignment



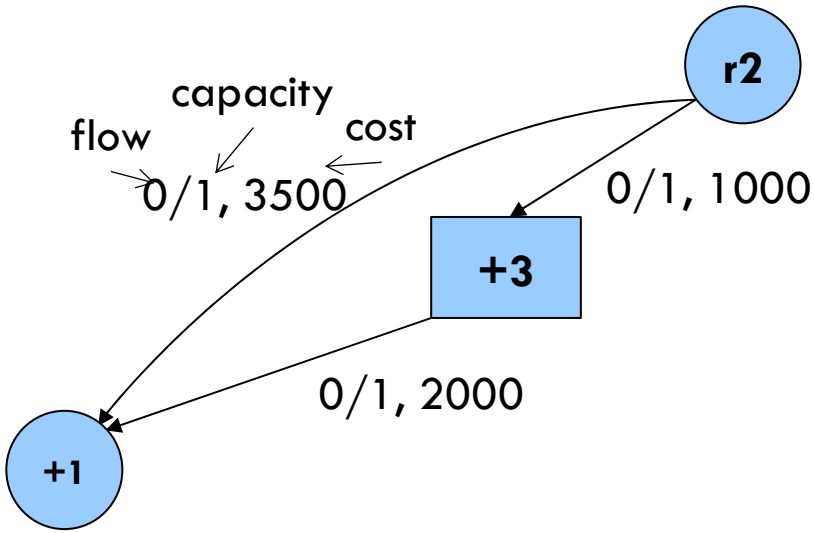
- Challenges
  - How to estimate interconnect length between FUs and registers
    - Use placement information
  - How to choose minimum length interconnects among several possible interconnects
    - Construct a network for data transfers at each c-step

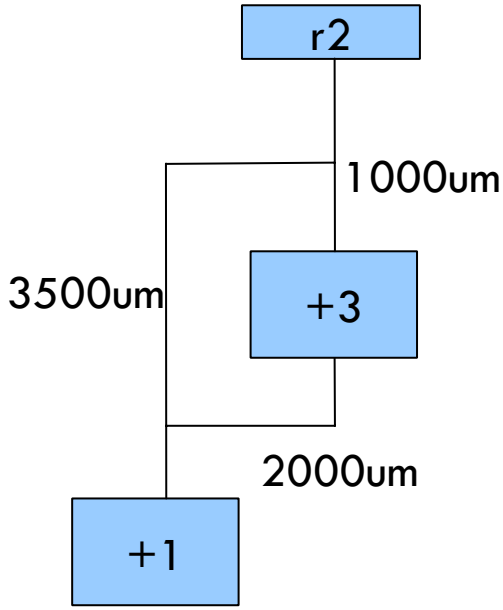


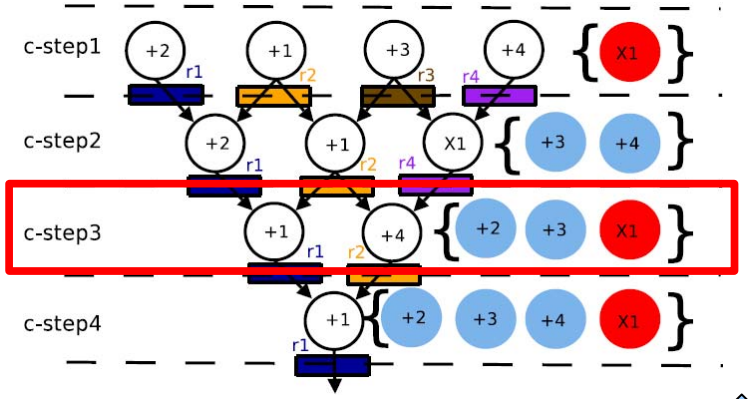

(a) DFG

| Data Transfer | Idle FU |
|---|---|
| r1 -> +1 | +2, +3, X1 |
| **r2 -> +1** | **+3** |
| r2 -> +4 | +2, +3, X1 |
| r4 -> +4 | +2, +3, X1 |

(b) Available idle FUs for each data transfer



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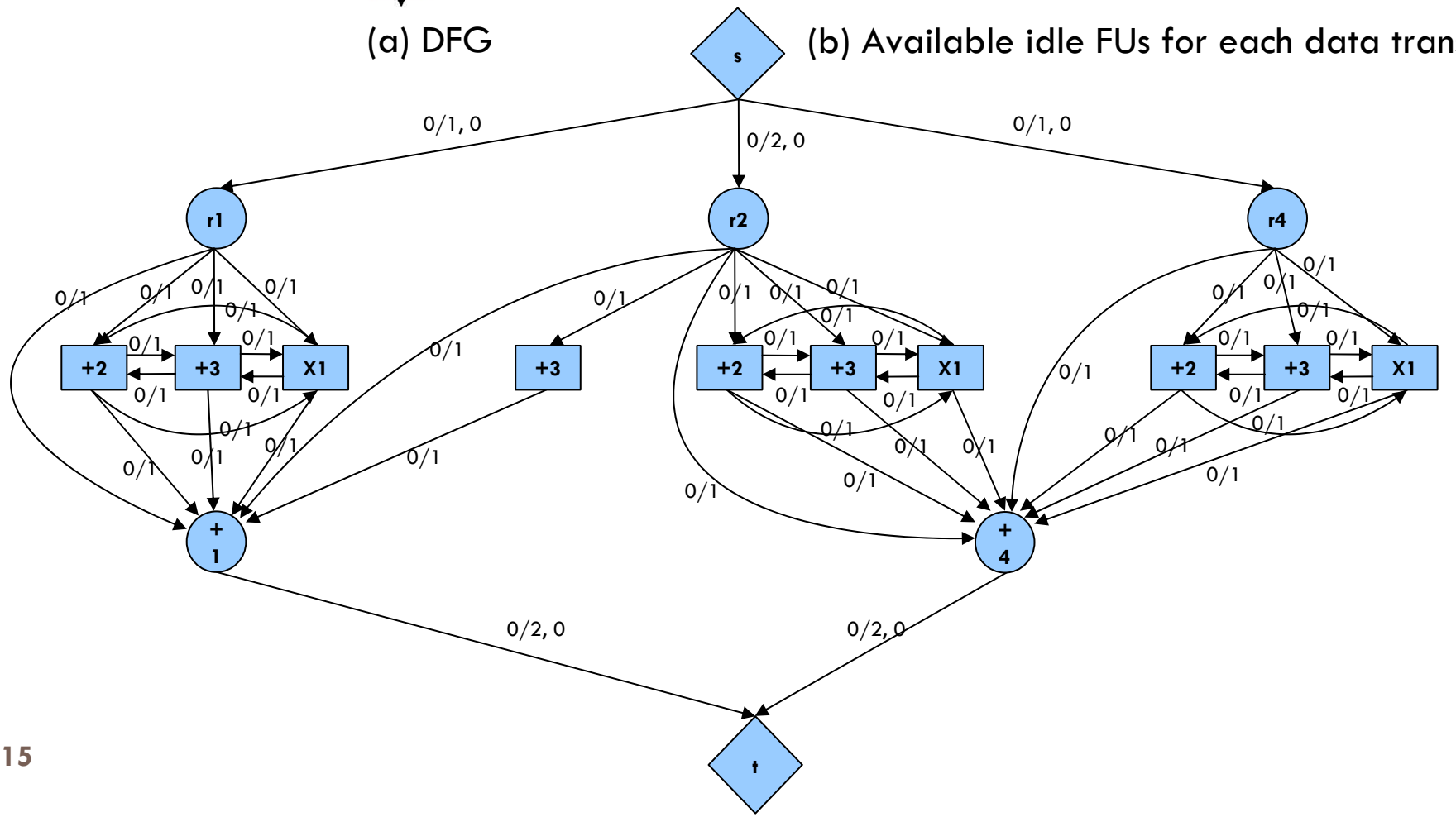
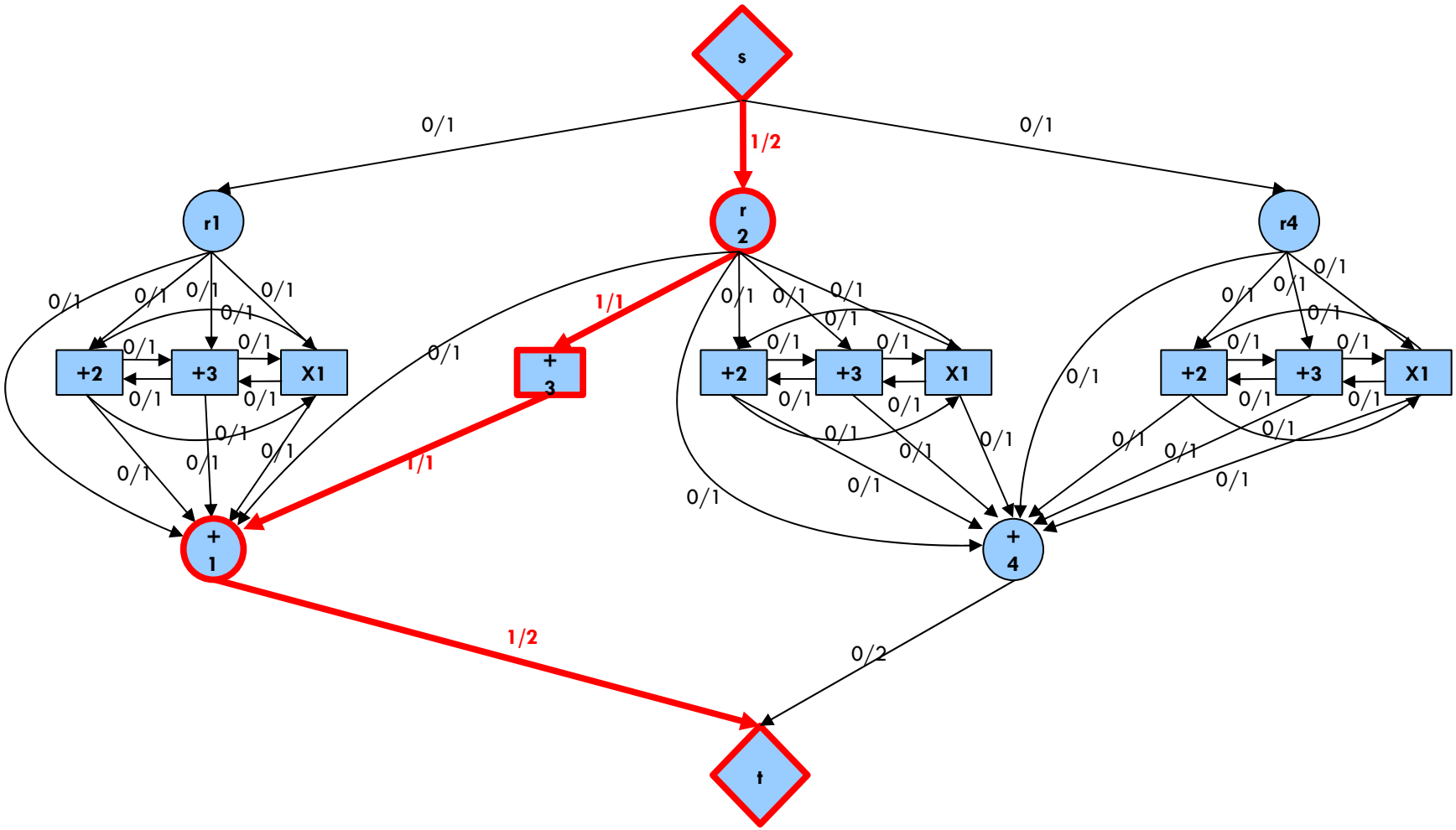
(b) Available idle FUs for each data transfer



# Min-Cost Flow





# Avoiding Timing Violation



- FU takes longer delay than wire
- Avoid timing violation with interconnect optimization

# Avoiding Timing Violation



- Min-cost Max-Flow algorithm
  - Uses shortest path algorithm to find min-cost flow
- Conventional shortest path algorithm
  - Considers only one type of cost
- Modified shortest path algorithm
  - Takes into account timing constraint

# Experimental Setup



- Implemented high level synthesis framework including our interconnect optimization algorithm
- Described in C++
- Used data intensive benchmark programs
- Evaluated the effectiveness with industrial flow
  - Synthesized with Synopsys Design Compiler™
  - Placed and routed with Cadence SOC Encounter™

# Experimental Results



<Total Wirelength After and Before Interconnect Optimization Using Idle FUs>

| **Benchmarks** | Ours | Comp | Ours | BIP | Imp-Comp | Imp-BIP |
|---|---|---|---|---|---|---|
| *chem* | 1.35E+06 | 1.55E+06 | 1.67E+06 | 1.83E+06 | 13% | 9% |
| *honda* | 3.22E+05 | 3.42E+05 | 3.47E+05 | 3.84E+05 | 6% | 10% |
| *dir* | 8.03E+05 | 8.64E+05 | 1.14E+06 | 1.23E+06 | 7% | 7% |
| *feig_dct* | 6.89E+06 | 7.32E+06 | 5.98E+06 | 6.81E+06 | 6% | 12% |
| *lee* | 3.26E+05 | 3.37E+05 | 2.87E+05 | 3.15E+05 | 3% | 9% |
| *mcm* | 8.81E+05 | 9.82E+05 | 1.09E+06 | 1.17E+06 | 10% | 7% |
| *u5ml* | 1.92E+06 | 2.07E+06 | 1.96E+06 | 2.15E+06 | 7% | 9% |
| **AVG** | | | | | 7% | 9% |

Comp : Compatibility path based binding algorithm for interconnect reduction
BIP : Bipartite matching based binding algorithm

# Experimental Results

<Power Consumption After and Before Interconnect Optimization Using Idle FUs>

| **Benchmarks** | Ours | Comp | Ours | BIP | Imp-Comp | Imp-BIP |
|---|---|---|---|---|---|---|
| *chem* | 13.17 | 14.76 | 13.27 | 13.09 | 11% | -1% |
| *honda* | 3.34 | 3.84 | 2.87 | 2.81 | 13% | -2% |
| *dir* | 5.83 | 6.19 | 6.03 | 6.62 | 6% | 9% |
| *feig_dct* | 36.84 | 37.51 | 26.72 | 28.48 | 2% | 6% |
| *lee* | 2.90 | 3.22 | 2.19 | 2.36 | 10% | 7% |
| *mcm* | 7.95 | 8.51 | 5.36 | 5.10 | 7% | -5% |
| *u5ml* | 12.69 | 13.86 | 11.03 | 10.79 | 8% | -2% |
| **AVG** | | | | | 8% | 2% |

# Conclusion

- Proposed a new interconnect reduction algorithm
  - Uses idle FUs as interconnect components
  - Guarantees no timing violation
  - 9 % reduction of total wirelength
  - 5 % reduction of power consumption
- Future Work
  - Include power model to guarantee no power overhead

# Thank you!