Gate Delay Estimation in STA under Dynamic Power Supply Noise

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Overview

- Background & Motivation
- Conventional methods to cope w/ noise on timing
  - Guard-banding based on Static IR-Drop Analysis
  - Gate delay estimation considering noise waveform
- Evaluation of conventional estimation method at 45nm
- Proposed method to improve the estimation accuracy
- Evaluation results of the proposed method
- Conclusion
What is Power/Ground Noise?

Temporal P/G level fluctuation due to simultaneous signal switching.
→ May cause timing failure.

So far, guard-bandning based on static IR-drop analysis.

Recently, dynamic voltage drop analysis tools are introduced.
→ Reduce peak voltage drop by proper placement of decoupling cells.
Technology Trends

- W/ Process technology scaling
  - Current density ↑, Wire resistance ↑
  - Power supply voltage ↓, Non-linearity of voltage-delay characteristics ↑
- Noise amplitude unchanged despite technology scaling
  [A. Mezhiba, IEEE Trans. on VLSI ’04]
  → Concern about timing failure becomes more serious. ↑
Static IR-Drop Analysis and It’s Limitation

Express path delay fluctuation as follows

$$\Delta v_i = \frac{1}{T_i - T_{i-1}} \int_{T_{i-1}}^{T_i} \Delta v \, dt$$

$$\Delta D_{path} = \sum_{i=1}^{n} \Delta D_i = \sum_{i=1}^{n} \frac{\partial D_i}{\partial v} \Delta v_i$$

where $n$: # of stages, $\Delta v(t)$: noise waveform, $D_i$: $i_{th}$ stage delay, $T_i$: arrival time of $i_{th}$ gate output, $\partial D_i/\partial v$: $i_{th}$ stage delay sensitivity to voltage.

Approximate the sensitivity by $m_{th}$ order polynomial and assume uniformity.

$$\frac{\partial D_i}{\partial v} = a_{0i} + \sum_{j=1}^{m} a_{ji} \cdot \Delta v_i^j$$

$$\Delta D_{path} = a_0 \int_{T_0}^{T_n} \Delta v \, dt + O(\Delta v^2)$$

→ Delay estimation by static IR-Drop analysis gives a reasonable approximation, only for setup critical path with insignificant sensitivity difference of each stage.
Conventional Gate Delay Estimation Method

- Gate delay estimation considering noise waveform at 180nm node.
  - Based on Eq. DC voltage approach.
  - Classify the fluctuations into following two cases.
    - Stage delay **increase** in *Current Change Case*
    - Stage delay **decrease** in *Charge Change Case*

→ Evaluate at 45nm node and improve the accuracy if needed.
Review of *Current Change Case*

Corresponds to rising transition under power supply noise.

- Stage delay increase since charging current becomes less.
- Eq. DC voltage is heuristically determined by averaging the noise between 0%-60% period of output waveform at an ideal voltage.

An example of *Current Change Case*  
Averaging interval for Eq. DC voltage
An example of *Current Change Case*

- Corresponds to falling transition under power supply noise.
- Stage delay decreases since output voltage is dropped in prior to the transition.
- Obtain starting voltage from output response to power supply noise.

Obtain output response to the noise.
Use triangular signal as a noise waveform.
- Sweep noise injection time within path timing window to obtain stage delay fluctuations.
- Evaluate the computed results against the SPICE reference.
Evaluation of conventional method at 45nm node

An example circuit of the evaluation.

- **Current Change Case**: X1, X3
  - The **tendencies** of stage delay increase differ from the references.
  - →Need to revise an averaging interval to obtain Eq. DC voltage.

- **Charge Change Case**: X2, X4
  - There exists both **delay increase region** as well as decrease region.
Improve the estimation of *Current Change Case*

Estimate delay increase iteratively

- Conventional method assumes linearity of voltage-delay characteristics and small fluctuation.
- Need to consider non-linearity in recent technologies.
  
  → Iteratively find $T_i$ satisfying $T_i - T_{i-1} = D_i + \Delta D_i$. 

\[
\begin{align*}
T_{i,0} &= T_{i-1} + D_i \\
T_{i,j} &= T_{i,j-1} + \Delta t \\
\Delta V_{i,j} &= \frac{1}{T_{i,j} - T_{i-1}} \int_{T_{i-1}}^{T_{i,j}} \Delta v(t) dt
\end{align*}
\]
Improve the estimation of Charge Change Case

An example of delay increase in Charge Change Case. Delay increase due to NMOS $V_{gs}$ reduction.

- Since PMOS is already OFF, delay increase originates from a temporal NMOS $V_{gs}$ reduction.
- Apply the iterative procedure as well as the Current Change Case with delay sensitivity to gate input voltage instead of supply voltage dependence.
- The stage delay decrease is estimated before the increase is estimated and both cases are considered.
Why was increase in *Charge Change Case* missed?

Stage delay fluctuation of 10 stages inverter chain at 180nm node.

- Stage delay increase in *Charge Change Case* is negligibly small at 180nm node.
- Emerged since noise amplitude and over-drive voltage ($V_{dd} - V_{th}$) become comparable.
Improved estimation results

The estimations are improved considering following factors.
- Non-linearity of voltage-delay characteristics.
- Decrease in over-drive voltage ($V_{dd} - V_{th}$).
Evaluation of proposed method

Circuit conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>$X_i$</td>
<td>INV, NAND2, NOR2</td>
</tr>
<tr>
<td>Drivability</td>
<td>x1, x8</td>
</tr>
<tr>
<td>Cell $V_{th}$</td>
<td>$V_{thL}, V_{thH}$</td>
</tr>
<tr>
<td>$C_{Li}$</td>
<td>[1, 30] (fF)</td>
</tr>
<tr>
<td>#stage (n)</td>
<td>10</td>
</tr>
<tr>
<td>W</td>
<td>$D_{path}/2$</td>
</tr>
<tr>
<td>H</td>
<td>0.2 (V)</td>
</tr>
<tr>
<td>#circuits</td>
<td>100</td>
</tr>
</tbody>
</table>

- Evaluate average error and standard deviation for each randomly-generated circuit.
- Compare averaging voltage within path delay (setup critical case with static-IR-drop analysis), conventional, and proposed.

$error = \frac{\text{Estimated} - \text{Reference}}{\text{Reference}} (\%)$

$\rightarrow (\mu_{\text{error}}, \sigma_{\text{error}})$
Evaluation results

- Delay fluctuation due to noise is 8.2% on average.
- Error is improved to 1.4% by guard-banding of Static IR-Drop.
- Errors of conventional and proposed which consider dynamic noise waveform are 2.0% and 0.61%, respectively.
- New estimation factors need to be considered in recent technologies.

<table>
<thead>
<tr>
<th>Estimation methods</th>
<th>Est. error</th>
<th>$\mu$ (%)</th>
<th>$\sigma$ (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>without noise consideration</td>
<td>8.2</td>
<td>3.4</td>
<td></td>
</tr>
<tr>
<td>Average</td>
<td>1.4</td>
<td>3.3</td>
<td></td>
</tr>
<tr>
<td>Conventional</td>
<td>2.0</td>
<td>5.0</td>
<td></td>
</tr>
<tr>
<td>Proposed</td>
<td>0.61</td>
<td>1.8</td>
<td></td>
</tr>
</tbody>
</table>
Conclusion

- Timing estimation based on static IR-drop analysis gives an optimistic results in the cases where,
  - Short delay path
  - Significant delay sensitivity difference to voltage of each stage.
- Following factors need to be considered in the recent techs. in addition to the conventional method proposed at 180nm node.
  - Non-linearity of voltage-delay characteristics
  - Decrease in over-drive voltage.
- Errors in experimental circuits are reduced from 8% to 2%.
Thank You