Parametric Yield Driven Resource Binding in Behavioral Synthesis Using Multi-Vth/Vdd Library

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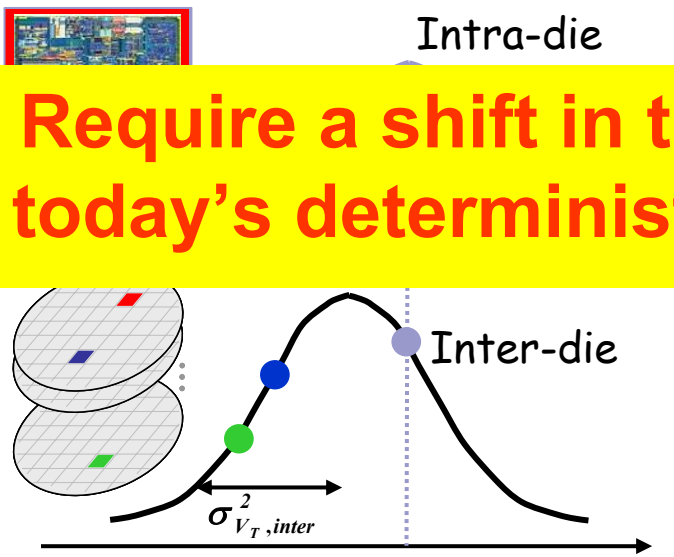
Outline

- Introduction and Motivation
- Multi-Vth/Vdd Library Characterization under PV
- Yield-Driven Resource Binding with Multi-Vth/Vdd
- Experiment Results and Conclusion

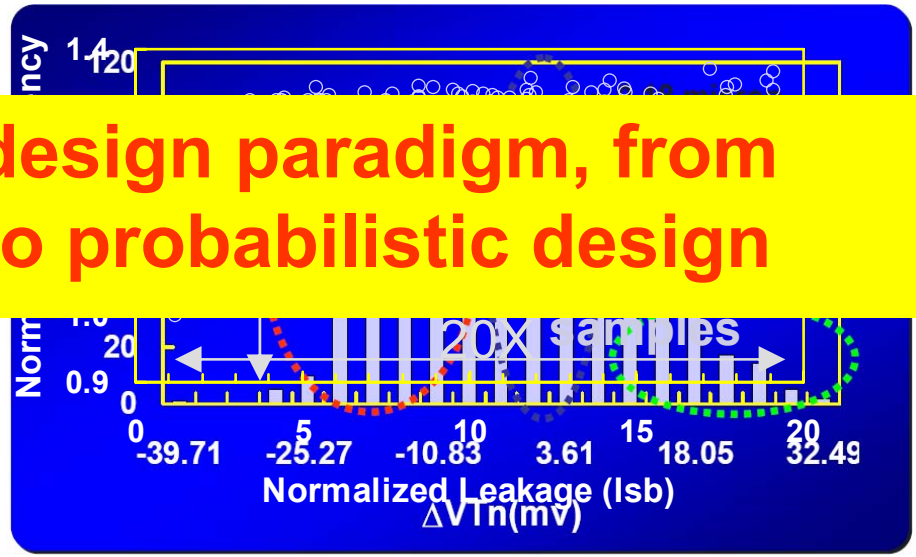
Motivation

- Process variation (PV) has become a prominent concern as technology scales
- Device and interconnect process variations increase with shrinking feature sizes

Require a shift in the design paradigm, from today's deterministic to probabilistic design



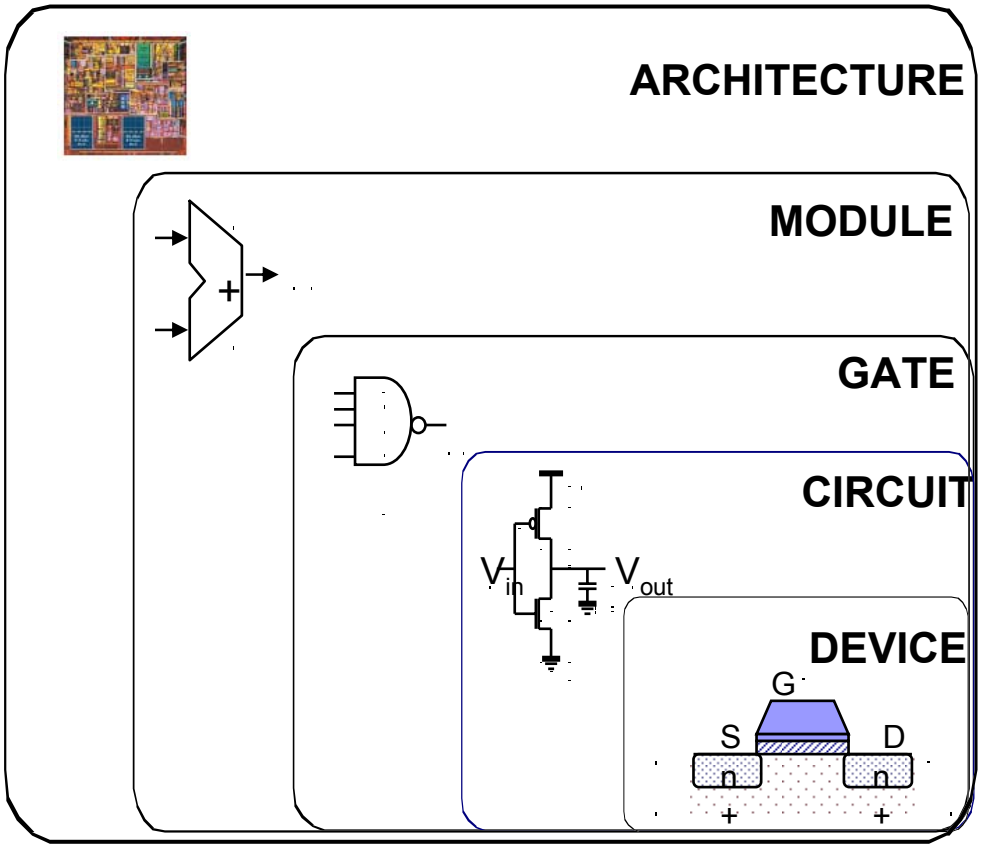
(Source: K. Roy DAC05)



(Source: Intel)

Probabilistic Design Paradigm

- **A holistic design paradigm shift to statistical design**



Variation-aware architecture

Variation-aware
behavioral synthesis

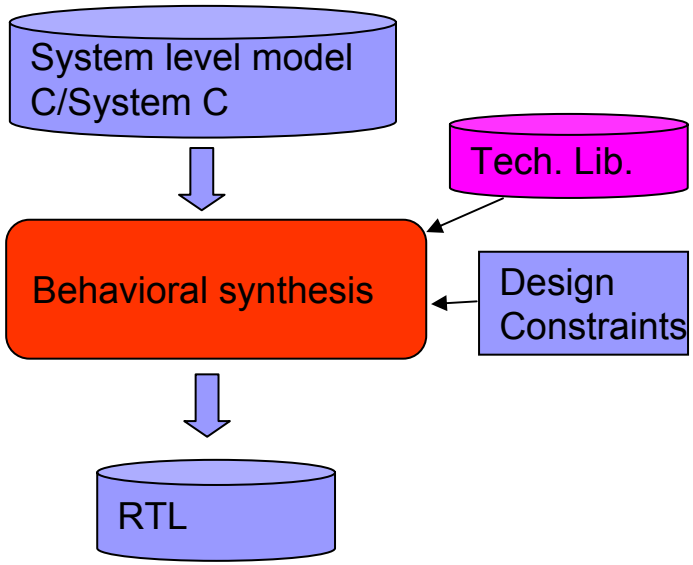
Statistical timing analysis
Statistical gate level optimization
Statistical technology mapping

Process variation modeling

Behavioral Synthesis

- **ESL (Electronic System Level) design methodologies**
  - Move design hierarchy to a higher level
  - Close the gap of productivity and design complexity

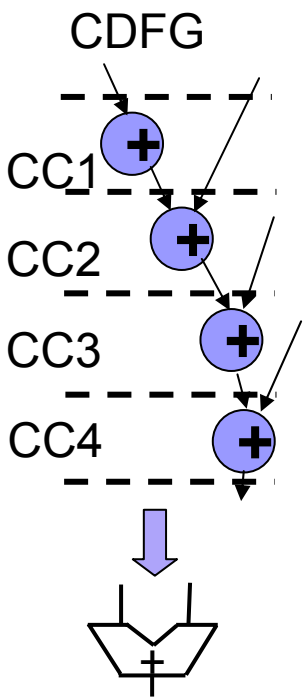
- **Behavioral synthesis (a.k.a. high level synthesis)**
  - Enables an ESL-to-RTL implementation flow
  - Gain a lot of emphasis recently
    - (e.g. workshop @ DAC: HLS-back to the future)
  - Industry success stories:
    - Mentor Graphics: Catapult-C
    - Cadence: C-to-silicon Compiler
    - Forte Design: Synthesizer
    - BlueSpec
    - AutoESL



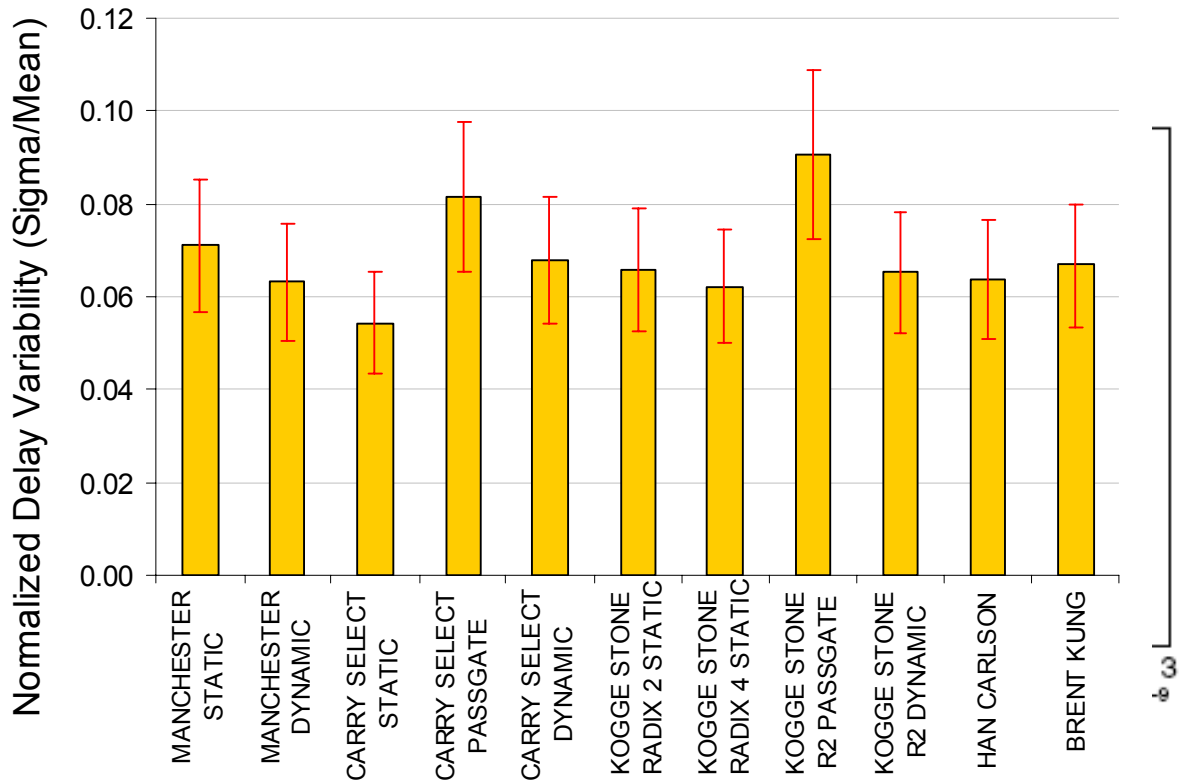
Variation-aware behavioral synthesis is still in its infancy

Variations' Impact on Behavioral Synthesis

- Behavioral synthesis schedules operations at difference clock cycle and maps them to function units (FU)
- Traditionally, each FU has a fixed latency value

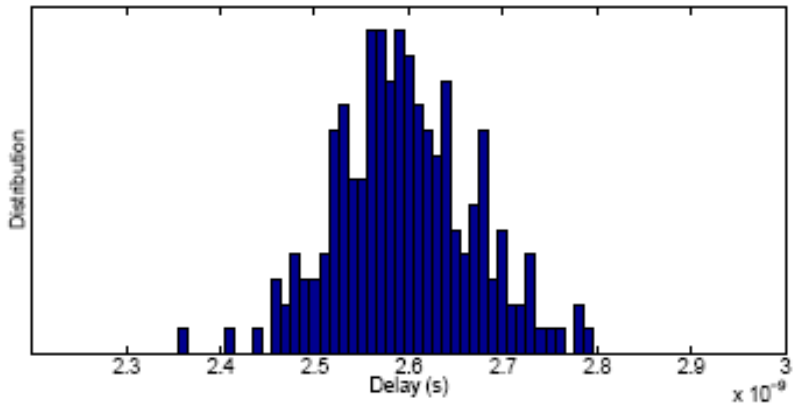


However, under process variation…

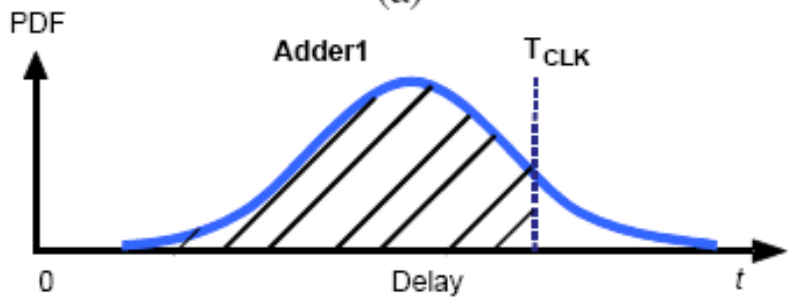


Parametric yield

- The probability that the synthesis hardware meeting a specified constraint



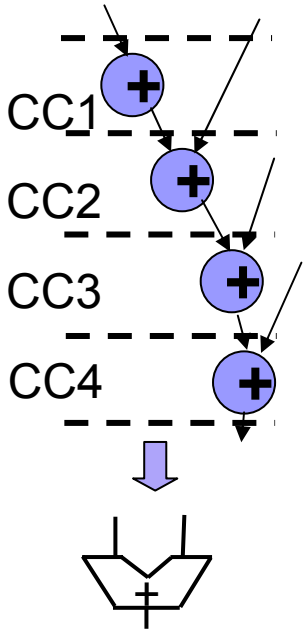
(a)

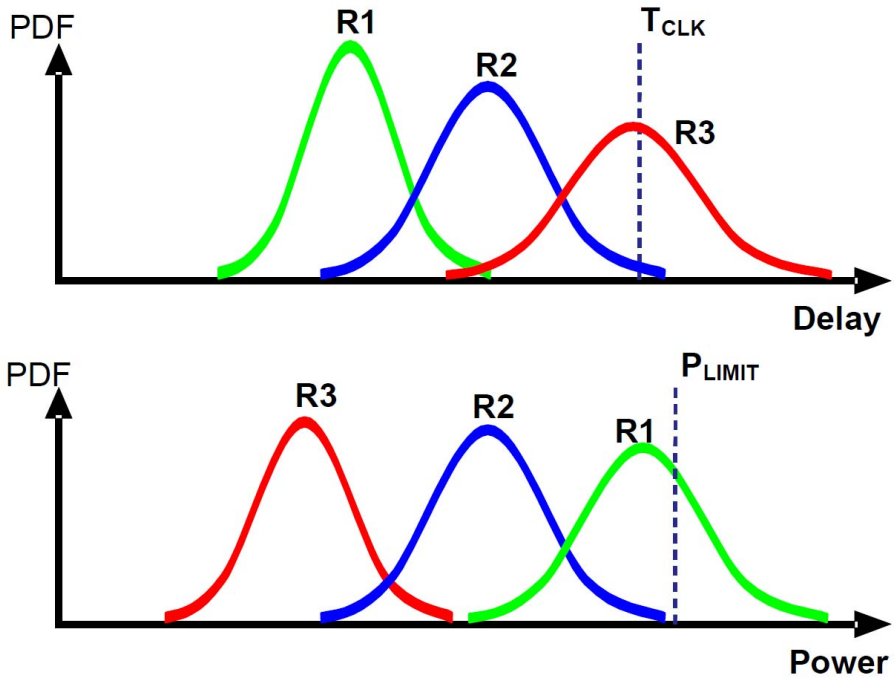


(b)

$$Yield = \int_0^{T_{CLK}} pdf(t)dt$$

Motivation Example





$$Yield = \int_0^T p(t)dt$$

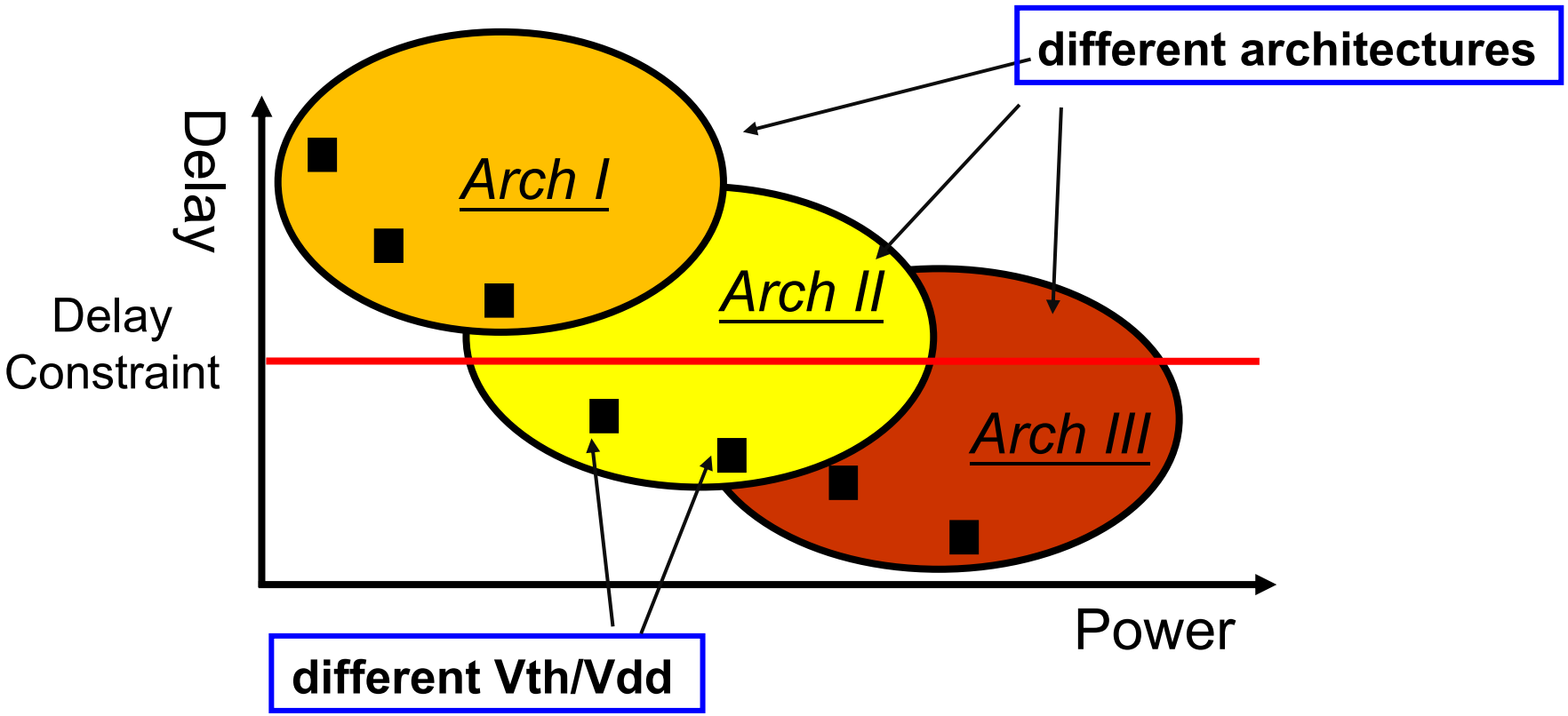
Nominal case analysis: any

Worst case analysis: R1

Variation-aware analysis: R2

Design Space Exploration For Power

- Resource lib: various kinds of multipliers (booth, array, etc) adders (tree, carry-lookahead, etc.) multipurpose units (ALUs, multiplier/divider, etc.)



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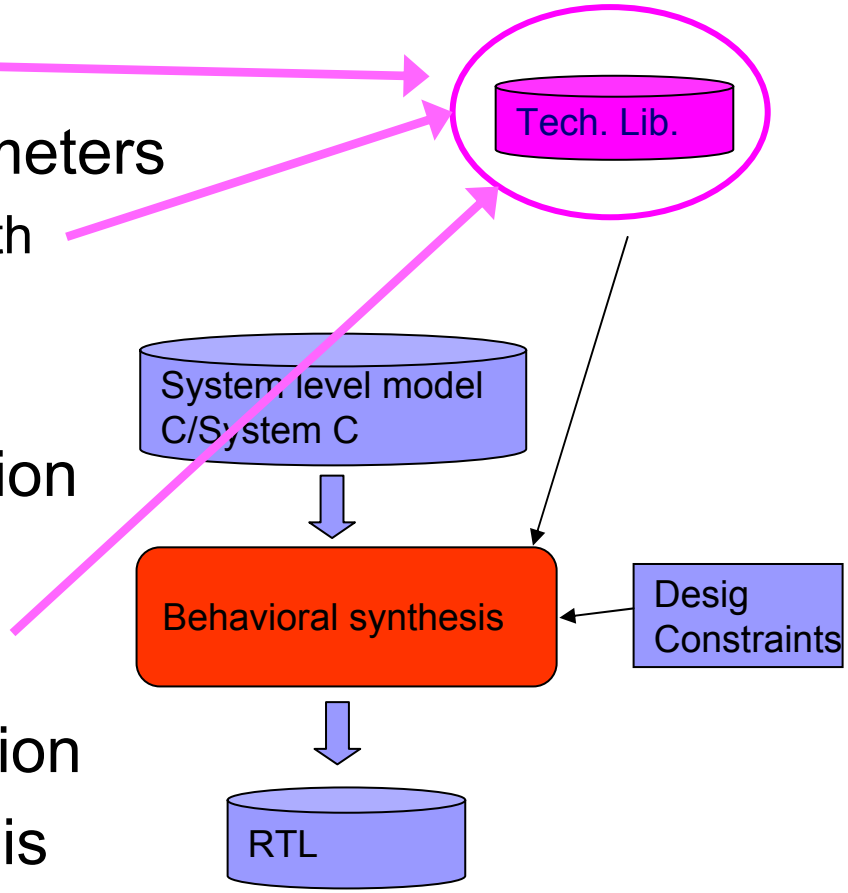
Multi-Vth/Vdd Selection

- Multi-Vth/Vdd in conjunction
  - Effective reduction in both dynamic and static power
- Combination of dual-Vth and dual-Vdd
  - 4 “Corners” of dual-Vth and dual-Vdd
- multi-Vth/Vdd applied at function unit level

PV-aware Library Characterization

- Based on 45nm technology
  - Multi-Vdd/Vth Settings
  - Variations on Device Parameters
    - Gate Length, Metal Line Width
    - Gate Oxide Thickness
- Statistical timing characterization
  - Synopsys PrimeTime VX
- Statistical power characterization
  - Hspice Monte Carlo Analysis



Timing Characterization Results

2 Adder Designs →		Delay : Kogge16		Delay : Bkung16	
Case	Power	Mean (μ)	Deviation (σ)	Mean (μ)	Deviation (σ)
Nominal	Medium	3.26417	0.07934	3.46797	0.17013
High-Vth	Low	3.66011	0.09215	3.89041	0.19547
Low-Vdd	Low	4.22523	0.11554	4.49699	0.24630

- High-Vth/low-Vdd leads to larger variations
- Different design implementations have different variations

Power Characterization Results

- Statistical power characterization of FUs
  - Library cells' leakage power characterized by Hspice Monte Carlo analysis
  - Leakage power distribution of FUs computed by summing library cells' leakage power distributions

Name of FU	Leakage Power	
	μ (nW)	σ (nW)
Bkung	3626.612	85.739
Kogge	5007.009	94.330
Pmult	4982.431	91.697
Booth	15523.711	205.399
Mux21	383.314	24.089

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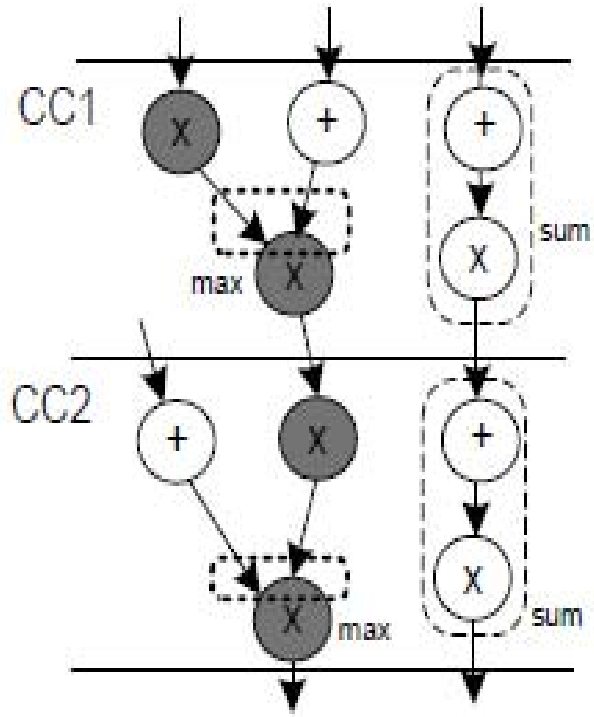
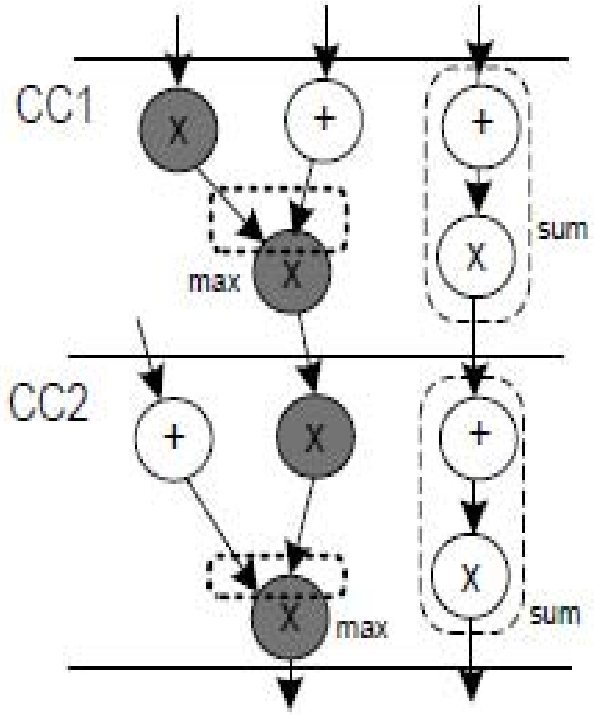
PV-Aware Resource Sharing/Binding

- This work focuses on Resource Binding/Sharing
  - Scheduling already taken place
  - Control/Data-path structure available
  - **Sharing and binding of the type of functional units is up to optimization**



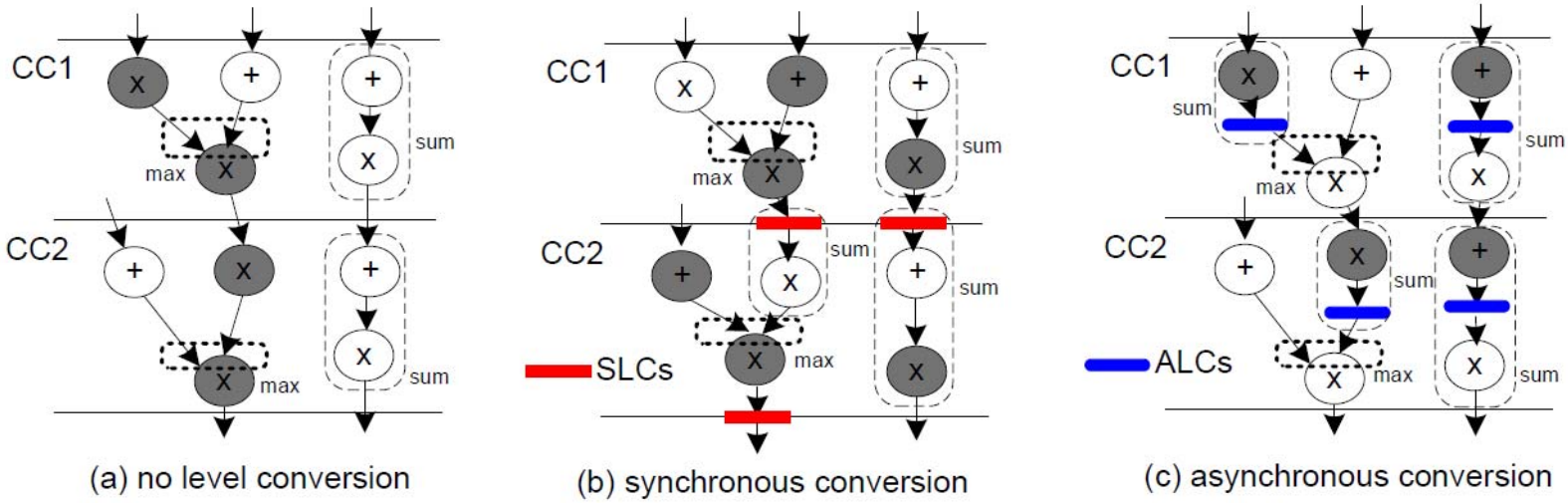
Parametric Yield Analysis for DFGs

- Need two atomic functions sum(A,B) and max(A,B):
  - Sum(A,B) is easy to perform
    - If both A, B are Gaussian, sum(A,B) is Gaussian:
      - $\mu = \mu_A + \mu_B$
      - $\sigma = (\sigma_A^2 + \sigma_B^2 - 2\rho\sigma_A\sigma_B)^{1/2}$
      - where ρ is the correlation coefficient between A and B
  - Max(A,B) is quite complex to compute
    - Tightness probability techniques are used to facilitate the computation of the max function



Voltage-Level Conversion for Yield

- Level Conversion needed with low-Vdd units driving high-Vdd units
- Asynchronous conversion allows passing slacks and helps improve timing yield



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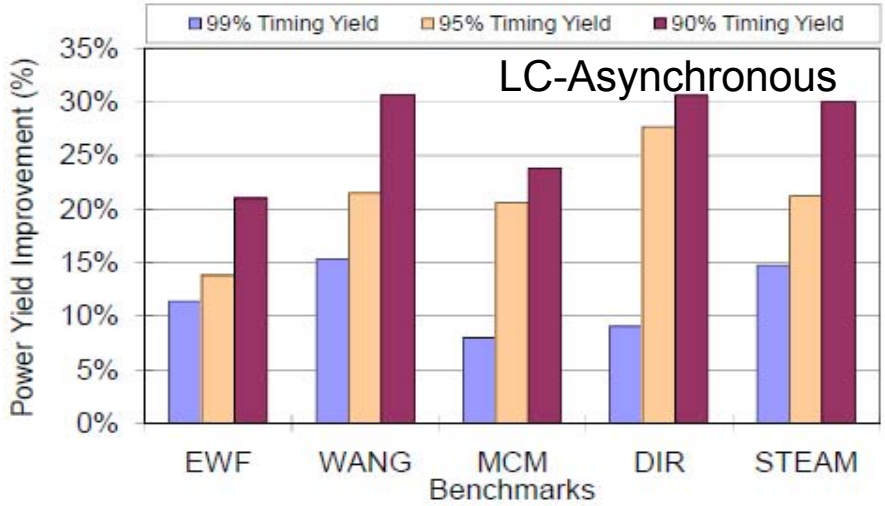
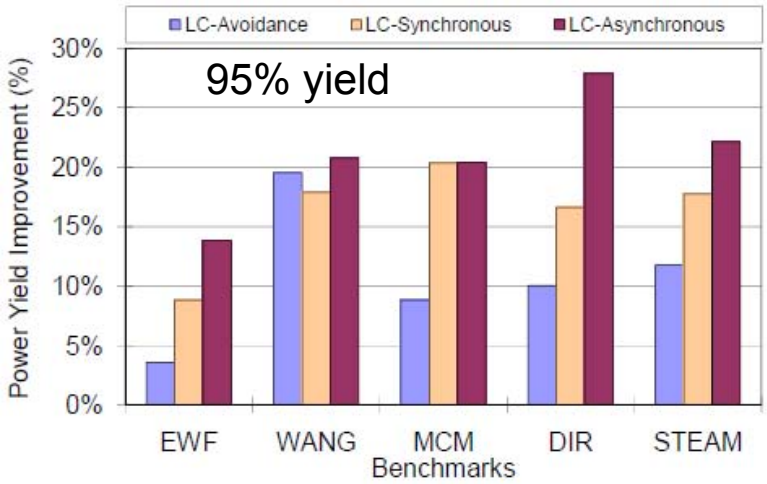
Variation Aware Resource Sharing/Binding

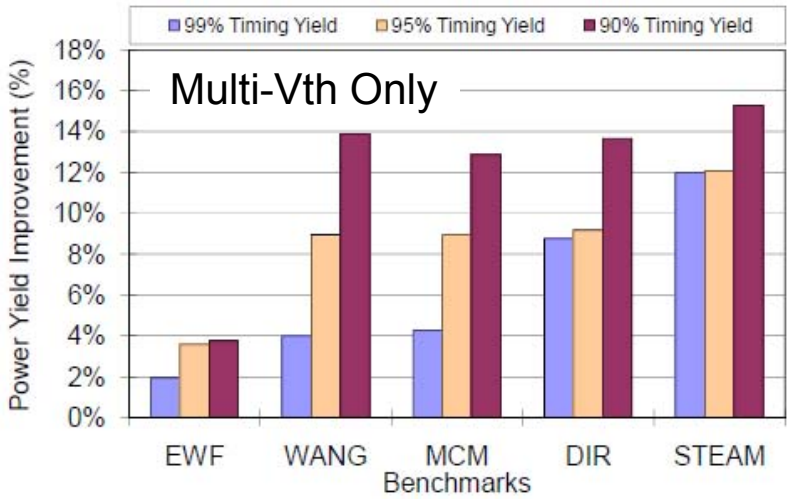
- Given
  - Scheduled CDFG
  - Design constrains
    - Clock period / Timing yield constraint
    - Technology library with variation
- Perform sharing/binding:
  - Determine how operations are assigned to and shared between resources
  - Minimize power without violating timing yield

Power yield improvement with joint multi-Vth/Vdd

- average power reduction of 21% with 95% timing yield constraint







Conclusion

- As technology scales, process variation has increasing impact on performance and power variations
- Multi-Vth/Vdd techniques are used for design space exploration
- We propose a statistical behavioral synthesis framework for multi-Vdd/Vth design
- Significant power reduction can be achieved with the proposed variation-aware framework