A Practice of ESL Verification Methodology

from SystemC to FPGA – Using

EPC Class-1 Generation-2 RFID Tag Design as An Example

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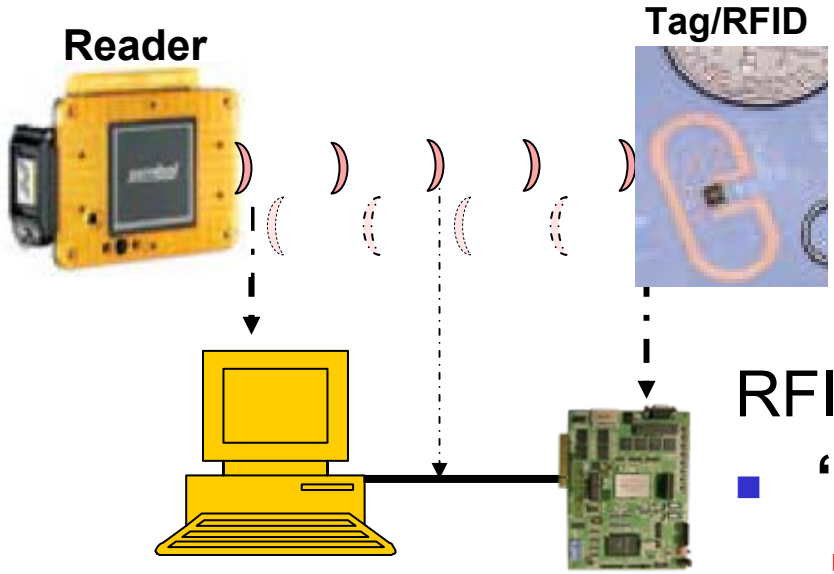
Outline

- RFID System Design Challenges
- ESL Design Flow
- ESL Design Verification Results
- Summary and Future Work
- Q&A

RFID System Design Challenges



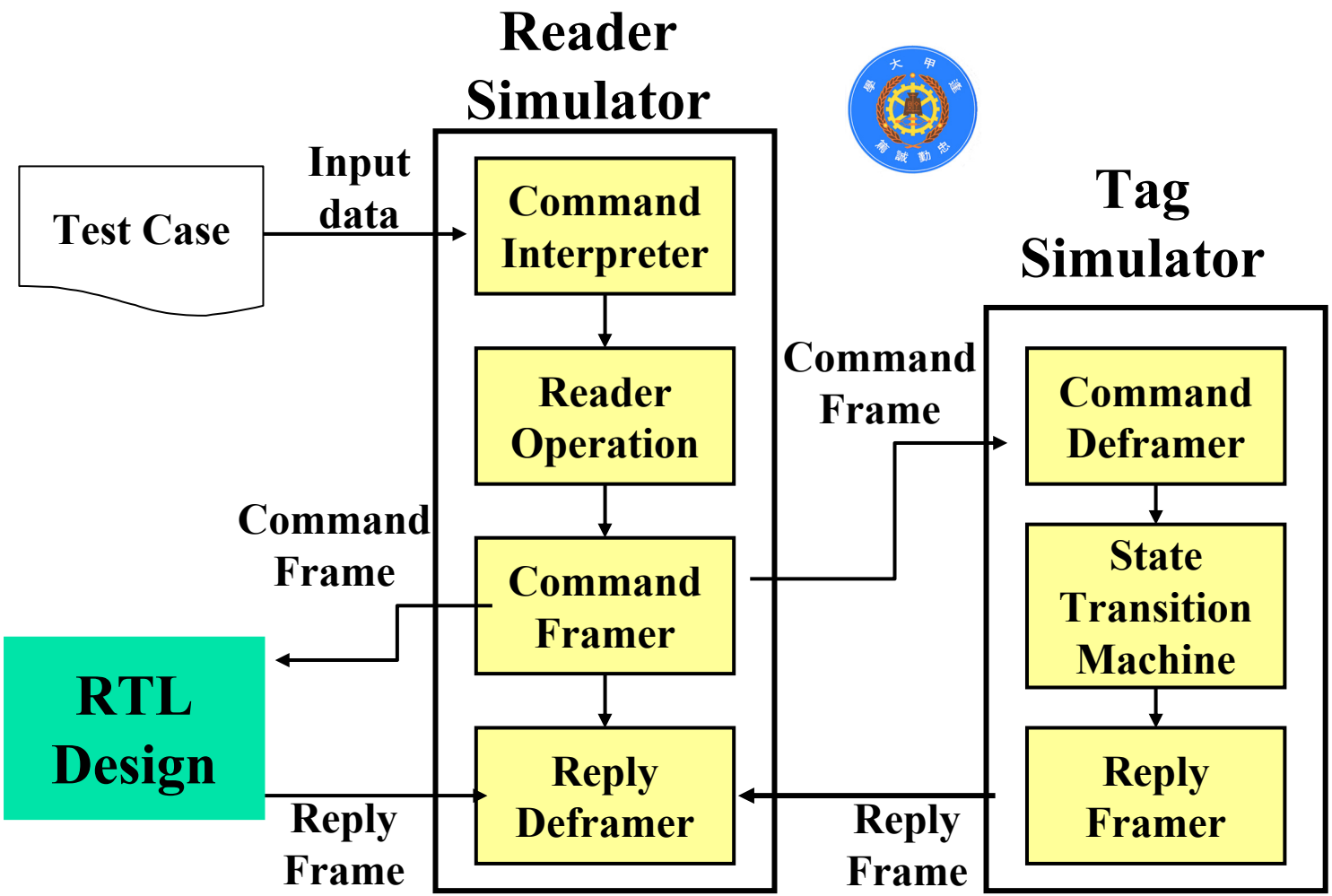
System Design Needs

- **Reader - Simulator**
- **Data Transfer**
- **Tag – Simulator**

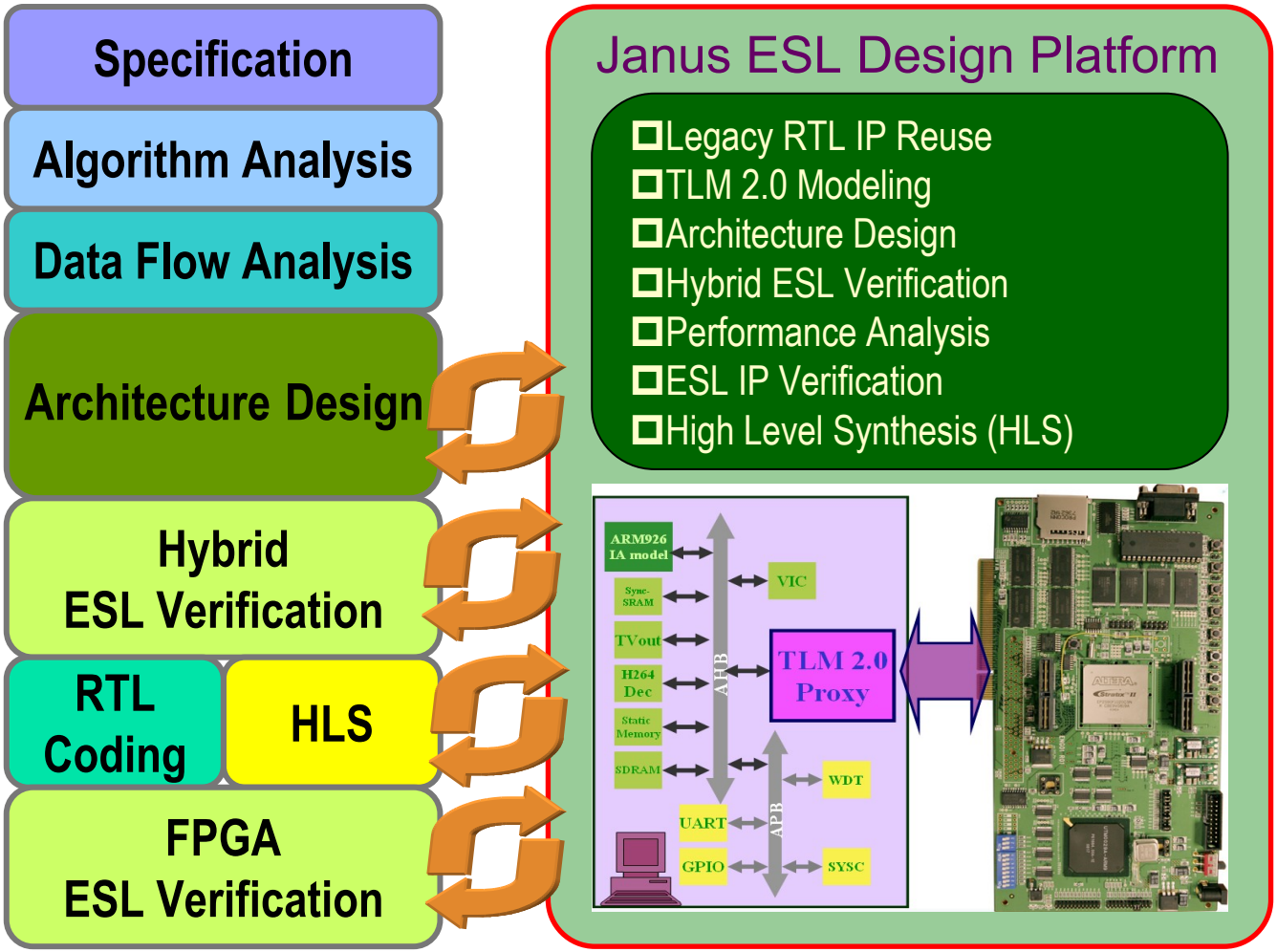
RFID IC Architecture

- **'STD' - IP**
  - STD Cell
  - Memory (MTP)
- **Customized - IP**
  - Digital
    - PHY/Codec
    - Protocol Engine
  - PMU
  - RF Transceiver

RFID System Design (C++)



ESL Design Flow



ESL Design Verification

TSMC RFID C++ Reader/Tag Models

RFID C++ Reader & Test Harness

RFI C++ Tag

TAG RTL

=

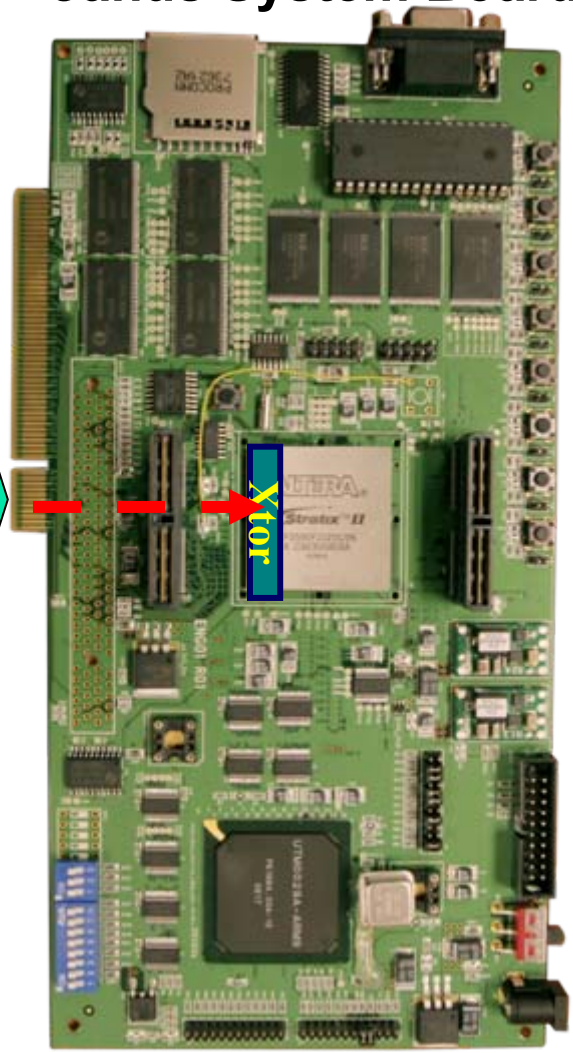
TLM 2.0 Proxy

PCI I/F

Xtor

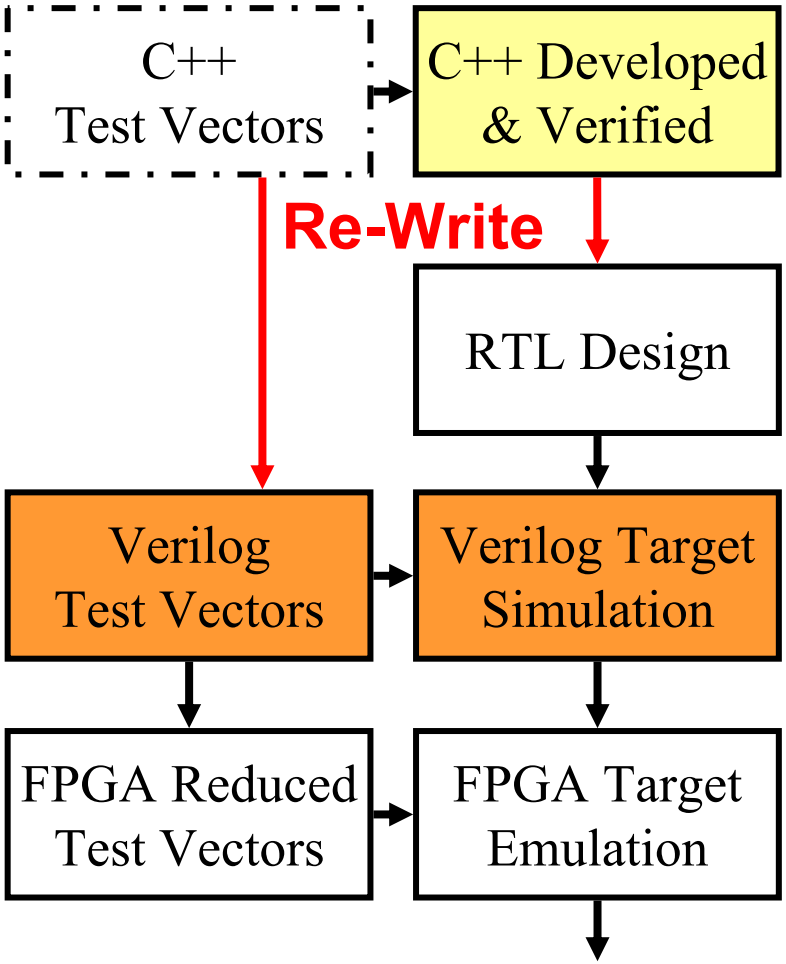
A 200 X Faster Regression Test than RTL Simulation

Janus System Board

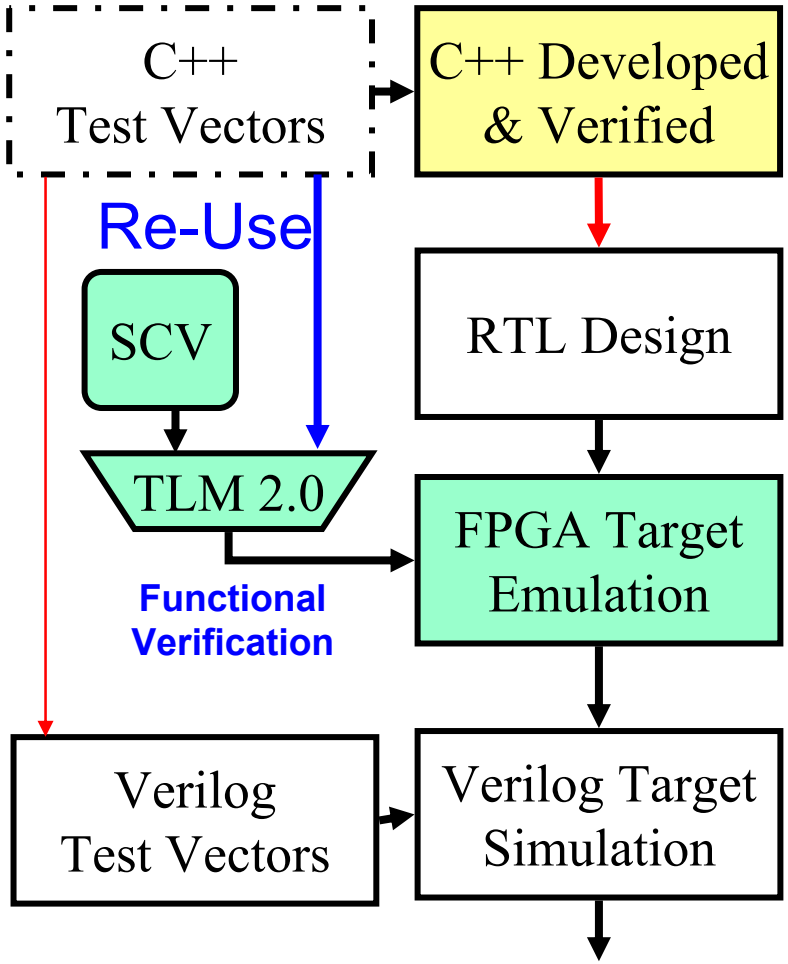


ESL Verification Flow

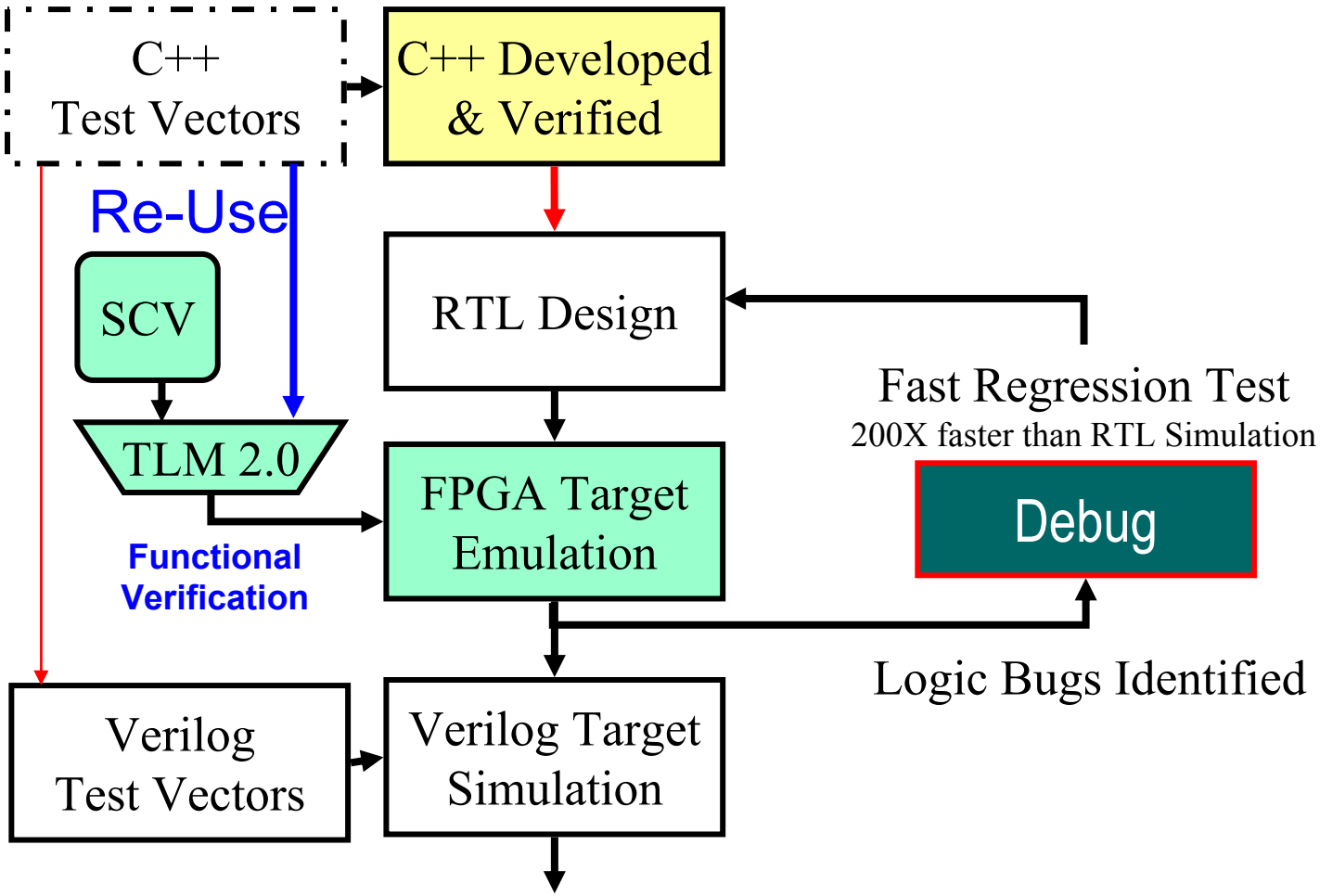
- Conventional



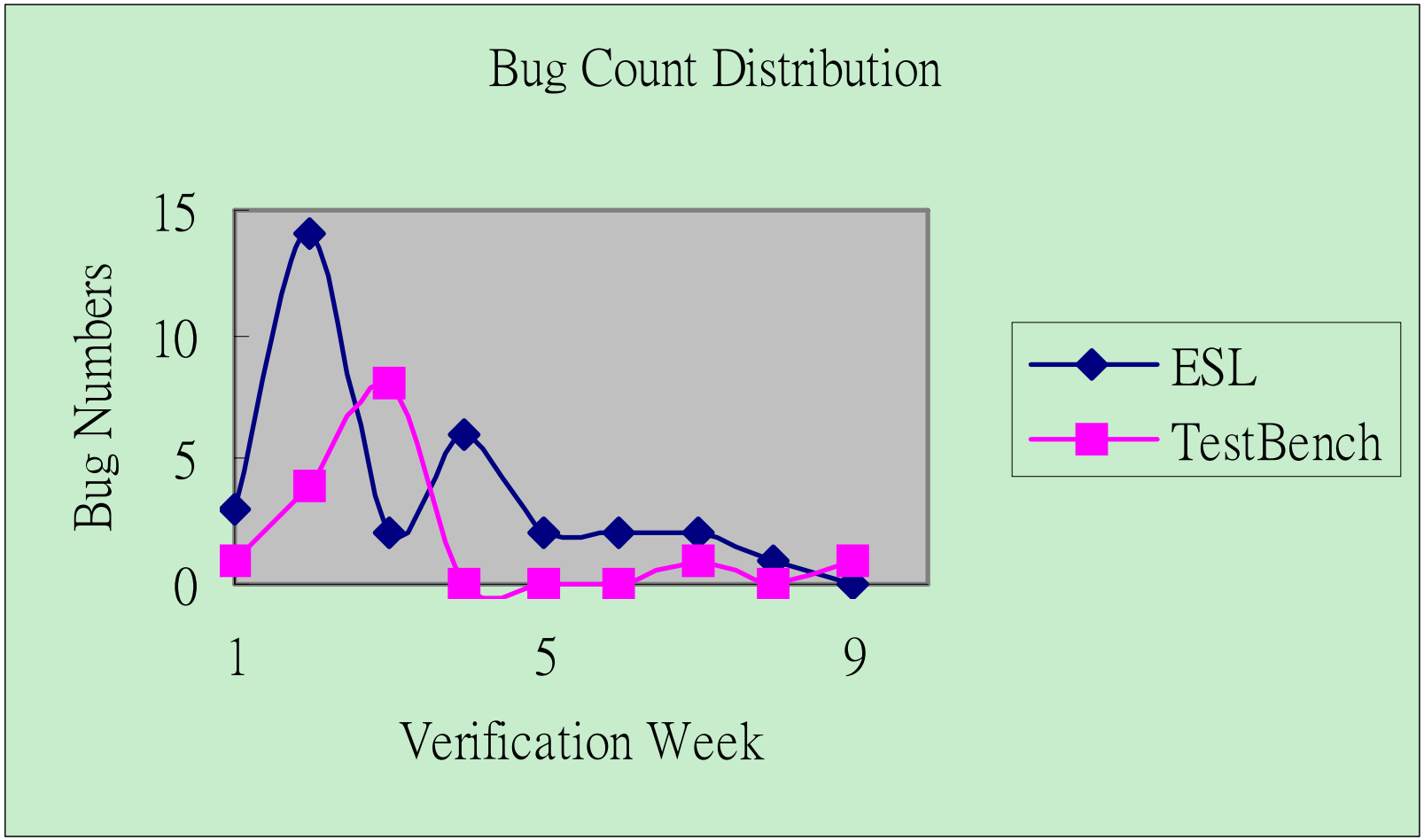
- Co-Emulation



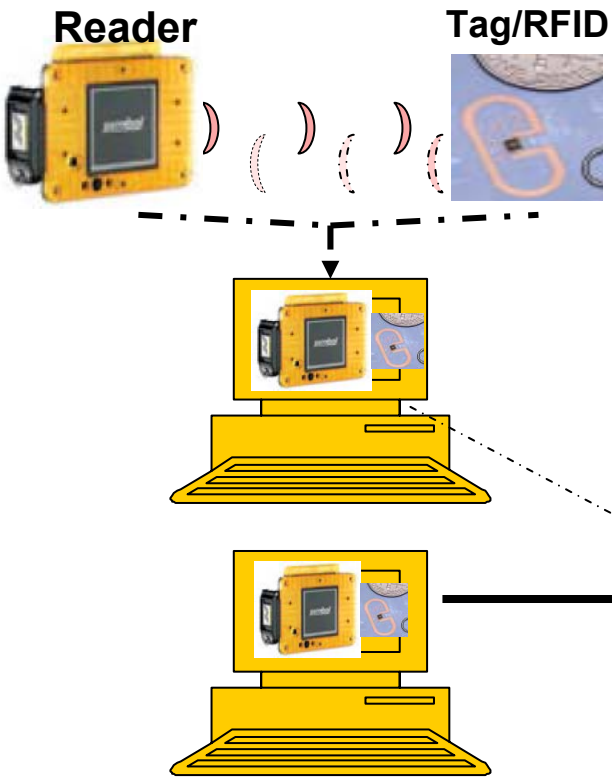
ESL Design on RTL



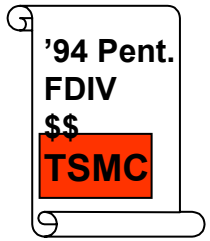
ESL Design Verification Efficieny



Summary - ESL Design Flow on RFID



1. C++ Reader-Tag Simulator **per STD**
2. Test-suites



3. **ESL/IC Verification**

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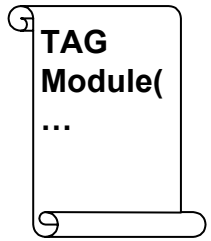
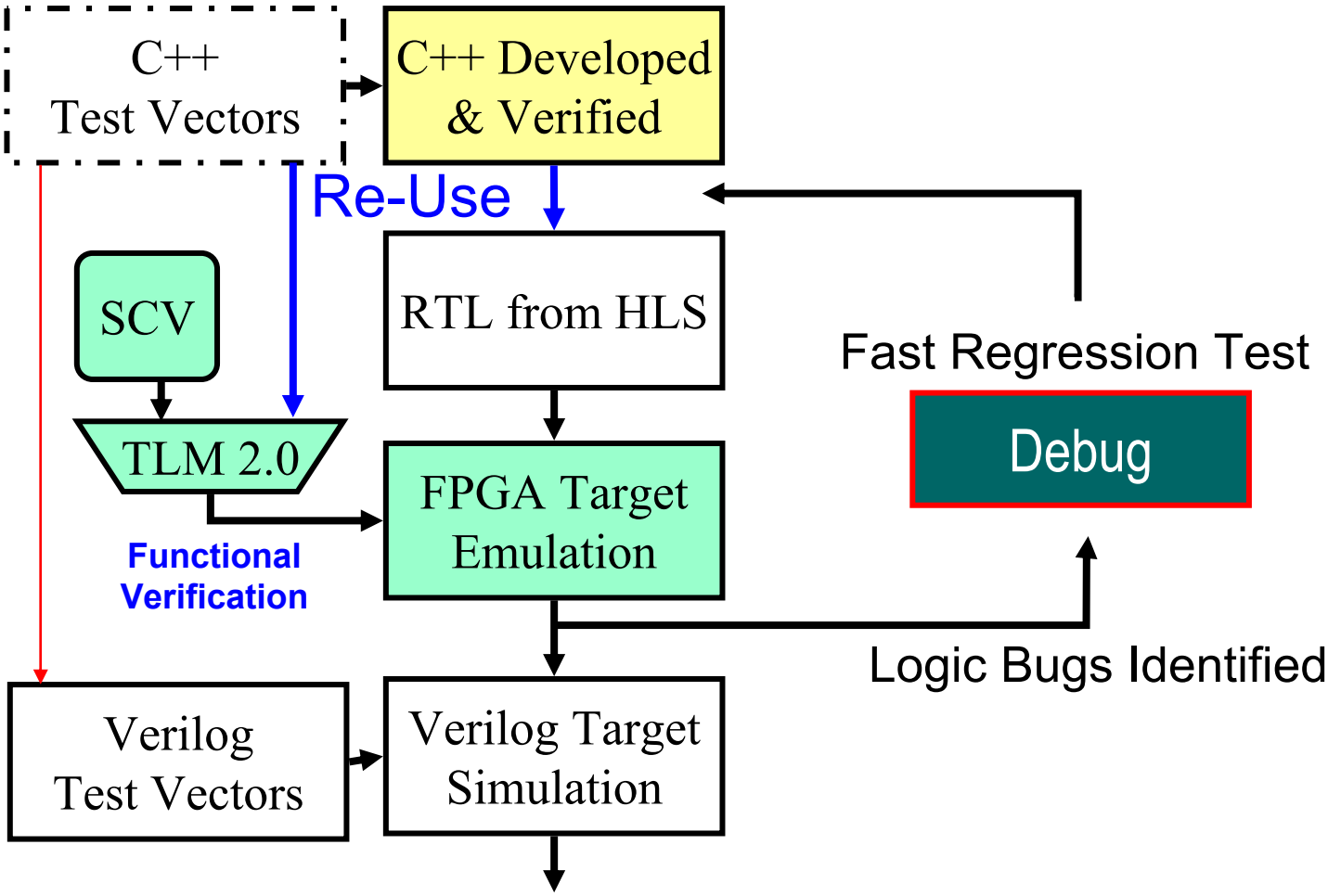
4. **IC Design**



5. **Customized Tester**

Future work :
ESL w. High Level Synthesis



Q & A