A Practice of ESL Verification Methodology
from SystemC to FPGA – Using EPC Class-1 Generation-2 RFID Tag Design as An Example

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Outline

- RFID System Design Challenges
- ESL Design Flow
- ESL Design Verification Results
- Summary and Future Work
- Q&A
RFID System Design Challenges

System Design Needs
- Reader - Simulator
- Data Transfer
- Tag – Simulator

RFID IC Architecture
- ‘STD’ - IP
  - STD Cell
  - Memory (MTP)
- Customized - IP
  - Digital
    - PHY/Codec
    - Protocol Engine
  - PMU
  - RF Transceiver
ESL Design Flow

Janus ESL Design Platform
- Legacy RTL IP Reuse
- TLM 2.0 Modeling
- Architecture Design
- Hybrid ESL Verification
- Performance Analysis
- ESL IP Verification
- High Level Synthesis (HLS)
ESL Design Verification

TSMC RFID C++ Reader/Tag Models

RFID C++ Reader & Test Harness

RFID C++ Tag

TAG RTL

Proxy

TLM 2.0

PCI I/F

Janus System Board

A 200 X Faster Regression Test than RTL Simulation
**ESL Verification Flow**

- **Conventional**
  - C++ Test Vectors
  - Re-Write
  - RTL Design
  - Verilog Test Vectors
  - FPGA Reduced Test Vectors
  - FPGA Target Emulation

- **Co-Emulation**
  - C++ Test Vectors
  - Re-Use
  - SCV
  - TLM 2.0
  - Functional Verification
  - FPGA Reduced Test Vectors
  - FPGA Target Emulation
  - Verilog Test Vectors
  - Verilog Target Simulation
ESL Design on RTL

- C++ Developed & Verified
- RTL Design
- FPGA Target Emulation
- Verilog Target Simulation
- Fast Regression Test: 200X faster than RTL Simulation
- Debug
- Logic Bugs Identified
- Re-Use
  - SCV
  - TLM 2.0
- Functional Verification
- C++ Test Vectors
  - Verilog Test Vectors
  - Verilog Target Simulation
  - Functional Verification
  - C++ Developed & Verified
ESL Design Verification Efficiency

Bug Count Distribution

Verification Week

Bug Numbers

ESL
TestBench
Summary - ESL Design Flow on RFID

1. C++ Reader-Tag Simulator per STD
2. Test-suites
3. ESL/IC Verification
4. IC Design
5. Customized Tester
Future work:

ESL w. High Level Synthesis

- Logic Bugs Identified
- Debug
- Fast Regression Test
- RTL from HLS
- FPGA Target
- Emulation
- C++ Developed & Verified
- C++ Test Vectors
- SCV
- TLM 2.0
- Functional Verification
- Verilog Test Vectors
- Verilog Target Simulation
- Debug
- Logic Bugs Identified
- Re-Use
- Verilog Target Simulation
- Verilog Target Simulation
- Functional Verification
- Verilog Test Vectors
- SCV
- TLM 2.0
- C++ Test Vectors
- C++ Developed & Verified
Q & A