A H.264/MPEG-2 Dual Mode Video Decoder Chip Supporting Temporal/Spatial Scalable Video

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Introduction – Motivation

Dual Mode Video Decoder (H.264 HP/MPEG-2 MP)
Supporting Temporal/Spatial Scalable Video (SBP mode 0)
Proposed Design – System Architecture

- RISC (H.264/SVC/MPEG-2 Decoding Control)
- External Memory
  - Reordered Frame
  - Prediction Data
  - Bitstream
  - Display Frame

- AMBA Slave IF
- System Controller
  - System Reg File
- AMBA Master IF
  - Master Arbiter
  - Prediction Data Cache Buffer
    - (Upper MB)

- VLD
  - Coeff. Data FIFO
- CAVLD
  - CABAD
    - Left MB Info
- MPEG-2
  - 8x8 IQ/IT
  - 4x4/8x8 IQ/IT
- H.264/SVC
  - 4x4/8x8 IQ/IT
- Residual Data SRAM
- Pixel Compensation
- De-blocking
- MPEG-2 Inter
  - Recon. Pixel SRAM
- H.264/SVC Inter
  - Left MB Prediction Data
- H.264/SVC Intra
  - Left MB Pred. Data

AHB

32/64-bit Adjustable Bus Width Interface

- 64-bit

Parameter Bus

H.264 High Profile / SVC Scalable Baseline Profile Decoding Path
MPEG-2 Main Profile Decoding Path
Modules Decoding 8x8 blocks by Looping 4x4 Data Path
Proposed Techniques - System Level Optimization

- **Central Dispatching Prediction Data Management**
  - Control complexity reduction
- **Low Memory Bandwidth Schemes**
  - MB-based frame buffer organization
  - Hybrid block size data reuse
  - Low row/bank switched processing schedule

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**MB-based Address Mapping**

<table>
<thead>
<tr>
<th>Luma</th>
<th>Chroma</th>
<th>Luma</th>
<th>Chroma</th>
<th>Luma</th>
<th>Chroma</th>
<th>Luma</th>
<th>Chroma</th>
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<tbody>
<tr>
<td>16x8</td>
<td>8x8</td>
<td>8x8</td>
<td>4x4</td>
<td>16x8</td>
<td>8x8</td>
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<tr>
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<td>8x8</td>
<td>8x8</td>
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<td>16x8</td>
<td>8x8</td>
<td>16x8</td>
<td>8x8</td>
</tr>
</tbody>
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**Low Memory Bandwidth Schemes**

- **MB-based Frame Buffer Organization**
  - Bandwidth requirement on 64-bit bus (3M cycles/s)

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**Low Row/Bank Switched Processing Schedule**

- **10% latency decreasing**
  - Reduce row/bank switched times

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**Central Dispatching Prediction Data Management**

- **Complexity reduction**

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**System Optimization**

- **Central Dispatching Prediction Data Management**
- **Low Memory Bandwidth Schemes**
  - MB-based frame buffer organization
  - Hybrid block size data reuse
  - Low row/bank switched processing schedule
Proposed Techniques - Component Level Optimization

- High Throughput CABAC Decoding
- Hybrid Block(4x4/8x8) Data Reuse
  - In-loop deblocking filter

Pipeline Scheduling

2.63x throughput speed up in average (at high bit-rate)

Look MPS Ahead Decision Parsing

Bin 1 is decoded if fit look ahead Eq:

\[ \text{codiRange} > \text{codiOffset} \]

(MPS of bin 0, Re-normalize 0/1 bit only)

Decoding 2 bins at most in a cycle

Dual Series Bypass Parsing

Zero stop mode

Fixed length mode

Stop if encounter 0

Decoding 4 bins at most in a cycle

Cycles

Set boundary strength = 0 (none filtering mode)

4x4 block

8x8 block

Looping 4x4 data path for 8x8 blocks

30% SRAM cost reduction
FPGA & Chip Implementation

- Supporting Scalability

FPGA XILINX V4-160

FIE8100

<table>
<thead>
<tr>
<th>Designs</th>
<th>Proposed Design</th>
</tr>
</thead>
<tbody>
<tr>
<td>Specification</td>
<td>MPEG-2 MP</td>
</tr>
<tr>
<td>Gate Count</td>
<td>439K</td>
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<tr>
<td>SRAM Size</td>
<td>10.9KB</td>
</tr>
<tr>
<td>Clock Rate</td>
<td>150 MHz (H.264, HD1080@30fps)</td>
</tr>
<tr>
<td>SDRAM Bus</td>
<td>Single SDR 32/64-bit adjustable bus</td>
</tr>
<tr>
<td>Technology</td>
<td>0.13μm</td>
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<tr>
<td>Power</td>
<td>328mW (HD1080)</td>
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