Design and Evaluation of Variable Stages Pipeline (VSP) Processor Chip

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Battery life is a problem for mobile computers

- Mobile computers are required to achieve both **Low energy** and **High performance**.

We propose low energy processor architecture
VSP (Variable Stages Pipeline)

High Speed (HS) mode
• Deep (super) pipeline
• High frequency
• High performance
• High energy

Low Energy (LE) mode
• Short pipeline
• Low frequency
• Low performance
• Low energy

Vary the pipeline depth dynamically.

Glitch propagation becomes serious problem.
VSP (Variable Stages Pipeline)

High Speed (HS) mode
• Deep (super) pipeline
• High frequency
• High performance
• High energy

Low Energy (LE) mode
• Short pipeline
• Low frequency
• Low performance
• Low energy

Vary the pipeline depth dynamically.

LDS-cell prevent glitch propagation.
LSI Design

<table>
<thead>
<tr>
<th>Technology</th>
<th>ROHM0.18μm CMOS process</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard cell library</td>
<td>VDEC Kyoto University Library</td>
</tr>
<tr>
<td>Chip size</td>
<td>2.5 × 5.0 mm²</td>
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<tr>
<td>Measure energy</td>
<td>HP83000 LSI tester</td>
</tr>
</tbody>
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<table>
<thead>
<tr>
<th></th>
<th>HS mode</th>
<th>LE mode</th>
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<tbody>
<tr>
<td>Instruction set architecture</td>
<td>MIPS R3000</td>
<td></td>
</tr>
<tr>
<td>Pipeline depth</td>
<td>9 stages</td>
<td>3 stages</td>
</tr>
<tr>
<td>Target frequency</td>
<td>100 MHz</td>
<td>25 MHz</td>
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<tr>
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<th>VSP</th>
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<tr>
<td>Number of transistor</td>
<td>521,971</td>
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VSP can reduce 13% energy than conventional approach.